A Paradigm Shift in Digital System Design Education With Industry Participation

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Abstract

While the commercial Electronic Design Automation (EDA) and the academic/industrial research communities have been aware of the requirement for an intensive effort to study the digital system design practice in its entirety, resource needs, fuzzy objectives, and short-time horizon have handicapped progress. The Rapid Prototyping of Application Specific Signal Processors (RASSP) program is a major ARPA/Tri-Service effort that is overcoming these previous handicaps. This effort is bringing a number of new technologies that will lead to shorter prototyping times, improved product quality, and reduced life cycle costs to fruition. In an effort to ensure the successful transfer of these new technologies, the RASSP Education & Facilitation (RASSP E&F) program is working with small and medium size universities to incorporate these new technologies into their undergraduate and graduate curricula. Only by successfully inserting these rapid-prototyping technologies into the curricula and research activities of the university community will the long term benefits of these technologies be realized. This paper discusses the need to change the existing embedded digital system design education paradigm, and the efforts being undertaken by the RASSP E&F program to work with the university community to effect this change. The result is a clarion call to stimulate academic participation in a progressive educational program that adopts the latest instructional methods and industrial strength tools to revolutionize the way system design is taught in United State's colleges and universities.

1. Introduction

Embedded digital systems are those digital electronics systems that are dedicated to specific applications, include both hardware and software, and customarily operate in rigid real-time, standalone environments. The market for embedded digital systems is estimated to be about two orders of magnitude larger than the personal computer (PC) market[1]. Significantly, its share as a percent of the total electronics market is growing due to products that increasingly rely upon embedded electronics to provide the flexibility consumers want. This situation is evidenced in smart cards that are automating a variety of transactions (banking, medical, etc.) to smart military systems that enable a "fire and forget" paradigm.

In 1993, the Department of Defense (DoD) ARPA and Tri-Services initiated a major, $150M, 4.5 year effort, called the Rapid Prototyping of Application-Specific Signal Processors (RASSP) program, focused on improving the process by which embedded digital systems are designed. The technologies being developed by the RASSP program will be instrumental in enabling the cost-effective development of the smart embedded digital systems desired today.

To ensure the successful transfer of RASSP program technologies in the longer-term, these technologies need to be reflected in the curricula of our academic institutions. Today, digital system design education is focused on a limited subset of embedded digital system applications. The academic focus tends to be on applications that are limited in complexity, lack real-time constraints, and can generally be satisfied by "hardware-only" implementations due to their limited flexibility[2,3]. The design of larger systems is taught via extrapolation of this approach.

The current education curricula (circa 1980), designed to support the design and implementation of digital systems, has been able to produce graduates that satisfied industry's needs because product lifetimes and therefore, time-to-market requirements were sufficiently generous (in order of years), to allow industry to use "brute-force" or inefficient design methodologies for larger embedded systems. However, the tremendous advances in electronics manufacturing technology and concomitant increase in the complexity and capability of the embedded digital systems used in the "smart" products sold today means that industry can no longer rely upon these inefficient design techniques. Industry needs engineers that are trained in the latest, most effective embedded digital system design technologies. To meet this industrial need, the educational modus operandi must be updated to incorporate the revolutionary new design techniques being developed in the RASSP program and elsewhere. In effect, a paradigm shift in digital system design education is needed.

This paper will describe a novel educational program that will ensure the successful transfer of the new technologies and associated tools being developed for the design and implementation of next generation products. This program is designed to allow the incorporation of not only the RASSP-developed technologies, but also all future technologies necessary for improved products and processes. The key strengths of this program are two-fold. First, the program is modular so that academic programs can use only those portions that are appropriate. Second, the program supports the continuous upgrade of the material, thereby making the educational material always up-to-date, and the potential for involvement of all participants in the education of system design. The later attribute of this effort creates the potential for a program that can outlive the RASSP program.

The remainder of this paper is organized as follows. Section 2 presents the system design process currently employed by industry. Section 3 presents the ARPA/Tri-Service RASSP program and addresses the shortcomings in the current state-of-the-art practices for embedded system design. Section 4 describes the RASSP E&F program, and how it addresses the transfer of RASSP program technologies to the industry. Section 5 presents the RASSP E&F university education program and contains an overview of the curricula development process. Conclusions are found in Section 6.

2. Current Digital System Design Practice

A high-level model of the current digital system design process is presented in Figure 1. This model, developed through a series of interviews with representatives from several different industrial organizations (including Hughes, Motorola, Lockheed Martin, and TI), presents the various stages in the current "waterfall" design process. The stages are demarcated and minimum and maximum time ranges for each stage are presented. The model is based upon design experience for large systems consisting of between 30 to 160 processing elements and processing between 80 and 700 Mbytes of data per second[4].

Figure 1 shows that the current design process for digital systems focuses the majority of time and effort (70%) on the detailed hardware design activities. Out of a total of between 37 and 73 months to prototype a large multi-board embedded system from system requirements definition to production and deployment, only token attention is paid to the system design process. This situation exists in spite of the fact that the front-end of the design process is where most of the life-cycle costs for the system being developed are determined[5]. Although not obvious from Figure 1, it is important to note that today the software development process is performed largely independent of the hardware design process. As a result, the current digital system design process expends significant and unnecessary time and effort on redesign to correct problems that are only identified during the hardware/software and subsystem/system integration processes.

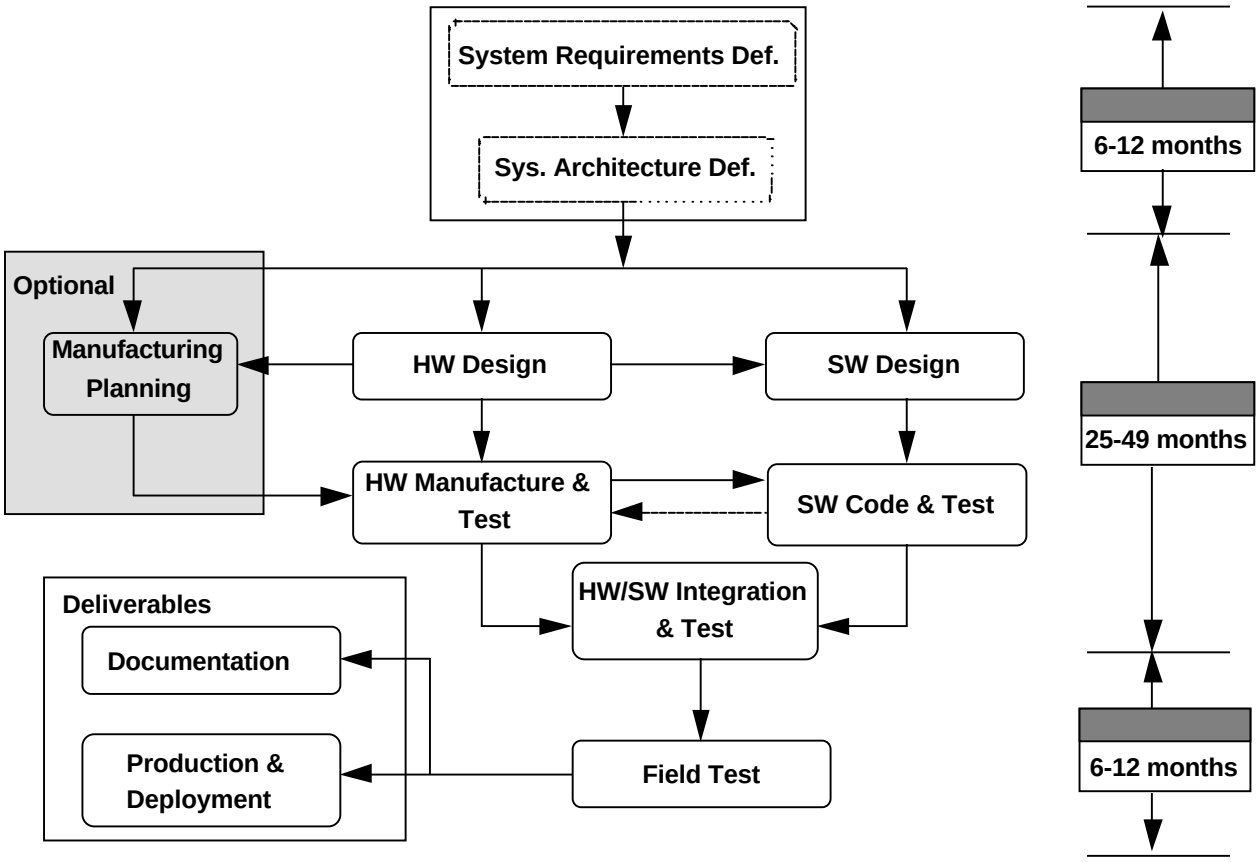

Figure 1: Current System Design Practice (circa 1993);
System Size: 30-150 processing elements, 80-700 Mbytes/sec.

To date, the current design process for embedded digital systems has been adequate because product lifetimes and therefore time to market requirements were sufficiently generous (in order of years) to allow the use of "brute-force" or inefficient design methodologies. This is no longer acceptable for the following reasons:

1. The electronics applications of current interest represent complete "systems", as opposed to dedicated hardware chips.

2. The majority of current applications involve considerable coupling between hardware and software during development which requires the hardware and software design tasks to be tightly integrated to form a *codesign* process.

3. The lifetime for systems has become dramatically shorter due to the tremendous rate of improvement in implementation technologies resulting in new market pressures that require design cycle times for large electronic systems be reduced from years to months, with no impact on quality.

4. Competitive pressures have also required that the cost of these systems be reduced by an order of magnitude.

The application needs of industry and government are driving the development of new design methodologies that can overcome the problems described above. To keep the industry competitive it is imperative that rapid transfer of this technology takes place.

3. The RASSP Technology Program

The Rapid Prototyping of Application Specific Signal Processors (RASSP) Program is a $150M Department of Defense (DoD) Advanced Research Projects Agency (ARPA) and Tri-Services initiative (1993-1997) intended to dramatically improve the way complex digital systems, particularly embedded digital signal processors, are designed, manufactured, upgraded, and supported. The target RASSP improvement is at least a four-fold (4x) reduction in the time to go from design concept to fielded prototype. Equivalent improvements in cost and quality are also targets. The motivation for the RASSP initiative is the pervasive need for affordable embedded signal processors throughout a wide range of electronic systems[5].

RASSP is aimed at the design of embedded digital electronic systems that typically have one or more boards, a variety of implementation technologies and interfaces, and a wide range of data rates. Since such systems are found in many applications, the strong RASSP focus on a specific problem domain (signal processing) is needed to keep the goals achievable. The overall RASSP technical approach is to coordinate and integrate improvements in *processor architecture*; *design methodology*; and *electronic design infrastructure*.

For processor architectures, the focus is on scaleable and modular architectures[6,7]. The architecture approach has three primary targets: 1) programmable embedded hardware, 2) embedded software, and 3) standard interfaces. For embedded software, the focus is reliable, real-time software that is modular in order to promote software reuse and simplify upgrade. For embedded hardware, the focus is programmable processors with scaleable interconnect and smart interfaces. Two notable characteristics for both software and hardware interfaces are wide use within industry and scaleability.

For design methodology, the RASSP approach is to capitalize on development techniques that have been widely explored and have demonstrated their value[8,9]. The primary techniques being focused on are concurrent engineering, top-down and spiral design, and simulation-based design methods such as virtual prototyping and executable specifications.

For design infrastructure, including such items as better system design automation tools, reuse libraries, and enterprise integration capabilities, the RASSP approach is to leverage the investments being made in the commercial EDA arena and to focus on system level design capabilities and enterprise integration[10,11]. The

primary focus in system level design aids is on the development and integration of better architectural tradeoff and selection tools that can play a valuable role in a top-down, codesign oriented design process. In the area of enterprise integration, the focus is on supporting collaborative design in a distributed environment and includes efforts directed at tool integration, enterprise level product data management, enterprise reuse library systems, and design methodology management systems.

RASSP is focused on the effort to bring these three diverse areas together in a consistent methodology integrated with both the automation infrastructure and the processor architecture approaches. Efforts have been directed toward filling the gaps that prevent wide use of these techniques.

Within its first two years, the RASSP program has resulted in a number of technical contributions to the area of digital system design. These include:

- A new technique for design requirements documentation and specification --- executable specifications.
- A new design methodology for design without actual manufacturing or hardware prototyping --- virtual prototyping. Virtual prototyping allows for rapid design and test within a simulation-based software environment.
- A integrated tool environment, allowing a number of design tools to work together in an efficient manner.
- A number of new tools for architectural design of multiprocessor systems that support the reuse of information from previous projects to enable organization-specific and application-specific tradeoffs.
- Development of virtual corporations that facilitate the rapid creation of multidisciplinary teams (design, manufacture, and support) across different organizations that can design products together.
- New design methodologies for hardware/software codesign and test.
- The technology for model year upgrades of existing embedded systems based upon the effective reuse of past designs.

The technologies being developed by RASSP will be instrumental to promoting the cost-effective development of the smart embedded digital systems desired today .

4. The RASSP Education & Facilitation Program

Successfully transferring the technology being developed by the RASSP program to industry and academia is a critical component of the overall RASSP effort. To accomplish this goal, a novel RASSP Education & Facilitation (RASSP E&F) program was defined and a team was tasked with leading the RASSP technology transfer efforts. The RASSP E&F program was awarded in June 1994 to a team led by SCRA with team members from the Georgia Institute of Technology, the University of Virginia, Raytheon, the University of Cincinnati, Arthur D. Little and Enterprise Integration Technologies (EIT).

To successfully transfer RASSP technology, the RASSP E&F effort must teach engineers and scientists how to use the RASSP top-down design concepts and give managers an appreciation for the potential payoff of

RASSP technology, thereby simultaneously creating a technology push and technology pull. To accomplish this goal, the RASSP E&F team has adopted a multi-faceted approach. This approach is designed to help push and pull individuals and organizations through the five step technology transfer process illustrated in Figure 2.

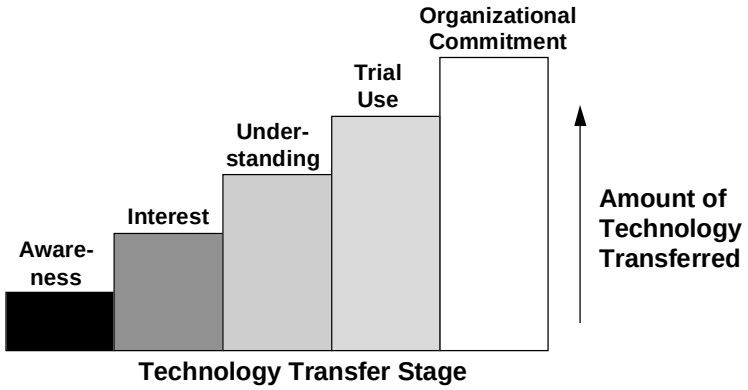

Figure 2: Technology Transfer Process

Accomplishing this process involves: 1) making available the information/knowledge necessary to progress from one stage of the process to the next and 2) providing an education process that will assist in the transfer process. The RASSP E&F objective in each area is described below:

- Information: develop awareness and interest in RASSP technology by providing easy access to useful and well organized RASSP-related information.

- Education: educate senior management as to the potential benefits obtainable through the application of RASSP technology thereby stimulating the use of RASSP technology and the demand for RASSP trained professionals; work with universities to effect a paradigm shift in the graduate, undergraduate, and continuing professional digital system design curricula of small- and medium-sized universities to ensure that graduating students can meet industry's need for RASSP trained engineers, scientists, and managers.

The activities of the RASSP E&F program in each of these areas is discussed in more detail next.

4.1 Information

To develop awareness and interest in RASSP technology, the RASSP E&F program is providing ubiquitous access to RASSP information in a number of ways. A World Wide Web (WWW) site **<http://rassp.scra.org/>** for the RASSP program has been established. This WWW site was identified in *IEEE Spectrum* as one of the top-three web sites for Digital Signal Processing (DSP)[12]. The RASSP WWW site contains both general and specific RASSP information including a RASSP overview, technical documents from RASSP contractors, and educational material to support the teaching of the advanced methods being developed by the RASSP program. In addition to the RASSP WWW site, a quarterly periodical, entitled *The RASSP Digest*, is published that provides insight into the accomplishments and progress obtained in RASSP and other related programs. Technical articles and conference tutorials and papers are also developed to facilitate information distribution.

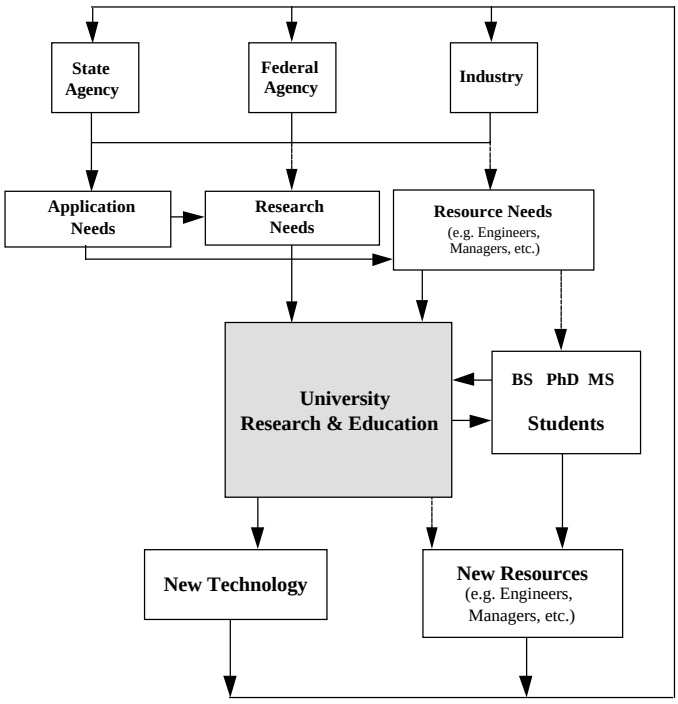

Figure 3: Relating industry and government to the university education and research program

4.2 Executive and University Education

To help create a pull for the RASSP technology and professionals versed in that technology, a series of Executive Seminars have been developed and delivered. Targeting senior executives in industry and government, these seminars are designed to generate understanding and the willingness to incorporate RASSP technology into their business by focusing on the business implications underlying the RASSP technology and presenting the business case behind this technology. To date, seminars have been given to senior managers in such places as the Georgia Tech Research Institute (GTRI), the National Security Agency (NSA), Texas Instruments, Allied Signal Corporation, NASA, and the Army Missile Command.

To create the technology push for RASSP, an innovative program targeted primarily small- and medium-sized universities has been established. As is illustrated in Figure 3, the education and research programs within universities are ultimately driven by the application needs of industry and government. These application areas determine the types of *resources* (e.g., qualified personnel) and *technologies* (e.g., research) that industry and government need from the university community. To ensure the successful transfer of RASSP technologies over the long-term, these technologies must be reflected in the curricula of the academic institutions. This approach will assure that industry's need for "resources" who understand the RASSP technology and for improvements to that technology will be met by the university community. This approach will also provide the RASSP technology push that will complement the technology pull being created through the Executive Seminars. Furthermore, given the increasing rate of technological change in the area of embedded digital systems, it is important that mechanisms be established that will help assure that the academic community can meet the changing needs of industry and government.

5. RASSP E&F University Education

The current curricula for digital system design was developed in the early 1980's with the onset of the silicon revolution. The focus has been on the design of products that are relatively simple and inflexible in application, and can be rapidly realized out of simpler hardware building blocks and implemented using VLSI technology[4,5]. These designs require very little software beyond that for simple setup and control. In the current paradigm, there is little link between advanced theoretical algorithms designed within laboratories and their final implementation to meet an application-specific need. The curricula of the early 1980's reflected the level of digital design complexity of the late 1970's. At that time the need for shorter design times, the need for hardware/software codesign, and life cycle cost issues, brought on by increasing design complexity, had not become apparent.

However, by the late eighties, the tremendous advances in electronics manufacturing technology and concomitant increase in the complexity and capability of the embedded digital systems used in the "smart" products being sold indicated that the educational modus operandi needed to be adapted. For example, the application of theory in the form of hands-on design through labs was being advocated by Denning, et.al.[13]. The report *Computing Curricula 1991*[14] proposed that rigid programs be made more flexible and sensitive to individual goals. This report proposes the use of "knowledge units" which contain a discrete amount of related topical information to achieve these objectives.

The need to update the existing curricula is further evidenced by a recent survey sponsored by Texas Instruments and Toshiba. The results of this survey, designed to assess the status of hardware description language (HDL) education in engineering schools within universities in the United States and Japan[15], are summarized in Table 1. Given the importance of top-down, language-based design techniques to meet the design challenges brought about by the rapid change in manufacturing capabilities, the results of this survey are significant. Indeed, this survey stimulated Robert Rozeboom, VP of Texas Instruments, to say, *"It's clear there is a significant need, and therefore, opportunity to increase the amount of training among undergraduate electrical engineering students at major universities worldwide*[16]*."*

Through the RASSP E&F program, ARPA and the Tri-Services are working to help universities adapt their curricula to incorporate RASSP technology so that tomorrow's graduates (BS, MS, Ph.D.) will be able to better meet the needs of industry and government. The approach being taken is to not only help the university community incorporate RASSP technology today, but also to establish a framework that will help the university community to effectively and efficiently respond to the ever changing needs of industry and government brought on by the dramatic rate of technological change.

5.1 Module-Based Courses and Curricula

The RASSP E&F team has developed a novel module-based framework that can be used to efficiently insert the technology being generated on the RASSP program into university curricula. Similar to the knowledge unit concept proposed by the Joint Curriculum Task force[13] , modules are developed on specific topics and used to develop courses. The attractiveness of this approach is that it is easy to insert new material (through the use of a module) into an existing course. This technique is extremely important because of momentum of curricula development.

Table 1: Survey Summary

Average Percent of Graduating Seniors with Working Knowledge of Language			
	UNIX/C	**VHDL**	**Verilog**
Japan	70%	2%	2%
U.S.	60%	14%	8%

Each module consists of a comprehensive discussion of one technical sub-area, (e.g., virtual prototyping) and presents the technical details, examples, and case studies needed to obtain a thorough understanding of the topic. The specific material found in a module includes such items as presentation materials, notes on presentation materials, predefined laboratories, and homework problems with solutions.

A typical module, illustrated in Figure 4, consists of three components. The first component is the fundamental core of design principles (e.g., in a high speed IIR digital filter design module, it could outline the use on the basic operations such as retiming, pipelining, and unfolding of the flow graph). The second component consists of examples, metrics, case studies and problems. This component provides simple examples that illustrate the theory covered in the fundamental core and provides problems that can be used for homework exercises. The third component of a module is a hands-on laboratory exercise. The laboratory exercise is intended to rigorously demonstrate the concepts taught in the other sections of the module by providing an opportunity to apply those theories on significant problems in a “learn by doing” fashion.

Each module represents a unit of a course that is independent of other modules in the course (aside from prerequisite or post-requisite requirements). A typical module is designed to provide three hours of lecture time. The laboratory portion of a module may actually not exist for all modules or may span multiple modules. In the ideal situation, the lab components represent a continuous, semester long design project broken into smaller pieces.

There are many advantages to encapsulating a focused amount of material in a modular fashion. These include:

- Modules can be used in a "mix and match" scenario, depending upon the particular area of digital system design as well as the target audience needs;

- As technology advances in an area, only modifications to applicable modules are necessary. This approach reduces the cost of upkeep and makes it easier to keep pace with the rapid pace of technological change;

- Modules can be easily incorporated into existing graduate or advanced undergraduate courses within a university.

Table 2 presents the modules that have been or are being developed by the RASSP E&F team. Each module is developed by the organization with the greatest strength in that technical topic. For example, the Real-Time Systems module was developed by the Georgia Institute of Technology, whereas the Design for Manufacturability module was developed by Raytheon. Because the development of each module may be done by a different author, a standard template was developed to maintain a consistent format amongst the modules.

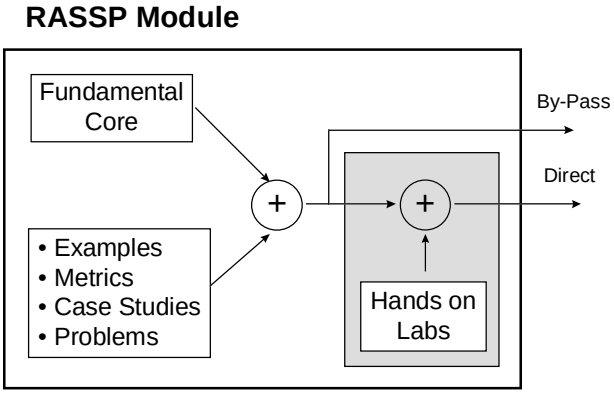

Figure 4: RASSP Module

After initial development, each module goes through an extensive review process beginning with an internal RASSP E&F peer review, which aligns the modules' focus for coherent course integration. Because authors have different styles, care must be taken to maintain consistency in module formats, terminology, and content, in terms of depth and detail. External review by independent experts from academia and industry helps to assure correctness and relevancy of the information captured in the modules.

The presentation material is being developed using Microsoft PowerPoint(TM), version 4.0. The slides use bulletized text, illustrations, etc. to communicate the subject matter. Associated with each slide is a "notes page." These notes provide the instructor with in-depth information including background, context, and references for further topic exploration. If desired, copies of the slides may be provided to the students. Although the hard copies tend to be in black and white, the presentations are in full color, when shown with an projection system.

One of the key challenges in the development of module-based RASSP curricula is determining what modules should be developed. The relationship between the module definition process and a module-based RASSP curriculum is presented in Figure 5. Using this technique, an example concentration area within a masters degree program is illustrated by the three courses shown in Table 2. These courses, RASSP 100, RASSP 101 and RASSP 102 are being piloted at the University of Virginia, the University of Cincinnati and the Georgia Institute of Technology.

The proposed university course sequence begins with RASSP 100, which focuses on rapid prototyping using VHDL, and explores the different levels of modeling, the relatively new practice of hardware/software codesign, and library reuse. It is followed by RASSP 101 and RASSP 102. RASSP 101 explores DSP algorithms and architectures in detail. RASSP 102 then examines some of the enterprise level issues associated with embedded digital system design. Not shown in Table 1, RASSP 103, is a project-based course designed to apply the principles learned from the earlier RASSP courses and to expose the student to a “near” industry scale problem. Table 1 also illustrates the flexibility of the modular approach.

By defining a module-based framework, proposing a example curriculum, and developing specific course material, the RASSP E&F program is creating an infrastructure that can help to ease transition from today’s circuit design dominated curricula, to curricula that incorporates the spectrum of top-down design

Table 2: Module Based RASSP Curriculum
(Shaded box indicates module is included in course)

Module	RASSP 100	RASSP 101	RASSP 102
System Level Modeling	■	■	
VHDL Basics	■		
Structural VHDL	■		
Behavioral VHDL	■		
System-level VHDL	■		
Hardware/Software Codesign	■		
HW/SW Partitioning		■	
Introduction to DSP		■	
DSP Architectures		■	
Scheduling & Assignment for DSP		■	
Algorithm/Functional Design		■	
Communication and I/O protocols		■	
Real Time Systems			■
RASSP Methodology Overview	■	■	
Requirements and Specification			■
Virtual Prototyping for DSP Architectures		■	
Virtual Prototyping with VHDL	■		
Hardware Synthesis Overview	■		
Libraries: Generation, Maintenance, and Documentation	■		
Enterprise Integration			■
Electronic Produce Life Cycle Analysis			■
Robust Design Practices			■
Project Management			■
Test Technology Overview	■		
Design for Manufacturing			■
Virtual Prototyping lab		■	
Cost Modeling & Analysis			■
Tradeoffs Analysis			■

capabilities needed to design sophisticated, embedded digital systems. The most significant attribute of the module based approach is its ability to outlive the RASSP program and be ultimately "managed" by the education community itself. It is also generic in such a way that it can help universities more easily adapt to the rapidly changing state-of-the-art in embedded system design technology.

5.2 Transferring the E&F Education Framework

In addition to developing an infrastructure to assist in the transfer of the RASSP technology, the RASSP E&F team is leading a series of "teach the teacher" educator workshops. These workshops are designed to

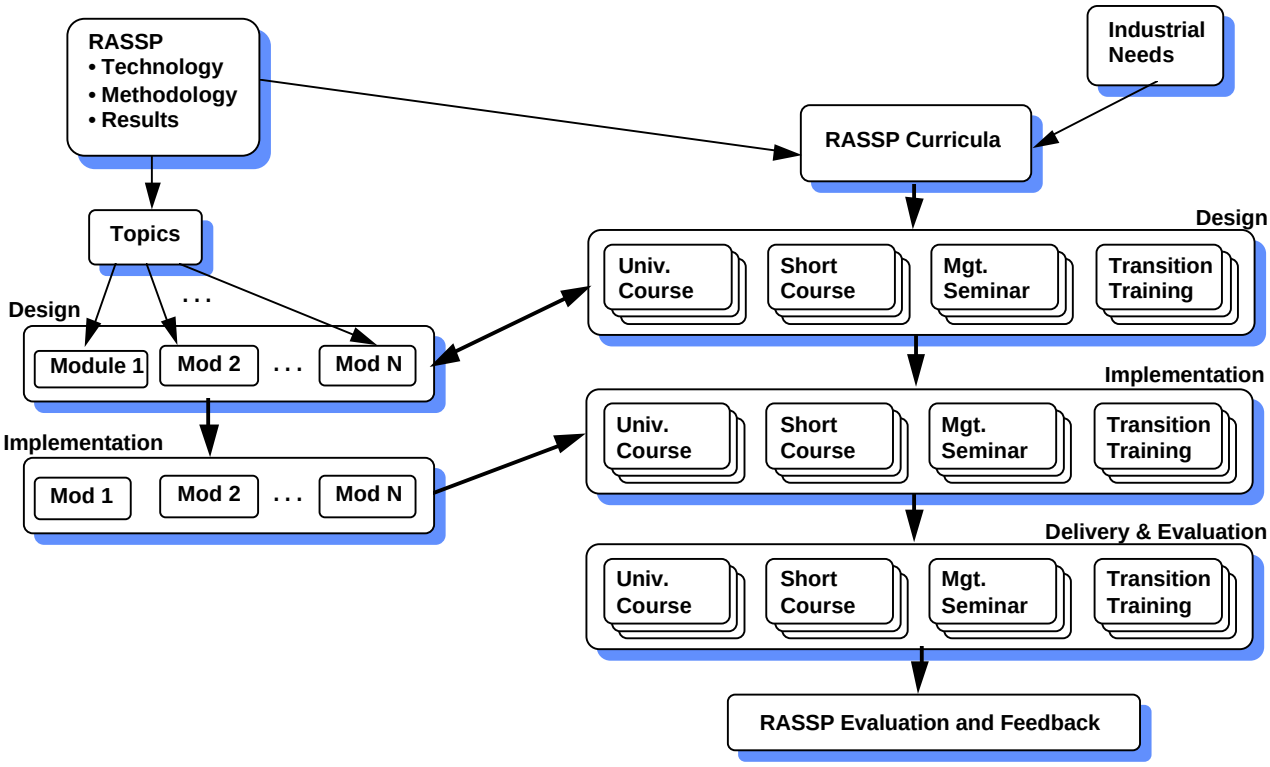

Figure 5: Developing a New Curriculum for Embedded Digital System Design

provide instructors with the understanding and material they need to include the latest technology in the classes they teach. The RASSP E&F team is working with other organizations, for example, the National Science Foundation and VHDL International (VI), to ensure that the widest possible benefits are derived from these workshops.

Working together with VI, the first of these workshops will focus on VHDL and its use in top-down design (Figure 6). VI is working with its members to ensure low or no cost access to VHDL software for universities. Together, the VI and RASSP E&F efforts will provide the impetus for addressing the need so clearly stated by Robert Rozeboom, VP of Texas Instruments.

6. Conclusions

The RASSP Education and Facilitation team has been tasked with leading the RASSP technology transfer efforts. Very early in the process, the E&F team realized one of the key elements to a successful transfer of RASSP technology was the incorporation of the technology into academic programs. Realizing how hard it is to insert new technologies into a curriculum, the E&F team developed a novel approach to accomplish this task. This new approach, based on the development of technology modules, is currently being tested at the various universities of the team members. At the same time, the E&F team is initiating programs to see that this approach and the RASSP technology is adopted by the academic community. It is anticipated that the approach and the specific modules will be of significant benefit to the educational community, given the enormous task of keeping curricula current with the advances in microelectronics. The ultimate goal is that, as students at all

levels (BS, MS, and Ph.D.) graduate and enter the workforce, industry will reap the benefit of the updated curriculum through more qualified engineers.

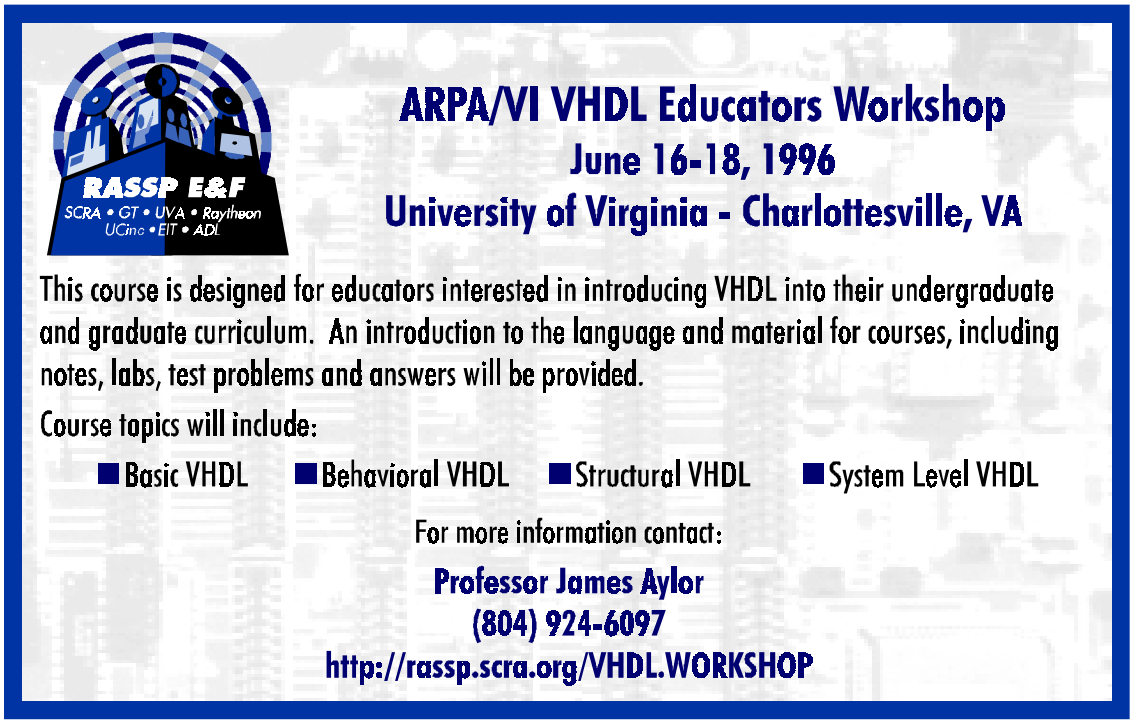

Figure 6: ARPA/VI VHDL Educators Workshop

Acknowledgments

The authors gratefully acknowledge the help of Prof. Harold Carter of the University of Cincinnati, the valuable input provided by all of the RASSP E&F team members (Tom Egolf, Shahram Famorzadeh, Max Salinas, Dr. R. Klenke), and the support from the Advanced Research Projects Agency Electronics Technology Office (ARPA/ETO) and United States Air Force Wright Aeronautical Laboratory under contract number F33615-94-C-1457 without whose support this work would not have been possible.

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Biography

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