2006-1020: AN EXEMPLARY CURRICULA WITH PROPER MIX OF ENGINEERING FUNDAMENTALS AND TRAINING STUDENTS AT STATE-OF-ART TECHNOLOGY

Kanti Prasad, University of Massachusetts-Lowell

An Exemplary Curricula With Proper Mix Of Engineering Fundamentals And Training Students At State-Of-Art Technology.

Kanti Prasad Ph.D.; P.E., Professor/Director
Microelectronics/VLSI Technology
ECE Dept., UMASS Lowell

Abstract:

The author established state-of-art laboratories in VLSI Design and Fabrication in 1984, and 1986 respectively at University of Massachusetts Lowell, and continually updating them. In addition he initiated courses e.g. 16.469, 15.502, and 16.602 in VLSI Design / VHDL Based Design and 16.470, 16.504 in the VLSI Fabrication field, teaching and updating these courses continually. In addition, the author initiated and taught courses such as 16.661 Local Area / Computer Networking, 16571 Microwave Monolithic Integrated Circuits (MMIC) Design and Fabrication and 16.547 Introduction to ITS Technologies. All these coursed demonstrate a proper mix of engineering fundamentals and training students at state-of-art technology, as will be evident from the course syllabi.

But the author felt astonished, how deeply this topic was germane to the industry as revealed at 50th anniversary of American Electronic Association celebrated at Motorola Campus at Schaumburg Illinois in 1995. Executive V.P. of Motorola articulated in his inaugural address, "Industry neither has Resources nor Will to train the people. Universities will have to do both i.e. teaching fundamentals as well as training the students on some state-of-art technology, so that they are productive right away". Dr. John White (Dean of Georgia Tech, then) said, "Our job is to teach Fundamentals". Motorola's executive V.P. said, "You will be history, and to prove my point I am awarding $ one million to Purdue University to come out with an integrated curriculum, which will accomplish both".

I came overwhelmed with enthusiasm and shared this conversation with our Chancellor William T. Hogan who said, "This is our mission in the university". I felt deeply relieved, that we were doing the right thing. On September 30, 2005 our chancellor invited leaders from Academia, Industry and Government to examine whether we are on right track at preparing the students broad enough at multi-disciplines in wake of global competition. Dr. Curtis Tompkins Emeritus President of Michigan Tech, and presently Director of Volpe Center assured the author that these issues are very dear to the heart of Dr. John White, presently President of Arkansas University, and Member on Motorola Board.

The author involved leaders namely Robert Meisenhelder from Analog Devices, Dr. Bradley Barber from Skyworks Solutions, Lisa Auction, Dr. Chris Carroll and Dr. Tom Kazior from Raytheon and Dr. John Vaughan from MA/Com. The issue of integrated curriculum is of prime importance to these national leaders. Preparing the students at UMASS Lowell with a proper mix of engineering fundamentals and training at state-of-art technology, so that they are reproductive on the job right away in the topmost percentage. It is because of this sublime endeavor of the department in general, and that of the author in particular, there is hardly any Hi-

Tech industry in the nation, where our alumni are not in significant numbers in leading jobs. Details of all these endeavors will be presented in the papers.

1. Introduction:

The author established state-of-art laboratories in VLSI Design and Fabrication in 1984, and 1986 respectively at University of Massachusetts Lowell, and continually upgrading them. In addition he initiated courses namely 16.469, 15.502, and 16.602 in VLSI Design / VHDL Based Design and 16.470, 16.504 in the VLSI Fabrication field, teaching and updating these courses continually. In addition, the author initiated and taught courses such as 16.661 Local Area/Computer Networking, 16.571 Microwave Monolithic Integrated Circuits (MMIC) Design and Fabrication and 16.547 Intelligent Transportation and Systems Technologies. All these courses demonstrate a proper mix of engineering fundamentals and training students at the state-of-art technology, as will be evident from the course syllabi at http://www.uml.edu/college/engineering/ece/.

The author however, felt astonished, how deeply this topic was germane to the industry as revealed at 50th anniversary of American Electronic Association celebrated at Motorola Campus at Schaumburg Illinois in 1993. Executive V.P. of Motorola articulated in his inaugural address, "Industry neither has Resources nor Will to train the people. Universities will have to do both i.e. teaching fundamentals as well as training the students on some state-of-art technology, so that they are productive right away". Dr. John White (Dean of Georgia Tech, then) said, "Our job is to teach Fundamentals". Motorola's executive V.P. said, "You will be history, and to prove my point I am awarding $ one million to Purdue University to come up with an integrated curriculum, which will accomplish both".

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2. Challenge to the Teacher and Taught

The global competition in High Technology, in general, and chip technology including very large scale integration (VLSI) and microwave monolithic integrated circuits (MMIC), in particular, has posed a challenge to the Teacher and the Taught. The most essential qualifications for the Teacher are: (1) mastery over the knowledge of the subject matter, (2) capability of transforming pertinent information continually available in the field into knowledge through integration with his own database. Only those people, who know the latter are called WISE, else, they remain OTHERWISE. Never, in the history, such a challenge as posed by CHIP technology, has presented the human race, where perfection is demanded at each stage of chip design, including test, simulation, all processing steps required for its fabrication along with consummate

testing; packaging and meeting its ISO 9000 reliability guidelines. The foundry needs a billion dollar investment in order to turn chips costing few dollars each. This challenge is being met at the University of Massachusetts Lowell through the development of Microelectronics Engineering Education Model by the author, and its implementation has culminated into proper mix of fundamentals and proper training for 21st century graduates.

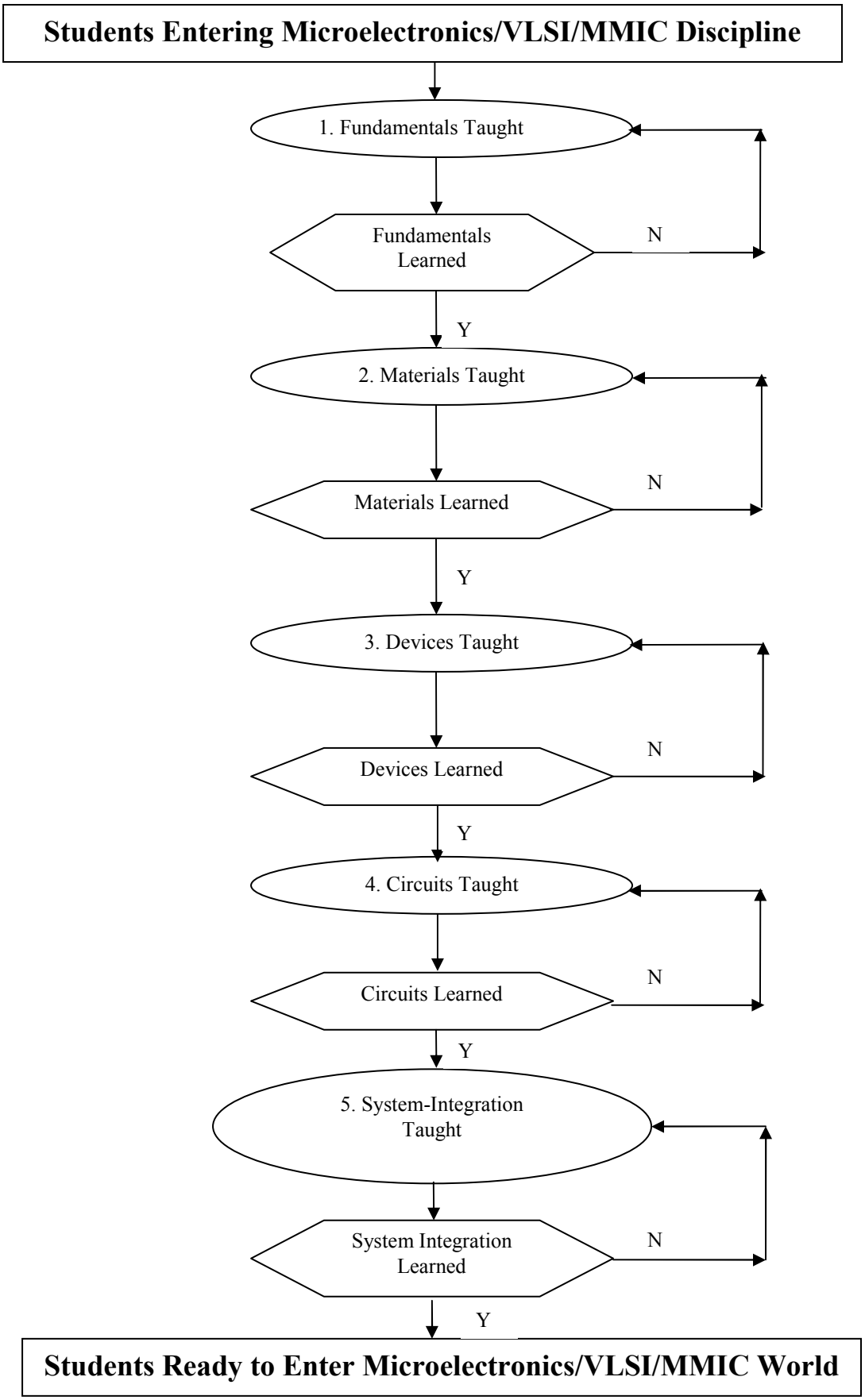
Teaching microelectronics / VLSI / MMIC technology presents a real challenge, because it demands a deep understanding of fundamentals as contained in physics, chemistry and mathematics. In addition, it demands knowledge in several distinct disciplines, such as materials including their chemical, mechanical and electrical properties, semiconductor phenomenon including modeling and simulation, non-linear circuit theory and system micro-architecture. Chip design is an integral part of VLSI/MMIC technology, which encompasses multiple levels of abstraction including electromagnetic field theory, topology, switching theory, semiconductor processing, packaging and reliability, along with their test and simulation procedures. The designer is challenged to transcend these disparate disciplines and transform them into detailed specifications for a chip that can be manufactured.

The author is successful in imparting such education because of his B.Sc. in Physics, Chemistry and Mathematics, along with B.E. in Telecommunication Engineering, and latter completing Ph.D. in Solid State Electronics. In the quest of mastering the discipline of VLSI/MMIC design, he took advanced graduate courses: 1. Computer Architecture. 2. Stochastic Controls, 3. Communication Theory 4. Speech Processing 5. Image Processing 6. VLSI Design, 7. Advanced VLSI 8. Thin Film Technology and 9. Parallel Processing, from university of South Carolina and Massachusetts Institute of Technology. In addition, the author has continued interaction with the regional industries of national/international eminence such as Skyworks Solutions, MA/Com, Analog Devices, Digital Equipment, Watson's Research Center, Raytheon Microelectronics Center, Sander's MMIC Technology and Volpe National Transportation Systems Center. These interactions have been/are in the form of research grants, summer faculty fellowship, consulting, and industrial training or engineering seminars.

3. VLSI Engineering and Technology Education Model

Based on forty years of dedicated teaching, consummate research and perpetual service to professional organizations including the American Society of Engineering Education (ASEE), the author has postulated the following model as depicted in figure 1. The fact the students who received microelectronics education in engineering from the University of Massachusetts Lowell have found gainful employment in state-of-the-art industries, with scores of them in key R&D positions, is a testament of the success of the proposed model.

The key is improved monitoring of the content of the courses and interaction with the instructors who are imparting instructions in physics, chemistry and mathematics to engineering students in order to assure the success of phase 1 i.e., Fundamentals. Material science is interdisciplinary in nature within engineering, so some improved interaction is applicable to this phase also. In addition, the author has instituted a lot of material technology in his VLSI Fabrication and MMIC Design and Fabrication courses in order to attain consummate success in phase 2 i.e. materials.


Students Entering Microelectronics/VLSI/MMIC Discipline
1. Fundamentals Taught
Fundamentals Learned
N
Y
2. Materials Taught
Materials Learned
N
Y
3. Devices Taught
Devices Learned
N
Y
4. Circuits Taught
Circuits Learned
N
Y
5. System-Integration Taught
System Integration Learned
N
Y
Students Ready to Enter Microelectronics/VLSI/MMIC World

In the VLSI Fabrication course, the students not only receive theoretical instructions in semiconductor devices, but fabricate them also in the Distributed Semiconductor Instructional Processing Laboratory (DSIP). For example, the students not only theoretically calculate the p-n junction depth "x_j" from the diffusion equation based on Fick's Laws

$$C_{(x,t)} = \frac{Q}{\sqrt{\pi Dt}} \exp\left(-\frac{x_j^{\,2}}{4Dt} \right)$$

but measure the p-n junction depth experimentally with the help of Philtec's sectioner. They not only calculate the oxidation thickness'd' theoretically based on Deal-Groove Model.

$$d^2 + Ad = B(t + \tau)$$

but measure it experimentally with the help of ellipsometer. In addition, devices are emphasized in several other courses, such as, Electronics I and II and Semiconductor Electronics. The DSIPL, however, is the most important laboratory wherein consummate understanding of phase 3 i.e. Devices is ascertained.

At the University of Massachusetts Lowell, Circuits I and II, and Electronics I and II courses embody a very strong suite of instructions, because of maintaining the tradition established by her predecessor institutions Lowell Technological Institute (LTI) and University of Lowell (UOL). In addition, design of circuit methodologies get reinforced in the VLSI Design and MMIC design and Fabrication courses. They assure the success of phase 4 i.e. Circuits in its entirety.

Discrete system design has always been rigorously taught at the University of Massachusetts Lowell and its predecessor institutions. The VLSI Design however are only being taught for the last 20 years, with additions in MMIC system design and VHDL/Verilog based system design. In VLSI, design constraints such as minimization of dissipated power, maximization of the speed, and optimization of device density onto the chip, are dealt with quite extensively. In MMIC system design, the issues predominant at microwaves such as, s-parameters, distributed parameters pertinent to device, as well as packaging, are dealt with detail. For example, during low noise, or power amplifier at microwaves, characterization of pseudomorphic high electron mobility (pHEMT) or metal semiconductor field effect transistor (MESFET), along with their doping profiles in layered-material-structure are explained in entirety.

In order to demonstrate the speed enhancement through software, the author emphasizes four-bit-arithmetic adder design with two distinct design methodologies:

(1) Ripple Carry adder based on

$$S_i = A_i \oplus B_i \oplus C_{i-1}$$
$$C_i = A_i \cdot B_i + A_i \cdot C_{i-1} + B_i \cdot C_{i-1}$$

, and

(2) Look-ahead-carry adder based on:

$$S_i = P_i \cdot \overline{C}_{i-1} + \overline{P} \cdot_i C_{i-1}$$
$$C_i = G_i + P_i \cdot C_{i-1}$$
$$G_i = A_i \cdot B_i$$
$$P_i = A_i \oplus B_i$$

where $C_{i-1} = 0$ in both cases

The execution of time simulation on these two distinct adders depicts the fundamental principle of increasing the speed through software. The similar truth has been established through design of 4-bit conventional multiplier versus the multiplier design based on modified Booth algorithm.

The design rules for the VLSI/MMIC chips can be taught within a few weeks. But designing a chip, which is functional, and meets all the specifications set forth, requires that knowledge of pertinent fields, such as communications, controls, digital systems, microwaves and so forth. Therefore, system design not only poses a challenge to the taught, but to the teacher as well. Because, system design not only demands deep understanding of various facets within electrical and computer engineering, but also other disciplines of engineering such as chemical, mechanical and materials.

4. New Courses and Laboratories at the UMASS Lowell

In the quest of consummate knowledge in the field of microelectronics/VLSI/MMIC technology, the author has initiated, developed and taught the following courses in the department of electrical and computer engineering:

- 16.469/502 VLSI Design
- 16.470/504 VLSI Fabrication
- 16.602 VHDL/Verilog Based Design and Simulation
- 16.517 MMIC Design and Fabrication
- 16.661 Local Area/Computer Networking
- 16.549 Intelligent Transportation System Technologies

The course descriptions can be viewed at http://www.uml.edu/college/engineering/ece/.

The crusade in Microelectronic education the author started much earlier than the 50th anniversary of American Electronics Association. But the essence of having a proper mix of fundamentals with state-of-art training in Hi-technology was fully realized at this conference.

The microelectronics education is pretty costly, maintenance of the clean room facility is a perpetual challenge. It requires a full time technical staff for its adequate maintenance. However, author has found that it could be made cost effective if technical cooperation from regional industries could be secured for equipment maintenance, as is being provided from our

sponsors namely Skyworks Solutions Inc, Analog Devices Inc, Raytheon Company, and MA/Com at the moment.

The author has established "Distributed Semiconductor Instructional Processing Laboratory (DSIPL) and a VLSI Design Laboratory at UMass Lowell through an initial equipment grant of one million dollars from the Massachusetts Microelectronics Center (MMC) and matching institutional grant in 1986, and successfully celebrated its 15th year anniversary through awarding plaques to the sponsors.

4. Conclusion.

'Theory without Practice is utopia, and Practice without Theory is NOT Engineering' has been a beacon of the author's life. The author presents in the class in appropriate mix of theoretical and experimental instructions. The technique of 'hand-on-experience' is the most effective teaching, which creates a conducive environment for learning. Preparing the engineering students, who would withstand the challenge of the 21st century, is of crucial importance that teachers must assure that their teaching gets transformed into learning to its fullest extent. The assessment of teaching/learning is even being demanded by ABET. This will entail alumnus, especially how they perform in the design world of engineering including invention and advancement at their jobs.

The author has collected a sizeable data on alumnus who under this model of microelectronic education. It is a matter of great pride that the model has resulted into spectacular success, as evidenced from their placement/advancement and R&D industries of national/international eminence. Other instructors are thereby encouraged to follow the model in the field of microelectronics/VLSI/MMIC technology and tweek it to suit the instructions in other fields of engineering.

The author involved leaders namely Robert Meisenhelder from Analog Devices, Drs. Bradley Barber and Stan Swearingen from Skyworks Solutions, Lisa Aucoin from Raytheon and Dr. John Vaughan from MA/Com. The issue of integrated curriculum is of prime importance to these national leaders. Preparing the students at UMASS Lowell with a proper mix of engineering fundamentals and training at state-of-the-art technology, so that they are productive on the job right away. It is because of this sublime endeavor of the department in general, and that of the author in particular, there is hardly any Hi-Tech industry in the nation, where our alumni are not in significant numbers in leading positions.

5. Acknowledgement

The author is grateful for university administration and sponsors, Skyworks Solutions, MA/Com, Analog Devices, Raytheon, and to Chancellor Hogan, in particular for encouragement for this DSIPL/Microelectronics Program, especially awarding plaques to the sponsors. Thanks are due to Vinay Kulkarni for helping me in preparing the manuscript. Thanks are due to my wife (Uma Rani) for leaving me alone for countless hours for these dedicated endeavors.

Appendix

Course Descriptions:

UNIVERSITY OF MASSACHUSETTS LOWELL
James B. Francis College of Engineering
Department of Electrical & Computer Engineering

Dr. Kanti Prasad 16.502/469 VLSI DESIGN Fall 2005

TEXT: CMOS VLSI Design: A Circuits and Systems Perspective by Weste & Harris.

REFERENCES:

1. Introduction to VLSI Systems by Mead & Conway

2. Basic VLSI Design Prinicples and Applications by Pucknell & Eshraghian.

3. Design and Analysis of VLSI Circuits by Glasser & Dobberpuhl.

4. Introduction to NMOS and CMOS VLSI Systems Design by Amar Mukherjee.

5. VLSI Engineering by Dillinger.

OBJECTIVE:

The domain of the Integrated Circuit Designer stretches from realms of device physics and Nonlinear Circuit Theory to the regime of digital systems microarchitecture. The field plays a central role in VLSI technology and encompasses multiple levels of abstraction: such as electrostatics, topology, switching theory, design methodology, and testing procedures, etc. It is the challenge of the VLSI Designer to transcend these disciplines and successfully transform an idea into the detailed specification for a manufacturable system chip. The main goal in this course is to generate a set of system MASKS for a chip on a computer tape, which would be converted into actual MASKS by a foundry. The Chip will then be fabricated at MOSIS and thereafter be tested at UMASS Lowell for its functionality. (ED credit 100%)

GRADING CRITERION:

Homework.....	10%
Project.....	30%
Mid-Term Examination.....	30%
Final Examination.....	30%

LECTURE	SUBJECT MATTER
S07	CMOS logic, the NAND gate, the NOR gate, Compound gates, Transmission gate, Tristate, Multiplexers, Inverters, Latches and Flip-Flops, Layout and Design Rules, Gate Layout, Circuit Design and Standard cells, Area Estimation and MIPS architecture.
S14	MOS Transistor Theory, Ideal I-V Characteristics, Simple MOS Capacitance Models, Gate and Diffusion Capacitances, Secondary effects such as velocity saturation and mobility degradation, channel length modification, body effect, junction leakage and geometry dependence, Beta ratio effects, Noise Margins and Switch level RC Models.
S21	Circuit Characterization and Performance Estimation with RC Delay models, Parasitic Delay, Transistor Sizing, delay in Multistage Logic Networks, Optimum number of stages, power dissipation, Interconnect Resistance and Capacitance, Delay, inductance, width and spacing, Repeaters, Design Margin, Reliability, Soft errors and Scaling.
S28	Circuit Simulation with Sources and Passive Components, Transistor DC Analysis, Inverter Transient Analysis, Optimization, Device Models, I-V Characteristics and Threshold voltage, Circuit Characterization, Path Simulation, Monte Carlo and Interconnect Simulation.
O05	Combination Circuit Design with static CMOS, Cascode Voltage Switch Logics, Dynamic Circuits, Pass Transistor Circuits, CMOS with Transmission Gates, Circuit pitfalls such as threshold voltage drop, leakage charge sharing, Power Supply Noise, Minority Carrier Injection, Hot Spots, Process Sensitivity. Sense Amplifier Circuits and Low Power Logic Design.

O19 Sequential Circuit Design with methodologies and constraints, Clock Skew, Latch and Flip-Flops, Pulsed Latches, Klass Semidynamic Flip-Flops, 2-φ Design, Dynamic Circuits and Skew Tolerant Domino Circuits, State-to-domino Interference, Synchronizers and Arbiters and Wave Piping.

O26 Mid-Term Examination

N2 Design Methodology and Tools along with strategies, Hierarchy, Regularity, Modularity, Locality, Microprocessor/DSP, Cell Based Design, Full Custom Design, Design Ergonomics with Prototype Costs, Schedule, and Design Reuse and Documentation. ASIC and Micro architecture, Layout Guidelines, Design Exchange Format and Optimization.

N09 Testing and Verification along with Debugging Test Fixtures, Test Benches, Fault Models, Automatic Test Pattern Generation, Ad-hoc Testing, Scan Design, Built in Self-Test TAP Controller, Instruction and Test Data Registers, SOC testing and Mixed Signal Testing.

N16 Data Path Subsystems along with Addition/Subtraction, Carry Propagate Addition, Manchester Carry Adder, Carry look ahead adder, One/Zero detectors, Comparators, Binary Counters, Linear Feedback Shift Registers, XOR/XNOR form, Shifters, Multipliers, and Booth Encoding, Wallace Tree Multiplication and Parallel-Prefix Computations.

N23 Array Subsystems along with SRAM, Read/Write Operation, Bitline Conditioning, DRAMs and Register files, Subarray Architecture, ROMs, PROMs and NAND ROMs, Shift Registers Content addressable Memory, PLAs, Array yield, Reliability and Self Test.

N30 Special Purpose Subsystems along with packaging, Heat Dissipation, Power Distribution, IR Drops, Inductive Noise and Bypass

Capacitance, Power Network Modeling, I/O Pads, Clock Subsystem Architecture, Global Clock Distribution, Clock Skew Budgets.

D07 MOS Small Signal Model, Common Source Amplifier, The MOS Inverter as an amplifier, Current Mirrors, Differential Pairs, D-to-A and A-to-D Converters, and Radio Frequency Circuits.

D14 Introduction to Verilog and VHDL Overview.

FINAL EXAMINATION WILL BE GIVEN AS PER UNIVERSITY SCHEDULE

UNIVERSITY OF MASSACHUSETTS LOWELL
James B. Francis College of Engineering
Department of Electrical & Computer Engineering

Dr. Kanti Prasad 16.504 VLSI Fabrication Spring 2006

Text: VLSI Technology by S.M. Sze, McGraw-Hill.

References:

1. Semiconductor Integrated Circuit Processing Technology by Runyan & Bean, Addison Wesley.
2. Microelectronic Processing by W. Scot Ruska, McGraw-Hill
3. VLSI Fabrication Principles by Sorab Ghandhi, Prentice-Hall.

Objective:
The domain of the VLSI Fabrication Engineer stretches from realms of device physics and nonlinear circuit theory to the regime of digital system micro-architecture. The main goal of the course is to embody all the essential steps of fabrication technology, as how to transfer the MASK (designed in 16.469 VLSI course, or provided by NIST) onto the silicon chip. The course, therefore, includes a comprehensive description of the processes such as diffusion, oxidation, photolithography, aligning, etching, implantation and metallization. The topics such as single silicon crystal growth, poly-silicon deposition, slicing the silicon boule into wafers, dicing the wafers into chips, bonding the chips and finally package the tested chips. The testing and measurements are covered at great length using equipment such as microscopes, ellipsometers, four probe-resistivity, Dektak, surface profiler, I-V curve tracer and C-V bridge.

DSIPL-VLSI Fabrication Laboratory:
Each student will be responsible for transferring MASKS set (provided by National Institute of Standards & Technology (NIST)) onto the Silicon Wafer. During the process, students will carryout detailed processing and testing at each stage and finally characterization of the device, making full use of the DSIPL.

Grading Criterion:
Homework…….....10%
Laboratory Work.....…….....30%
Midterm Examination.....…….....30%
Final Examination.....……30%

LECTURE	SUBJECT MATTER
J24	Silicon structure; bonding; hybridization, Miller-indices. Density of silicon atoms concentration along various planes. Wafer preparation, Czochralski method. Sequential techniques in microelectronic processing, testing and packaging, yield and the clean room environment.
J31	The band theory of conduction, doping and p-n junctions, deep level impurities. MOS structures, applications of semiconductor properties; crystalline semiconductors. Crystal defects, an elemental semiconductor (silicon), and a compound semiconductor (Ga-As).
F07	Derivation of laws of diffusion including Fick's first and second law. Diffusion in a semiconductor crystal and mechanics of diffusion. Application of the diffusion equations, dopants and dopant sources including Boron and Phosphorus.
F14	Oxidation of silicon; kinetics of oxidation. Implications of the oxidation mechanism, and oxidation behavior in MOS devices. Introduction of photolithography process; negative and positive photoresist, development, and stripping.
F28	Photoresist chemistry and its applications; surface preparation, photolithography process control. The formation of images, limits on image reproduction, and the modulation transfer function. Dimensional control, pattern alignment, contact printing, UV and X-ray and electron-beam photolithography.
M07	Wet chemical and dry etching; etching of multiple layers, rate and time; factors governing etch rates, chemical safety. Chemical etchants; etching thermal SiO2 with HF acid. Etching of CVD SiO2; etching of silicon nitride and aluminum.
M21	Plasma etching, and plasma etchants; photoresist removal and lift-off processing. Vacuum science and technology. Sources for vacuum deposition, deposition by evaporation and sputtering.

M28 MID-TERM EXAMINATION

A04 Metallization for conductors; metals, silicides. Schottky diode and its fabrication, process control for vacuum deposition. Chemical vapor deposition, transport of reactants to the surface, reactors for the CVD and reduced pressure CVD.

A11 CVD applications, vapor phase epitaxy, doping and autodoping, molecular beam epitaxy, and CVD process control. The ion implantation. Ion implantation for substrate doping, and elements for ion beam processing.

A18 Implant damage and annealing, masking for implantation and related effects; and control of implantation processes. Fabrication of a bipolar transistor. Construction of a bipolar transistor along with base, emitter and collector.

A25 Metallization, Passivation, alternate thin film processes, multilayer metallization and bipolar processing. Fundamentals of Physical Vapor deposition & optimization. Electromigration and multilevel structures.

My02 Assembly techniques and packing of VLSI devices, Rent's role, packaging design considerations. Electrical and thermal considerations in packaging, mechanical design considerations. VLSI assembly technique, including die interconnection, eutectic die bonding & wire bonding. Package fabrication technologies including ceramic glass-sealed refractory and plastic molding under a variety of assembly environment.

My09 Mechanisms of yield loss in VLSI, processing defects modeling of uniform density of point defects. Simple non-uniform distributions such as delta, triangular and rectangular, multiple types of defects, radial distribution of defects. Reliability requirements for VLSI, cumulative distribution function (cdf), probability density function (pdf), reliability function and failure rate mean time to failure (MTTF) analysis. Common distribution functions such as Weibull, exponential and log-normal, accelerated testing including temperature voltage and current acceleration.

FINAL EXAM WILL BE GIVEN AS PER UNIVERSITY SCHEDULE.