QPSK Modulator: A Design Example for EET

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Abstract
Quaternary Phase Shift Keying (QPSK) is a fundamental method of encoding digital data in the phase of an analog carrier. This technique was used by early modems using the public telephone network. While the technology is no longer economically valid, the components of the modem span the coursework of most EET curricula; i.e. both analog and digital circuits, within a communications framework.

A directed design project approach was used. The instructor defined the objectives of the project, and directed the sequence and tools used in the design. The class was given a QPSK modulator constructed from TTL 7400 series gates and 741 op amps. From this circuit, the students had to identify parts and create a schematic. The linear circuits included an oscillator and a band pass filter, and both were analyzed using PSpice. The digital circuits were split into combinational and sequential sections, and timing diagrams were developed. The digital circuits were then divided into sections suitable for implementation using programmable logic devices. The signal waveforms were observed in both the time- and frequency-domains, and the concept of bit rate vs. baud rate was introduced.

This design project was first implemented in a sequential digital circuits course, after the students had taken a linear circuits course, both at the junior level. For most students, this was their first exposure to mixed digital-linear circuits, and the first circuit that they had to reverse engineer. The directed design approach is used as a prelude to the senior design projects. While the circuit is straightforward, it serves to reinforce the students' knowledge of linear and digital circuits, their ability to analyze and design simple state machines, and their schematic capture and laboratory skills.

Introduction

A key tenet for engineering technology is hands-on experiential learning. For Electrical Engineering Technology (EET), this most often translates into building, testing, and troubleshooting electronic circuits. Most commercial designs are mixed analog and digital circuits. For our curriculum linear and digital circuits are covered in separate courses. This means that portions of the digital circuits class must be combined with previously studied analog op amp circuitry. The design example described here is a modem, which is then covered in a later class in digital communications.

The goal of this project is to incorporate analog and digital circuit elements in a practical design that mimics a commercial device. Most students at least know that a modem is used between a computer and the Internet. From this fundamental knowledge, a modulator can be built using circuits already covered in the junior year. This design can be simulated using PSpice and Altera

MAX+PLUS II software, with these two modeling programs providing complementary views. The circuit can also be assembled in the lab and tested using conventional test instruments. In both cases, the students can verify the bandwidth requirements for transmitting an input data stream.

Overview of Phase Shift Keying

The Public Telephone Network (PTN)[1] is a well-established and characterized analog transmission system. The existence of the PTN to nearly every home and business made it an obvious first choice for data transfer between computers. However, to transmit and receive digital data on an analog line requires a modulator/ demodulator pair, or modem. For the modulator portion, the input is a digital bit stream, with appropriate control and header bits. The modulator output is a sinusoid, with a frequency within the 300 – 3300 Hz pass band of the PTN. The receiver is the obvious counterpart.

As in general communications systems, a modem can encode data on a sinusoid by modulating its amplitude, frequency, phase, or a combination of these three attributes. Phase Shift Keying (PSK) is the name given to the technique of encoding a digital bit in the phase of a constant-amplitude, fixed-frequency sine wave. Binary PSK describes systems where one bit selects one of two phases. Quaternary PSK (QPSK) relies on two bits (a dibit) to select 1-of-4 phase angles. This process can be extended to include 8-PSK and 16-PSK, where 3 or 4 bits are grouped to select 1-of-8 or 1-of-16 phase angles[1].

We can expand the discussion of QPSK by using Table 1. For a half-duplex modem, the entire transmission line bandwidth is dedicated to one channel, and the carrier frequency, f_c, is set to 1800 Hz, the pass band center. The serial bit stream is "read" two bits at a time, with each dibit selecting a unique phase angle. This can be re-stated by claiming that QPSK has 2 bits/baud, where a baud is a change on the analog output. It is the baud rate that determines the bandwidth required for transmission.

Table 1: QPSK Modulated Waveforms

2-bits	Analog waveform
00	$A\sin(2\pi f_c t + 0°)$
01	$A\sin(2\pi f_c t + 90°)$
10	$A\sin(2\pi f_c t + 270°)$
11	$A\sin(2\pi f_c t + 180°)$

The bandwidth required to transmit a quaternary phase shift keyed signal is $f_c \pm f_b/4$, where f_b is the input data rate. By associating two bits with each baud, the data throughput is doubled for a given bandwidth. Getting the most bits through a given channel bandwidth is the driving force for modem revisions in all communications systems.

The design example presented here includes a digital portion used to create the serial bit stream through the 1-of-4 phase angle selection. A separate analog section is presented which contains a band pass circuit, generating an output suitable for spectrum analysis.

Relevance to EET program

The junior level curriculum at WCU includes a course in digital electronics, covering sequential and combinational circuits. While some lab work is done with TTL devices, many of the labs are performed using the Altera MAX+PLUS II software, and the Complex Programmable Logic

Devices (CPLD) on the Altera UP-1 prototyping board. Schematic entry is used with many of the combinational circuits, while the VHSIC Hardware Description Language (VHDL) is presented as sequential circuits are studied[2]. Several authors have described this methodology for digital labs[3,4,5].

Students have had op amps circuits in their sophomore years, using a conventional textbook[6] and doing simple one and two chip labs. PSpice analysis of operating points and frequency effects is known.

The QPSK system is typically the first system studied by the students, where they are expected to interface digital and analog circuits. While each component circuit has been previously studied, the interrelationships, both in the lab and in the simulation software, are now the important areas of study.

For most students, a digital communications course follows this digital course. Modems are studied in that class as systems, with the mathematical analysis including Fourier series. This later abstract presentation now has a practical foundation due to this design project.

QPSK Modulator System

The overall system is shown in Figure 1. Two inputs are required, the byte of digital data, along with a data clock. The system output is the analog phase shift keyed sinusoidal waveform. The five functional blocks were selected mostly to facilitate incorporation into lab exercises and the modeling software.

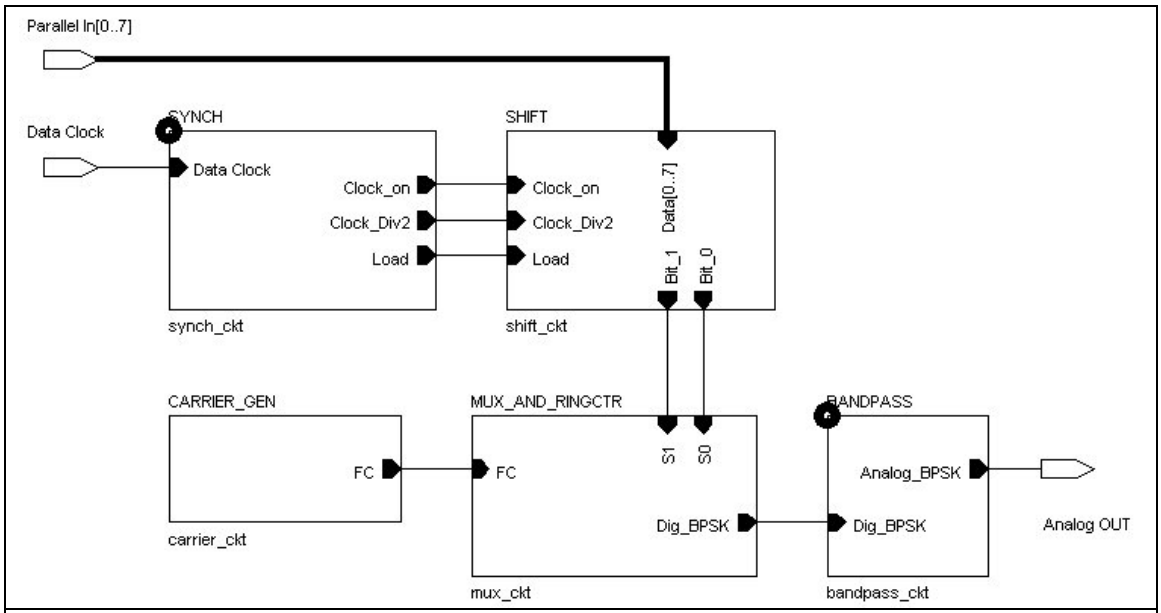

Figure 1. QPSK Modulator System

Digital Circuitry

The fundamental circuitry for the QPSK modulator is shown in Figure 2, and is the block labeled MUX_AND_RINGCTR in Figure 1.

A 4-bit ring oscillator is initially loaded with "1100". The four Q-outputs each produce a 50% duty cycle waveform, at a frequency one-fourth of the internal carrier clock (7200 Hz, in this case). In addition, the Q-outputs provide four waveforms, with the required 90-, 180-, and 270-degree phase shifts. These four Q-outputs are then used as inputs to a 4-to-1 multiplexer. One of the four inputs is selected by the two bits D1 and D0.

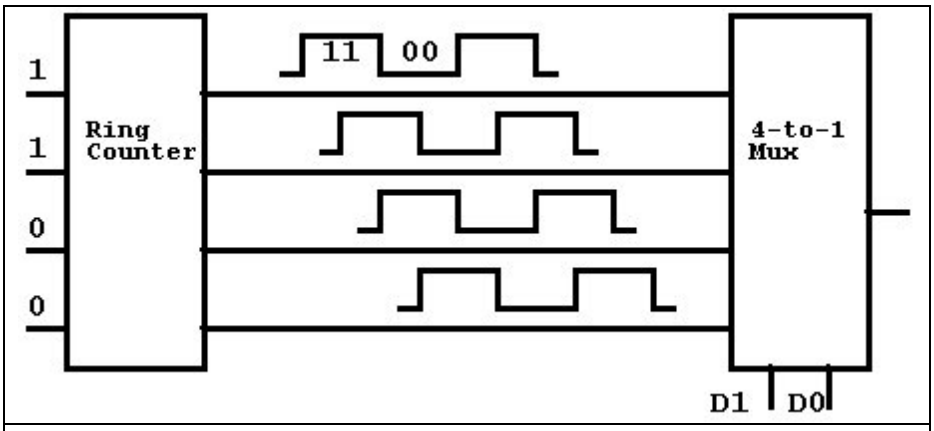

Figure 2. QPSK Basic Circuit

This block is easily implemented using TTL chips in the lab. Both PSpice (Figure 3) and Altera MAX+PLUS II (Figure 4) can model this circuit and provide timing plots.

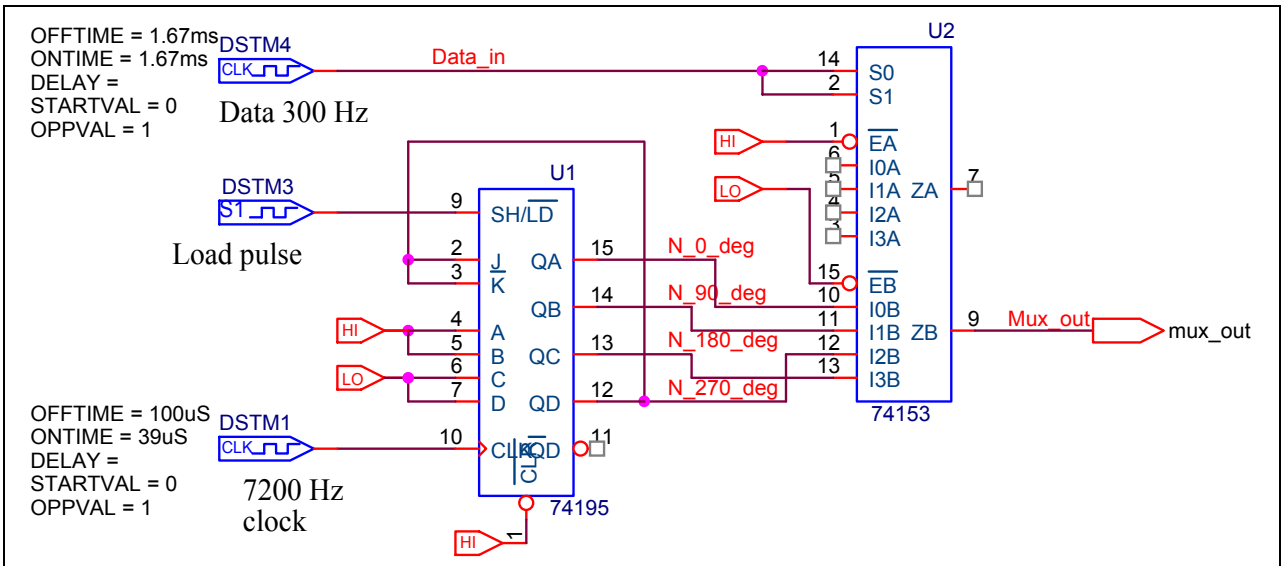

Figure 3. PSpice schematic for ring oscillator and multiplexer.

```
-- qpskpart1.vhd
-- First circuit for QPSK modulator: contains 4:1 mux, ring counter, and 2-bit counter for mux select.

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY qpskpart1 IS
        PORT(   carrier_clk     : IN            STD_LOGIC;
                data_clk        : IN            STD_LOGIC;
                mux_out         : OUT           STD_LOGIC;
                q               : BUFFER        STD_LOGIC_VECTOR(3 downto 0));
END qpskpart1;

ARCHITECTURE part1 of qpskpart1 IS
        SIGNAL d : STD_LOGIC_VECTOR(3 downto 0); -- these are internal to the chip
        SIGNAL s : INTEGER RANGE 0 to 3;
BEGIN
        PROCESS (carrier_clk, data_clk)  -- if either clock changes, then execute this loop
                VARIABLE count : INTEGER RANGE 0 to 3;  -- this is local variable for
PROCESS only
        BEGIN
                -- Define a 4-bit D flip-flop for shift register
                IF (carrier_clk 'EVENT and carrier_clk = '1') THEN
                        q <= d;
                ELSE
                        q <= q;
                END IF;
                -- two bit counter for mux select
                IF (data_clk 'EVENT and data_clk = '1') THEN
                        count := count +1;
                END IF;
                s <= count;
        END PROCESS;

-- D flip flop section to create 50% duty cycle with ring counter
        d <=    "0110" WHEN (q = "1100") ELSE
                        "0011" WHEN (q = "0110") ELSE
                        "1001" WHEN (q = "0011") ELSE
                        "1100" WHEN (q = "1001") ELSE
                        "1100";
-- mux section
        mux_out <=      q(0) WHEN (s = 0 ) ELSE
                        q(1) WHEN (s = 1 ) ELSE
                        q(2) WHEN (s = 2 ) ELSE
                        q(3) WHEN (s = 3 ) ELSE
                        '1';
END part1;
```

Figure 4. VHDL file for Multiplexer

The next requisite digital block is labeled SHIFT in Figure 1. Its major function is to take an 8-bit byte (in parallel) and serially shift out two bits at a time. The two output bits are the dibit presented to the multiplexer in Figure 3 above. The 8-bit wide shift register is clocked at the

(input) data rate, and is a conventional parallel-in-serial-out (PISO) circuit, either implemented in TTL or VHDL. A two-bit holding register is constructed to capture and hold the dibits. The dibits are presented to the multiplexer at half the input data rate. It is this data rate divided by two that determines the baud rate.

The third digital circuit is used to derive the data clock/2, and the synchronizations signals for re-loading the PISO, and for latching data into the two-bit register. This circuitry is in the block labeled SYNCH in Figure 1.

Analog Circuits

Two analog circuit blocks are defined, and both can be analyzed using PSpice. The first is the carrier clock generation circuit, where a 555 Timer is used to generate a 7200 Hz pulse train. The final band pass circuit is centered at 1800 Hz, and is implemented using 741 op amps.

PSpice student version 9.2 has a model for the 555 Timer, and time domain analyses can be performed to design and verify a working circuit. This circuit is described in most linear circuits textbooks, and standard designs are readily available[6,7]. The duty cycle of the waveform is not important for this application, only the frequency.

The student version of PSpice limits the number of components that can be analyzed. Consequently, a fairly simple band pass circuit is modeled. This is adequate to view the band pass frequencies for the circuitry, and the resulting impact on the square wave coming from the multiplexer. The Fourier Transform function in PSpice is a useful tool in this analysis. Figure 5 shows the schematic for the filter used, which consists of a two-pole low pass filter (f_2 = 3300 Hz) cascaded with a two-pole high pass filter (f_1 = 300 Hz).

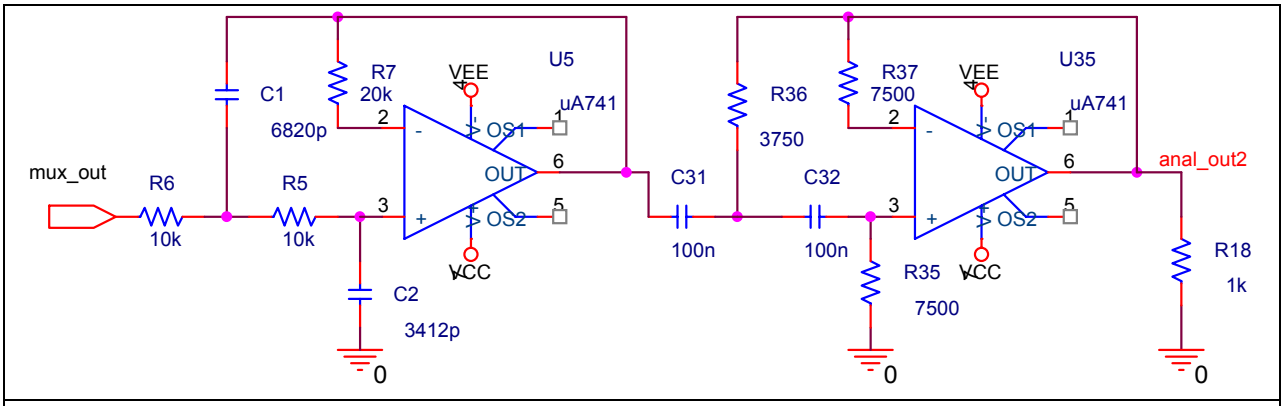

Figure 5. Band pass filter schematic.

Implementation Results

By using a simple band pass circuit in PSpice, the multiplexer circuit from Figure 3 can be added to the band pass circuit of Figure 5 without exceeding the component limit. An inspection of Table 1 will reveal that the maximum phase change occurs for a binary data input of "1100".

This input will cause the output to shift by 180 degrees, at the baud rate. In Figure 6, the phase of the digital output of the multiplexer, MUX_OUT, can be seen to change each time the DATA_IN signal changes. In this simulation, the input data rate is 600 bits per second, and multiple cycles of the phase-shifted carrier are visible for each input dibit (11 or 00).

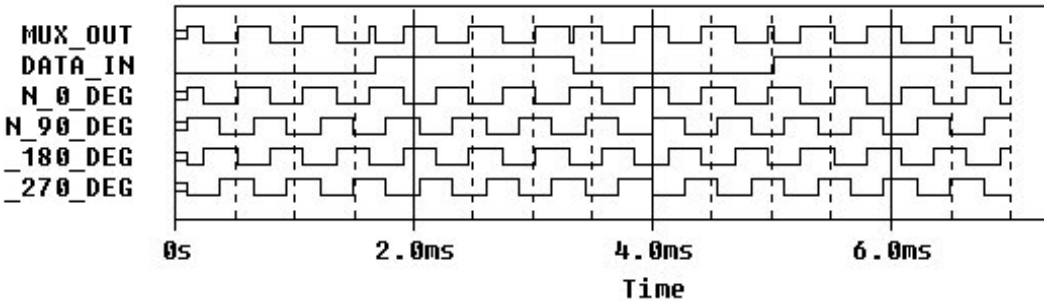

Figure 6. PSpice output showing phase shifted square waves.

This digital output becomes the input to the band pass circuit. Figure 7 shows the same digital input and the corresponding analog output. Again, the output phase is seen to change each time the input changes. Even a two-pole filter has substantially enhanced the sinusoidal nature of the output, so that it looks like a conventional analog waveform.

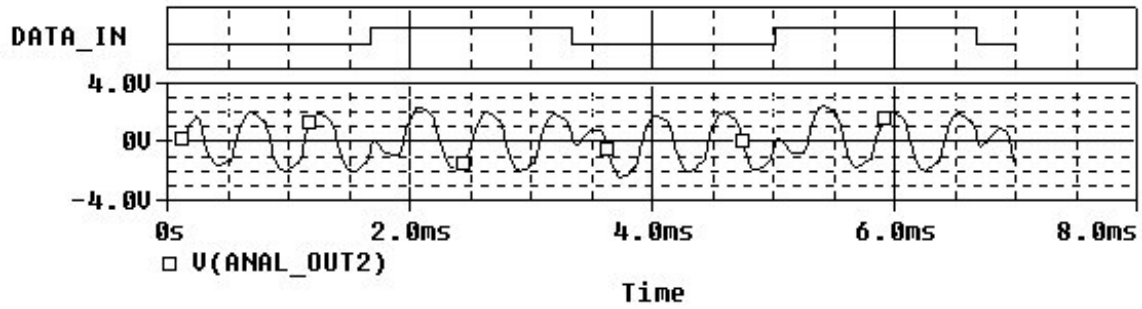

Figure 7. Analog output from the Band Pass Filter.

Using the built-in PSpice Fourier transform function, the spectral analysis of the analog output is computed and presented in Figure 8. The students can observe the bandwidth of the transmitted output (300 Hz, in this example), and can then investigate the bandwidth requirements as the data rate changes. This concept is fundamental for modems and much of digital communications.

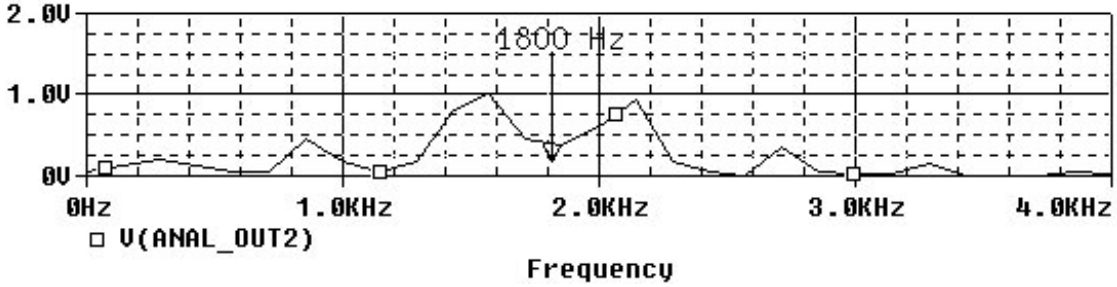

Figure 8. Fourier Transform of the Analog QPSK output.

This circuit can be built using op amps and TTL devices. Using an oscilloscope, the phase changes can be observed, verifying operation. Careful adjustment of data rates may be necessary to synchronize the image on the scope. More importantly, a spectrum analyzer can be used to experimentally observe the bandwidth change as the data rate is varied.

The complete digital portion can be implemented using VHDL in MAX+PLUS II from Altera. In the lab, the design is compiled and downloaded to the EPM7128SLC84-7 CPLD. The two clocks required for this circuit are available with this CPLD. This arrangement allows the students to again use an oscilloscope and a spectrum analyzer to verify operation.

The simulator in MAX+PLUS II is very useful in presenting results from the various sections of the digital design. Figure 9 contains the simulation output that shows the output phase changes as the dibits change from 00 to 01 to 11 to 10 as the byte B4H is shifted out. The "behind-the-scenes" waveforms that are created and selected to effect the changes are included. A comparison of Figure 6 (PSpice) and Figure 9 (MAX+PLUS II) shows the complementary simulations available to the student.

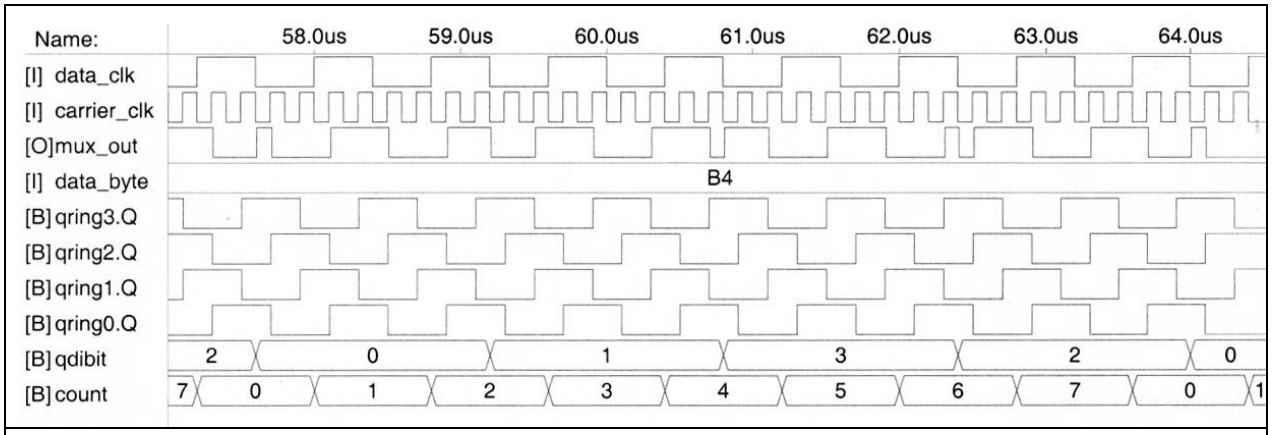

Figure 9. MAX+PLUS II Simulation Output.

Discussion

This design project was developed to incorporate linear and digital circuits in a practical design. While it can be questioned if a QPSK modulator is practical, most students are familiar with the basic concepts of a modem, including the inputs and outputs. For most students, this is the first analog-digital system studied. As such, it is useful before students take a digital communications course, which is primarily a systems course.

Expected outcomes from the design project can be summarized under knowledge, skills, and abilities. It is expected that a student completing this project will have knowledge of the time-domain and frequency domain characteristics of digital signals, when and how to use combinational and sequential logic, the design and behavior of counters, shift registers, and programmable logic devices, and Fourier series analysis in relation to linear circuits. The student will be able to design and analyze active filters using op amp circuits, design and analyze simple state machines, and identify timing requirements.

The related skills expected include the logical design of a schematic, the use of PSpice as a linear circuit analysis tool, the use of the Altera MAX+PLUS II software with VHDL entry, as well as the conventional building and troubleshooting of a multi-chip circuit.

Conclusion

A QPSK modulator is a useful design project, incorporating both digital and analog circuits commonly studied by third year EET students. It adequately serves as a first system to be assembled, as it can be modeled using the tools routinely available, and tested using traditional laboratory test instruments. The subsystems can be built and tested separately. The choice of a digital communication circuit also helps to integrate the subject matter of three separate courses. This multi-week project also serves as a directed design project, and as such is an excellent precursor for the senior project courses. The knowledge, skills, and abilities expected of EET students are enhanced by this project, and weaknesses can be identified before the student attempts an independent project.

References

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