2006-2524: LABORATORY FOR DIGITAL ELECTRONICS

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Laboratory for Digital Electronics

Abstract

The Digital Electronics course (ECE 3500)[1] was created in the Department of Electrical and Computer Engineering of Western Michigan University to develop the skills students need to design, and simulate digital integrated circuits down to the transistor layout level using Mentor Graphics Category II tools[2]. Digital Electronics is a required course for students majoring in computer engineering. The class has an embedded lab which makes use of the 0.25 micron technology for IC implementations (0.25-micron Design Kit by MIT). In order to pass the course students need to pass the embedded lab as well. Students work with the Mentor Graphics Electronic Design Automation (EDA) tools to design and simulate their circuits. The tools used are as follows: IC Flow (Design Architect and IC Station), Analog and Mixed Signal Design (AMS-ELDO Simulator and Xelga Viewer) and Calibre (Design Rules Check (DRC), Layout Versus Schematics Check (LVS), and Parasitic Extraction).

The focus in the course is primarily on designing digital circuits. Topics include CMOS transistor models, static and dynamic CMOS gate styles, CMOS logic function blocks, sequential circuits, timing issues, memory and array structures, and interconnect parasitics. The embedded lab provides a hands-on approach of applying the concepts taught in the class. Students are required to create CMOS transistor-level designs, perform function tests along with timing analysis and create layouts for their circuits. The designs must pass the DRC and LVS checks. The final step in verifying the performance of the designs is the parasitic extraction in each lab. The best two designs with respect to the shortest circuit delays and the smallest layout areas are given bonus credit in each lab. Lab experiments include the design of inverter, basic logic gates, 2-input XOR gate, 1-bit full adder module, static SR flip-flop, two-bit synchronous counter, one-of-four multiplexer module, and 4bit x 1bit static RAM

In addition to the lab and class work (which includes homework assignments, midterm exam, and final exam) students develop two class projects (4-bit ALU unit and a dual 4x4-bit register bank). Students are required to give demonstration of each project to the instructor to get full credit for the projects. A 100-page Tutorial on using the Mentor Graphics tools is available on the class Web Page to help students. Various useful topics regarding the projects and the labs are also provided on the class Web Page.

In the first part of the paper, we will summarize the outline and summary of the class. The second part of the paper will focus on the class projects and laboratory work in detail. The third part of the paper will focus on the assessments used for the class and future developments planned based upon the assessment and comments provided by the students.

Introduction

The Digital Electronics course and the Digital Electronics Laboratory have been developed in the Department of Electrical and Computer Engineering Department such that its main emphasis is on the various aspects of designing and simulating digital integrated circuits by taking a bottom-

up approach (staring at the transistor level). This course is a 4 credit hour course with 3 hours of lecture per week and a 3-hour lab session per week. The lab makes up 20% of the course grade and students are required to pass the lab in order to pass the course. The course is offered only in the Spring Semester. Apart from the laboratory assignments the course work also comprises of homework assignments, lab projects, and exams.

Class Work

There are three one-hour lectures per week. The in-class lecture sessions cover for topics as follows: Overview of CMOS transistor models, CMOS inverter, CMOS gate styles, CMOS logic function blocks, Sequential circuits and timing issues, memory and array structures and interconnects.

The lecture sessions also include a brief explanation of the next week lab to be performed, as well as hints on how to approach the lab problems, and the ways of carrying out the Prelab assignments. All of that information is posted and updated every week on the Class Web Page. The Web Page is the main source of information for the class.

There is a required textbook for the course: "*Digital Integrated Circuits* by Jan M.Rabaey[3]. The textbook, the Instructor's Lecture Notes and the Mentor Graphics Tutorial available on the Class Web Page are the main sources of information for the class. It also contains information about the weekly labs, prelabs, weekly lectures, homework assignments and solutions to the homework assignments, etc.

The most important and handy section of the Class Web Page is the Tutorials section which provides detailed information and step-by-step procedures on how to work with the various modules of the Mentor Graphics tools. They cover for the following tools: Design Architect, Eldo simulator and Xelga viewer, IC station and Calibre. The Tutorials have been developed by the authors of this paper.

Class work also includes about 10 homework assignments that are typically due the following week. Most of the homework assignments include real world applications as well as mathematical calculations to achieve the required timing details, and Mentor Graphics simulations to verify the results. Students are expected to give a detailed explanation of their procedures to solve the problem. The assignments define problems that are either analytical in nature to practice with the theory segment of the class, or they refer to particular circuit types that are not included in the lab assignments.

Students are required to take a midterm exam and a final exam that test the students' ability of problem solving. The two exams in total comprise of 50% of the course grade.

Lab Work

Most major topics covered in class are also practiced in the lab. The lab sessions provide a hands-on approach and yield a good understanding of the operation and characteristics of digital circuits. The lab meets every week for a 3-hour session during the Spring semester. All labs are single session but the introductory lab (Lab1) and Lab2 which are two-session labs.

At present the laboratory configuration is made up of 8 Unix workstations (Figure 1). Students typically work in groups of two throughout the semester. Each Unix workstation has access to the Mentor Graphics Electronic Design Automation tools[2]. These workstations are available in the general computing lab so that students can access the software anytime through out the semester. Different software modules include Design Architect (Figure 2) for design entry at the transistor-level, Eldo (SPICE-like) for simulation, Xelga (Figure 3) for wave viewer, IC station (Figure 4) for developing the IC layout and Calibre for performing DRC and LVS checks and back annotation.

Figure 1. SUN Workstations Lab

The basic functionality of the Mentor Graphics tools used in the lab is as given below.

Design Architect	→	Creates a schematic design using transistor models
ELDO Simulator		Generates a Spice netlist and simulates the design using the Spice netlist generated
Xelga Viewer	→	Used to view the simulation waveforms and to determine the signal transition times
IC Station	→	Used to create a CMOS layout out of the schematic design and to perform the Layout Vs. Schematic (LVS) check
Calibre Xrc	→	Used to generate the necessary parasitic resistor and capacitor values that are to be included in the CMOS layout of the schematic design for real-time simulations

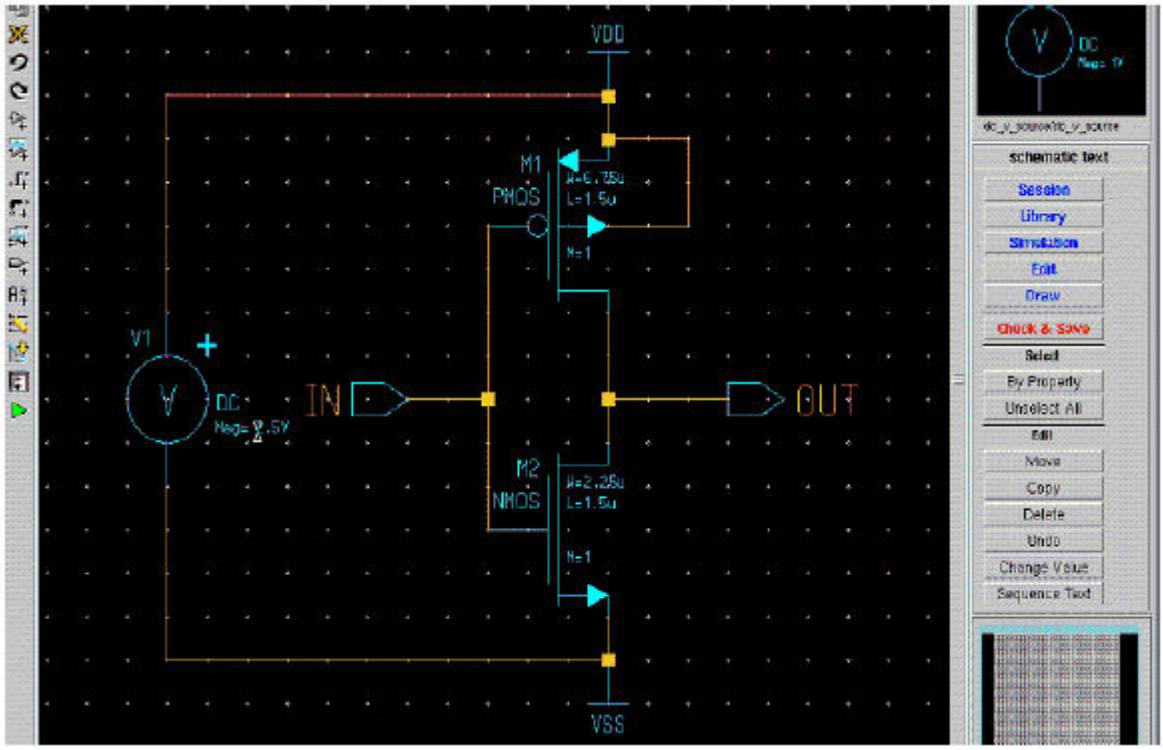

Figure 2. Schematic diagram for inverter in Design Architect

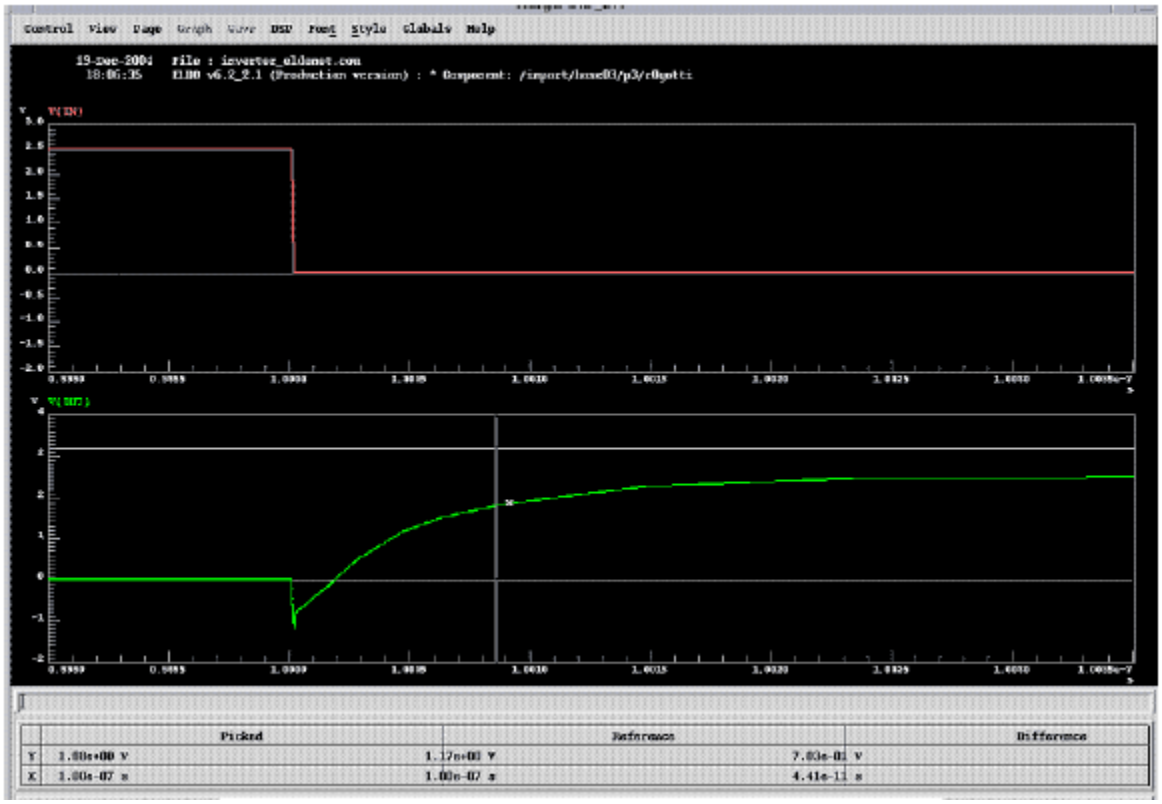

Figure 3. Verification of the dynamic behavior of inverter using Eldo along with Xelga

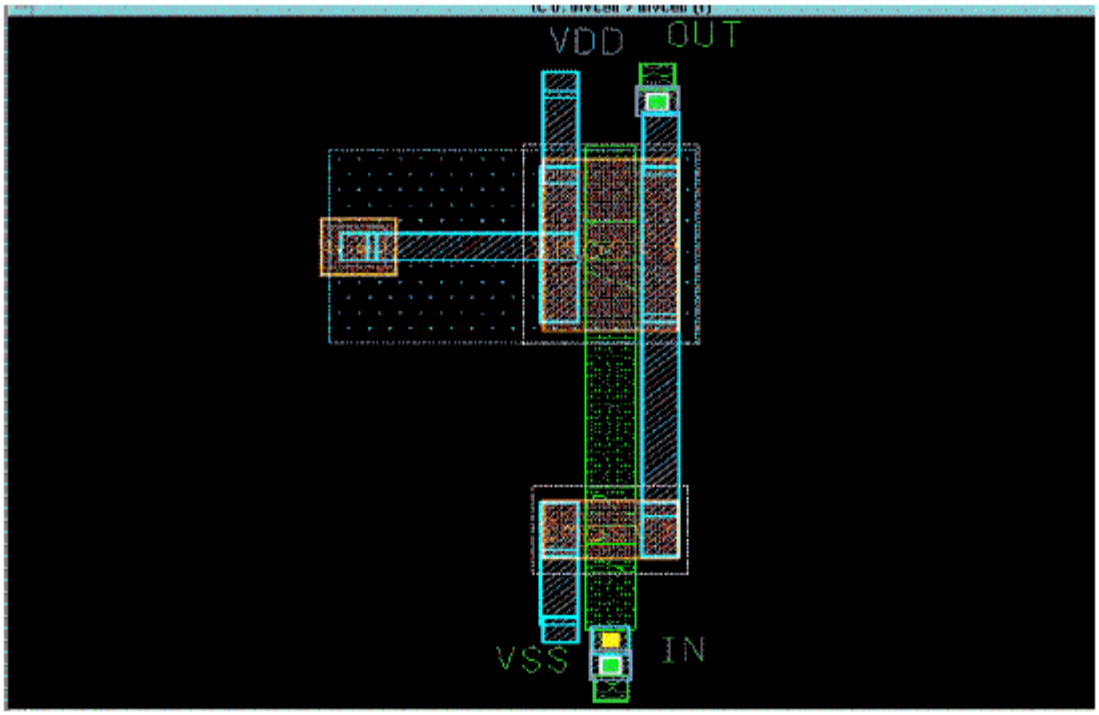

Figure 4. Layout design for inverter using IcStation

Each lab assignment is broken up into a prelab and a set of lab tasks. Students are required to submit their prelab at the beginning of the lab session every week. The prelab calls for a schematic diagram, transistor sizing and timing calculations to meet the specs for the lab. Students are required to turn in their Lab Reports after they have completed a lab session. The report consists of a detailed schematic diagram, timing calculations, simulation waveforms with low to high and high to low transition times, IC layout, DRC and LVS checks and parasitic extraction reports. Each lab is assigned a total of 12 points with 3 points for the prelab and 9 points for the lab.

The laboratory experiments are listed below:

Lab 1: Introductory Lab (Inverter Design)
Lab 2: Layout editing and performance analysis
Lab 3: Design of 2-Input XOR gate
Lab 4: Design of 1-bit full adder module
Lab 5: Design of one of four multiplexer module
Lab 6: Design of static SR flip flop
Lab 7: Design of 2-bit synchronous counter
Lab 8: Peripheral circuits for a 4-bit x 1-bit CMOS static RAM
Lab 9: Design of a Muller C-element

Lab1 is a two session lab which introduces all the software tools used in the lab. In this lab students develop an inverter as part of the lab work. During Session1 students learn the concepts of developing a CMOS design using Design Architect and the concepts of simulating the design

using ELDO (Analog and Mixed signal) simulator and finding low to high and high to low propagation delays using the Xelga viewer. During Session2 students learn the concepts of developing IC layout for a CMOS design, perform Design Rule Check (DRC), Layout Versus Schematic check (LVS) and then perform the parasitic extraction using Calibre.

Lab2 is also a two session lab to help students gain more hands on approach with the software tools being used in the lab. Students are supposed to enter the CMOS design provided to them in Design Architect, perform timing simulations and analyze the logic function of the CMOS circuit provided to them. Also students are supposed to develop IC layout, perform DRC, LVC checks and parasitic extraction. Main idea behind Lab2 is to make sure that students understand the fabrication processes for NMOS and PMOS transistors. In this lab students are introduced to the concept of developing symbols for the design and the layout developed so that the symbols can be used as part of more complex designs in the later labs.

Lab3 involves the design of a two input XOR gate. Starting from lab3 students are expected to develop the working design in their prelabs. The XOR gate should be implemented using complementary CMOS logic. Also the XOR gate should be designed with the minimum number of devices and with a relatively small layout area such that the design can be transformed into a symbol and can be used in later labs. Also students are supposed to come up with the W/L values for the transistors such that circuit will have equal rise and fall times. Starting from Lab3 the best design (less rise and fall times, less layout area and good parasitic capacitances) are given 2 points as bonus credit.

Lab4 involves the design of a 1-bit full adder module. Students are expected to develop a concise layout of a cell that implements sum and carry-out functions of a binary full adder. The 1-bit full adder module should be implemented using pass-transistor logic. Design developed using any other transistor logic will be given zero credit.

Lab5 involves the design of a one-of-four multiplexer module. Students are expected to design a combinational logic circuit module using dynamic np-CMOS technology. The idea of this lab is to study the properties of dynamic combinational logic circuits.

Lab6 involves the design of a static SR flip flop. Students are expected to develop a concise layout of a cell that implements a clocked CMOS 8-transistor SR flip flop. The cell structure should be developed in a neat and concise way such that it can be replicated for more complex designs such as register modules, etc.

Lab7 involves the design of a two bit synchronous counter. Students are expected to develop a concise layout of a module that implements a two-bit (modulo-4) synchronous up/down counter with parallel load and asynchronous clear. The counter should be based upon positive edge triggered D flip flops. The flip flops should be constructed using 6-transistor asynchronous CMOS SR latch cells.

Lab8 involves the design of peripheral circuits for a 4bit x 1bit CMOS static RAM. Focus will be given on the design of a single column segment of a 4bit x 4bit static CMOS register bank module. During Phase One students are expected to develop a concise SRAM cell, and make sure that read and write operations can be performed properly. In Phase Two students will layout

the column 0 of a 4 column register bank (RB) module. Necessary peripheral circuits will be added to the RB module and will be verified for the correct operation of the whole circuit. Modules to be developed as part of the Lab8 are as follows:

4 x 1 SRAM unit
Row-Address decoder
Pre-charge circuit
Sense Amplifier
Read/Write control circuit
1-bit temporary register
Three-State buffer

Lab9 involves the design of a Muller C-element using static CMOS technology. A Muller C-element is a key component to develop asynchronous, interlocked hand-shake type interfaces between complex, collaborating circuit modules rather than using a centrally-distributed clock signal to synchronize operations.

In addition to the lab experiments described above students are also required to complete two lab projects that make up 25% of the course grade (Project1 – 15%, Project2 – 10%). Project1 is about to design, simulate and layout of a 4-bit Arithmetic Logic Unit (ALU) that performs 8 basic functions. Students can use any design style they are familiar with. The Bonus Assignment to Project1 adds 8 more functions to the design. Project 2 is about to develop a static, dual 4x4bit Register Bank for a simple RISC processor. The Bonus Assignment for Project 2 calls for the integration of the 4-bit ALU with the register banks. The proper functioning of the new, integrated module should be proven by simulations.

The demonstration of the projects to the instructor is done at the simulation level, no actual circuits are fabricated. The specifications for the projects are essentially the same for one year to next but the chances for cheating are relatively slim. The project files are huge and the accounts are purged after the assignments are completed.

Assessment

The assessment[4] of the course and the lab have resulted in a good, positive response from the students on the overall quality of the class and also on the experiments done in the lab. Assessment questions were selected in a way such that the instructor's teaching effectiveness, subject quality as well as the student's ability and level of confidence after the class are assessed. Some of the assessment questions that were given to students with respect to the quality of the class/lab are listed below.

a. Rate the instructor's overall teaching effectiveness
b. Rate the overall quality of this course
c. Was the grading system for the course explained
d. The instructor seemed well prepared for the class
e. The instructor promoted an atmosphere conductive to work and learning
f. Was there agreement between announced course objectives and what was taught?
g. How well did examination questions reflect content and emphasis of the course?

The results of the assessments are shown in Figures 5 (a) and (b), respectively. Score 5 is the highest one.

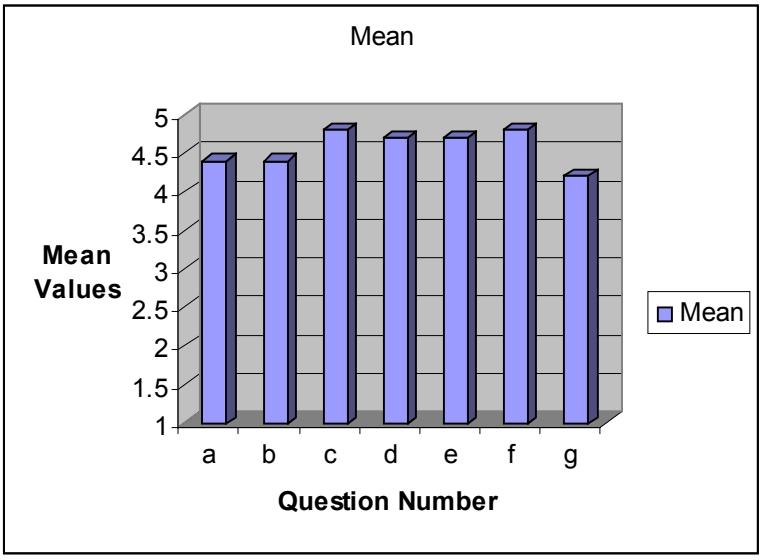

Figure 5 (a). Mean values of assessment questions

a. How much have you learned in this course?
b. Did the course improve your understanding of concepts and principles in this field?
c. Did you improve your ability to communicate clearly about this subject?
d. For this course rate the importance of simulation and thinking
e. Did you improve your ability to solve real problems in this field?
f. I gained skill during this course to help me learn independently
g. This course broadened my perspective of working in a global/societal context
h. This course helped me to fulfill some of my personal goals

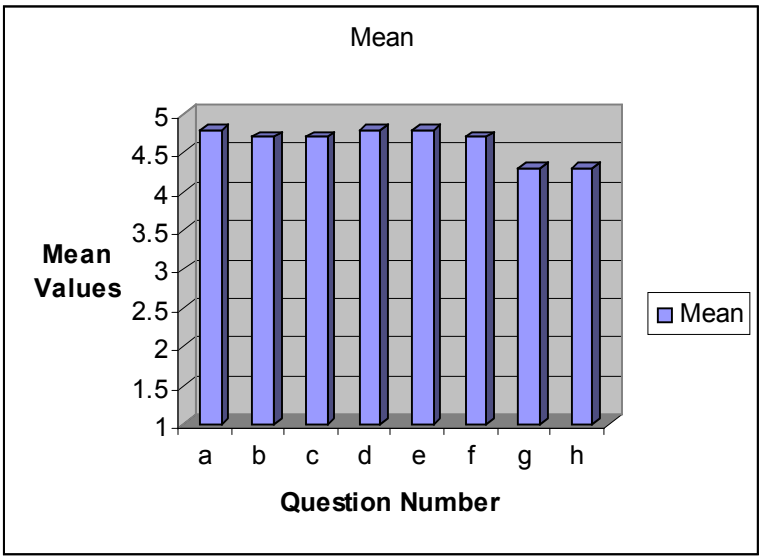

Figure 5 (b). Mean values of assessment questions

Conclusion and Future Work

This lab is kind of unique in the ECE curriculum in the US in the sense that it gives the students a very detailed experience from transistor-level digital circuit design to layout design and verification by simulation both at the functional and the layout level. Students are required to work on all the necessary steps for a given digital circuit but the creation of the layout structures for the individual transistors that are automatically generated by the tools. In most comparable courses student are given readily available solutions to design problems and they are only required to make small revisions and then verify the results. Another unique aspect of the lab is that it is based upon the 0.25-micron technology that is not too far off from what is actually being used by industry leaders. It has strategic importance for the US that graduates are exposed to industrial design tools and nearly cutting edge technology so they will possess a suitable skill level before entering the work force of leading US semiconductor companies.

The unstructured (anonymous) segment of the assessment indicates that some students need more help to familiarize with the use of the Mentor Graphics tools and they also like to have more attention by the lab instructor. We are planning to have two well-trained lab instructors in each lab section. In addition, we will extend the Tutorials to cover for recovery from various situations when the user has made some errors and can't continue the work.

The current competition for bonus credits rewards the smallest and fastest circuit designs. Since the Mentor tools support analysis of the power consumed, we would like to revise the bonus criteria such that it will favor minimum power consumption. It needs further work to devise a new, meaningful criteria set for that.

We would also like to develop a Control Unit as a library module that students can integrate with the ALU and Register Banks circuits. That would make possible to run programs on the core of this simple 4-bit RISC processor. It would provide a very satisfactory experience for the top students in the class.

A lot of domain knowledge and intellectual property have been invested in the course. They primarily manifest in the Tutorial that is more that 100 pages long and keeps on growing. The MIT Design Kit is essentially enables the use of the 0.25 micron technology but it doesn't give the know how to use the Mentor Graphics tools.

A potential adaptation of this lab by another ECE department is possible on the grounds that the interested parties can offer each other extra knowledge and experience that can be shared in a mutually beneficial way

References

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2. www.mentor.com
3. *Digital Integrated Circuits* by Jan M. Rabaey, Second Edition, Prentice-Hall, 2002,
4. The ICES Catalog, Division of Measurement and Evaluation, University of Illinois at Urbana-Champaign