A Custom Printed Circuit Board Differential Amplifier
For Instruction In
Undergraduate Analog Electronics

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Abstract

Instruction in the theory and operation of analog electronic circuits remains an essential element of contemporary electrical engineering curricula. While computer based simulation of these circuits is extremely helpful to mastery of essential topics, hardware implementation of these circuits in the undergraduate electronics laboratory best reinforces theoretical explanations and solidifies understanding. However, hardware reinforcement of more advanced topics such as component dependent frequency response, feedback and pole compensation is more difficult to achieve. Hardware circuits implemented by students will inevitably possess anomalies and errors which thwart the achievement of a laboratory's teaching objectives. After some years of development, we have found that a prepared custom differential amplifier presented on small custom printed circuit board (PCB) can greatly improve the undergraduate laboratory experience with advanced analog amplifier circuits. This circuit performs in a predictable, repeatable manner since correct component connections and biasing has been established and parasitic circuit elements are fixed. Components within the circuit remain accessible to test equipment so students may verify circuit condition. External components chosen by the student can be easily added to illustrate important behaviors. Furthermore, additional stages can be added to this circuit, presenting additional opportunities for student design. We fabricate these circuits in sufficient numbers that inevitable student mis-application of these PCBs is easily remedied. This paper discusses the objectives of instruction, theory of operation, implementation details, robustness and student experience related to this circuit. Sufficient detail is provided so that interested faculty may easily reproduce our design.

Introduction

Instruction in the theory and operation of analog electronic circuits remains an essential element of contemporary electrical engineering curricula. While computer based simulation of these circuits is extremely helpful to mastery of essential topics, hardware implementation of these circuits in the undergraduate electronics laboratory best reinforces theoretical explanations and solidifies understanding. However, hardware reinforcement of more advanced topics such as component dependent frequency response, feedback and pole compensation is more difficult to achieve. Hardware circuits

implemented by students will inevitably possess anomalies and errors which thwart the achievement of a laboratory's teaching objectives. After some years of development, we have found that a prepared custom differential amplifier presented on small custom printed circuit board (PCB) can greatly improve the undergraduate laboratory experience with advanced analog amplifier circuit concepts. In this paper, I present the pedagogical framework in which this amplifier is presented, details of the amplifier's design and operation, as well as information relevant to its fabrication and implementation.

Pedagogical Framework

The laboratory exercise which employs our printed circuit board (PCB) based amplifier is one of eight executed in our two semester required course sequence in electronics. Laboratory exercises are integrated with lecture and classroom exercises with the same faculty member responsible for both forms of instruction. Laboratory exercises throughout our curriculum follow a cycle of theoretical analysis or design followed by computer based simulation which are subsequently compared with hardware circuit performance. The first course in the electronics sequence, Electronics I (El Engr 321), covers semiconductor physics and the theory of operation of the junction diode, bipolar junction transistor (BJT) and metal-oxide-semiconductor field effect transistor (MOSFET). Circuits involving small numbers of these active devices are used to illustrate their operation and practical importance. Complementary hardware laboratory exercises reinforce the concepts of diode and transistor biasing as well as small and large signal operation. The second electronics course, Electronics II (El Engr 322), focuses upon multi-transistor circuits including differential amplifiers, feedback, stability, high current output stages and a variety of small and medium scale complementary MOSFET digital circuits. Our PCB based amplifier is an integral part of the second laboratory exercise of this second course.

The block of instruction supported by EE 322 Lab 2 presumes a theoretical understanding of direct coupled differential and single bipolar junction transistor amplifiers. It also presumes an understanding of the origin of circuit poles and the methods for estimating and simulating their effects. The block of instruction which Lab 2 supports begins with a formal study of analog feedback. Feedback circuit topologies, feedback circuit implementation, criteria for stability, stability analysis and methods for stability augmentation are presented. We also choose to include output stage operation and limitations in this block of instruction. The theory of operation of push-pull output stages includes signal swing limitations, methods for biasing, power dissipation considerations and frequency response.

The Laboratory Exercise

Within the pedagogical framework described above, we wished to create a laboratory exercise which would simultaneously illustrate both feedback and output stage concepts. The associated amplifier needed a differential input making it possible to reinforce the feedback concepts illustrated through operational amplifiers. The open loop gain of the amplifier needed to be low enough to be directly measured without saturation.

To illustrate the impact of pole compensation under feedback, the amplifier had to be designed inherently unstable at feedback factors near unity. Furthermore, the amplifier needed a common collector output stage through which output signal swing limitations under low resistance loads could be illustrated. The dc bias voltage of the output node needed to be adjustable across a range of about one volt above and below ground potential. The latter characteristic permits students some freedom of design in their output stage.

In addition to the electronic characteristics, the amplifier had to support an exercise subject to additional practical limitations. The exercise had to complement out design, simulate, build and measure instructional cycle. This meant it our amplifier had to be simple enough to be simulated through our department standard circuit analysis software, OrCAD-Cadence PSPICE. The exercise was further constrained to work within the limitation of our student laboratory equipment. Administrative constraints further limit the number of days which could be devoted to this exercise to seven-100 minute class meetings, spread over approximately three weeks, plus approximately six out of class clock hours. This is because the USAF Academy's curriculum is designed so that the average student can complete assigned work in 42 lesson meeting of a total of 150 minutes each. Finally, any hardware we developed had to be reasonably robust and be designed from readily available components. It also had to be fabricated in such a way that the inevitable student mis-use could be corrected with reasonable ease.

From the perspective of laboratory equipment, we have available an HP Model 54645A 100 MHz sampling oscilloscope, Kepco MPS620M +/-15V@1A DC power supplies and a Wavetek Datron 50MHz Model 80 function generator. Standard value leaded discrete components are available and may be interconnected through prototyping boards.

One obvious alternative to the custom circuit approach we have taken in the subject exercise was the application of a commercial operational amplifier whose dominant pole frequency could be adjusted externally. The pole adjustment feature is essential to illustration of pole shifting and stability under feedback. Our experience has shown that such an approach has two distinct disadvantages. First, commercial operational amplifiers have very high gain-bandwidth products. It would therefore very difficult to experimentally evaluate the loop gain of these amplifiers at low frequency. Second, commercial operational amplifiers offer students no opportunity to adjust internal parameters or to measure the condition of internal circuit nodes. The ability to verify circuit bias conditions and small signal gain across the amplifier is too important to ignore.

Another approach we considered in the development of this exercise was simply to require students construct a common pre-designed differential amplifier from discrete components. Our experience has shown this approach would inevitably involve student wiring errors which would slow the lab's execution and divert attention from the exercises objectives. Furthermore, the magnitude of parasitic capacitances inherent to proto-boards and exact placement of components, would vary widely among student

designs. These variations would make it unlikely that every student would see the desired frequency dependent behavior or achieve success in pole compensation.

The Amplifier

Based upon the considerations described above, we concluded the best method for executing the proposed laboratory exercise was to build our own custom amplifier presented to students on a custom PCB.   In order to keep the circuit simple and reasonably small, and to further minimize parasitic capacitances, we chose to implement the amplifier with surface mount components. SOT23 and SM1206 style packages were chosen for relative ease of handling. We also decided to have our PCBs fabricated through a commercial vendor so that the design could be solder masked and silk screen labeled. The former characteristic further reduces the possibilities of unintentional student short circuits and greatly eases replacement of burnt components while the latter permits easy identification of components. We also chose to place single-turn RES41 packaged potentiometers in key circuit locations, thus permitting the student some control over circuit biasing. Finally, the PCB was designed to be connected via a simple 100 mil pitch pin jack to student protoboards. Details of layout and wiring are presented in the appendix.

The amplifier's design is illustrated in the Cadence-OrCAD PSPICE schematic of Figure 1 below. An npn differential pair (Q1, Q2) with resistive loads drives a pnp common emitter (Q3), followed by an npn common collector (Q4). The schematic shows a 50Ω emitter resistance in each leg of the differential pair. This resistance represents a 100Ω potentiometer used in the hardware circuit for balancing the differential pair. R5, D3, Q5 and R1 create a pseudo Widlar current source designed to supply about 3.3mA. It's reasonably high output resistance minimizes circuit's common mode gain. The common emitter and common collector are biased at about 6mA and 5mA respectively. The widely available Zetek 2N2222 npn and 2N2907A pnp BJTs are used throughout the basic design. RC3 is illustrated with the somewhat peculiar value of 2.6445 KΩ. In order to communicate a bias condition in which the output node voltage was very nearly zero (732μV as illustrated), this non-standard resistance is used in the nominal circuit simulation. In the hardware circuit, RC3 is replaced with a fixed 2.2KΩ resistor in series with a 10KΩ potentiometer permitting students the freedom to adjust the output node bias voltage at the cost of some low frequency open loop gain.

The differential amplifier (Q1, Q2) is designed with a mid-band single-ended voltage gain of about 44. The common emitter second stage (Q3) has a designed voltage gain of only about -5.6, while unity gain is expected of the common collector output stage (Q4) with any reasonably large load resistance. The overall voltage gain is therefore expected to be about 264 V/V or 47.8dB. Unlike conventional operational amplifiers, the higher gain of the differential pair causes its transistors to set the dominant pole of the amplifier through Miller multiplication. The gain of the second stage is traditionally set much higher, thus permitting it to set the dominant pole. In this design, our choice of gain results in a combination of poles producing a marginally unstable circuit when feedback factors approaching unity are applied.
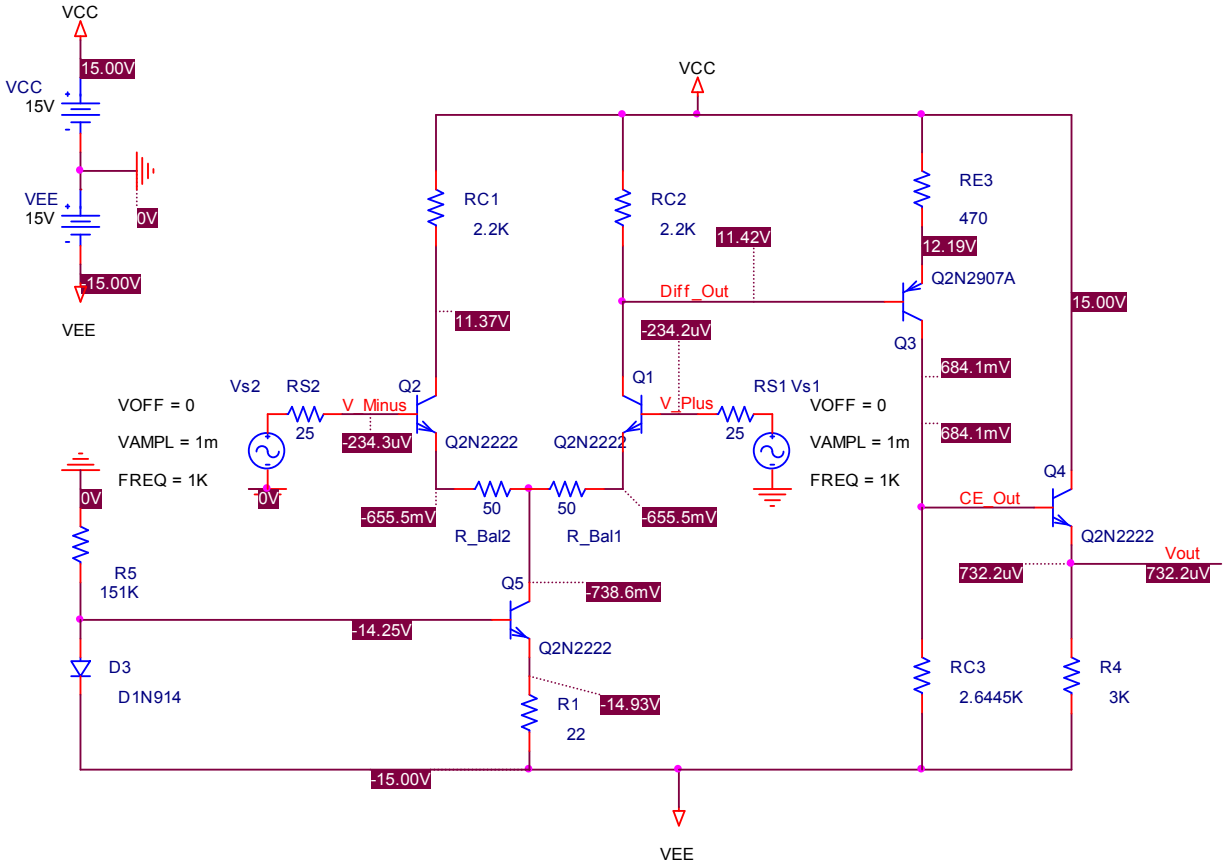
Figure 1. Cadence OrCAD Capture schematic of the differential amplifier's nominal design as presented to students. Circuit bias conditions are shown presuming both input terminals are held at ground potential. RC3's value is intentionally adjusted to 2645.5Ω so the bias voltage at the output node is very nearly ground potential.

Amplifier Stability Simulation

The feedback stability of an amplifier with feedback is generally demonstrated through evaluation of its loop gain and phase as a function of frequency.[1] In the exercises in which our amplifier is used, series-shunt feedback is required and implemented through the familiar non-inverting op amp circuit. The simple voltage divider feedback circuit used in this configuration can easily be adjusted across a wide range of values without unduly loading this preamplifier. The loop gain of this amplifier in the subject configuration is illustrated below. Here a somewhat arbitrary feedback factor, β, of 0.91 is implemented with a RF1 = 5KΩ and RF2 = 500Ω. By breaking the non-inverting amplifier's feedback loop and sweeping an ac test source, the loop gain Aβ, can be simulated as a function of frequency. The PSPICE schematic representation of the circuit arranged for loop gain analysis and the resulting frequency response are illustrated in Figure 2a and 2b below. Here the 2N2222 and 2N2907A transistor models

supplied with the Cadence OrCAD – PSPICE evaluation library are applied. AC sweep analysis confirms that the combination of amplifier poles and zeros creates a sub-minimum phase margin at this feedback factor. Indeed the loop gain becomes unity at about 33MHz with a slightly negative phase margin.

To further illustrate the instability of this circuit condition, we ask our students re-simulate the frequency response of the circuit in closed loop configuration. The behavior presented in Figure 3a and 3b below exhibit the classic gain and phase overshoot of unstable circuits with feedback. To further demonstrate instability, a sharply varying pulse source replaces the sinusoidal signal source on the non-inverting input. The results of the corresponding simulation show a sustained oscillation. Such a behavior is illustrated in Figure 4.
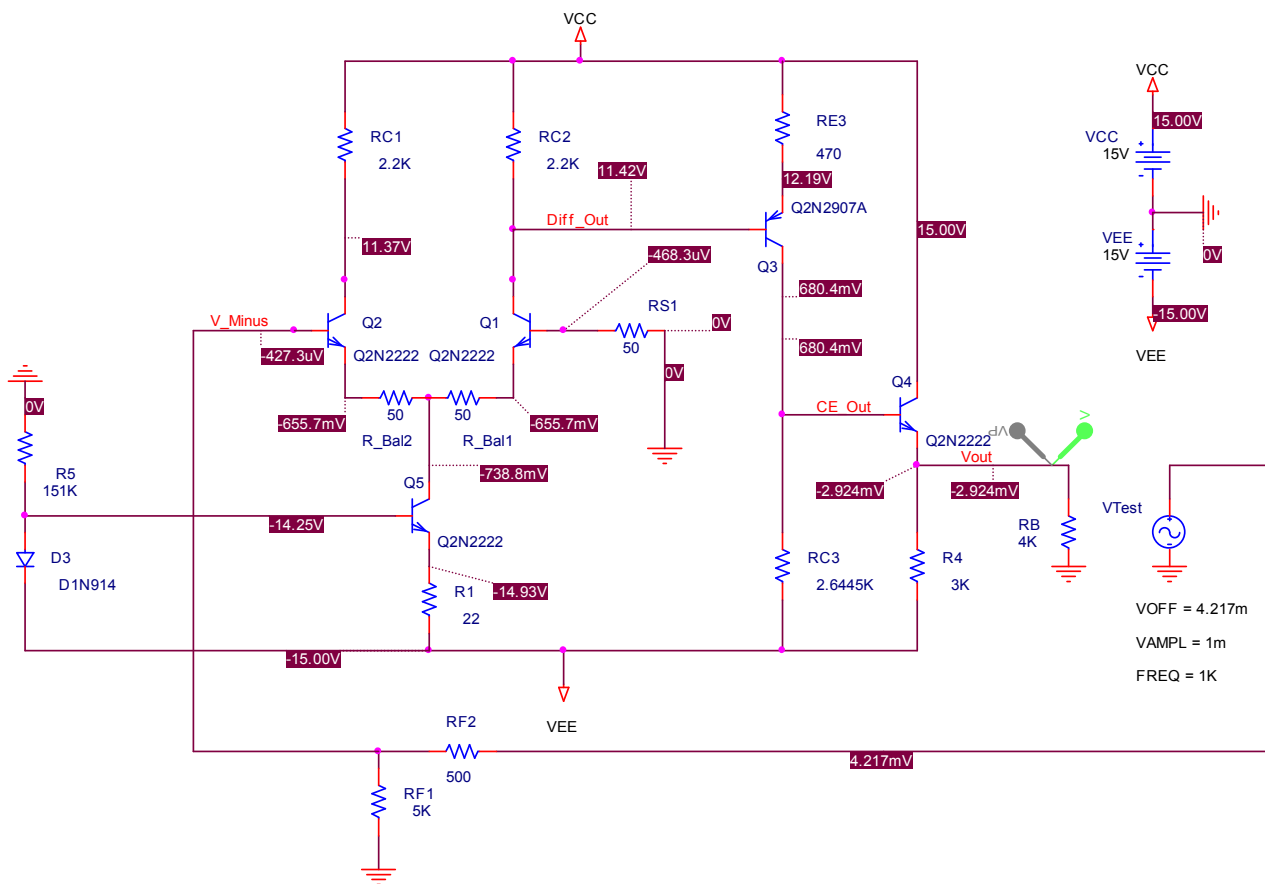

Figure 2a. Cadence OrCAD-PSPICE schematic of our amplifier configured for loop gain simulation. RF1 and RF2 are chosen for β = 0.91. Vtest's magnitude and offset are chosen to assure all components remain in active mode at all frequencies. Load resistor RB is chosen to model the resistance which the feedback network presents to the output of the circuit.
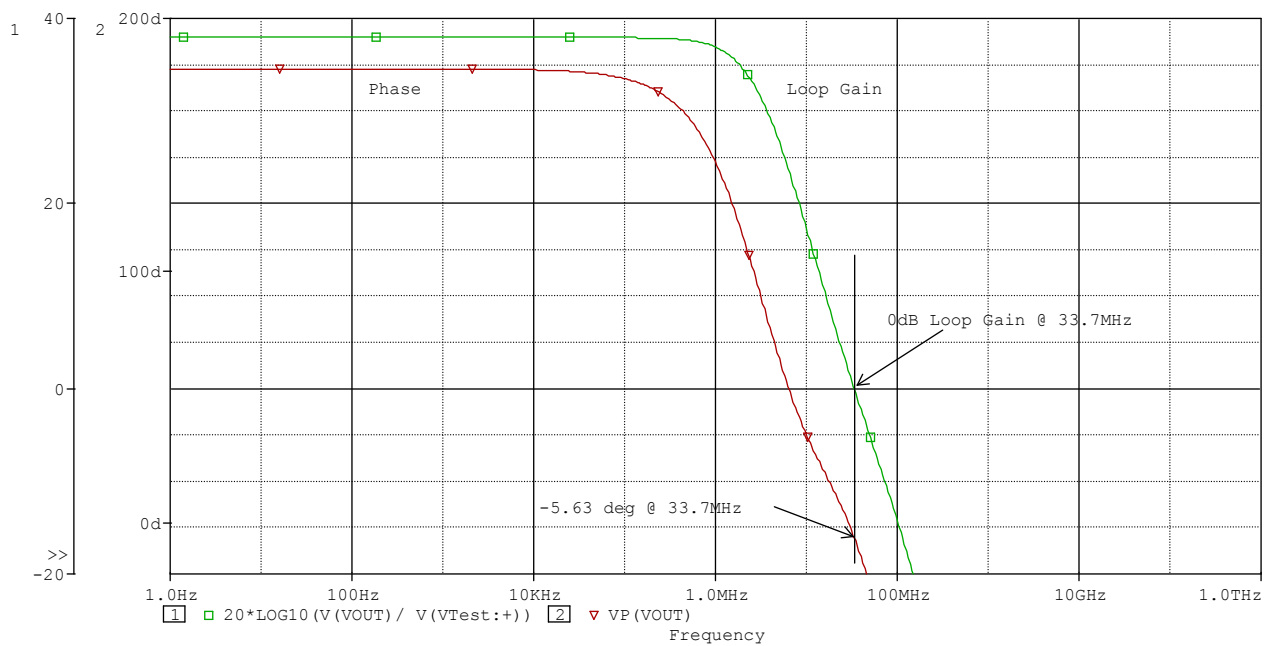
Figure 2b. Cadence OrCAD-PSPICE simulation of our amplifier's loop gain and phase with β = 0.91. Notice the resulting phase margin is about -5.6°, far less than the normally accepted +45° minimum. We therefore expect unstable operation under feedback for this circuit condition.
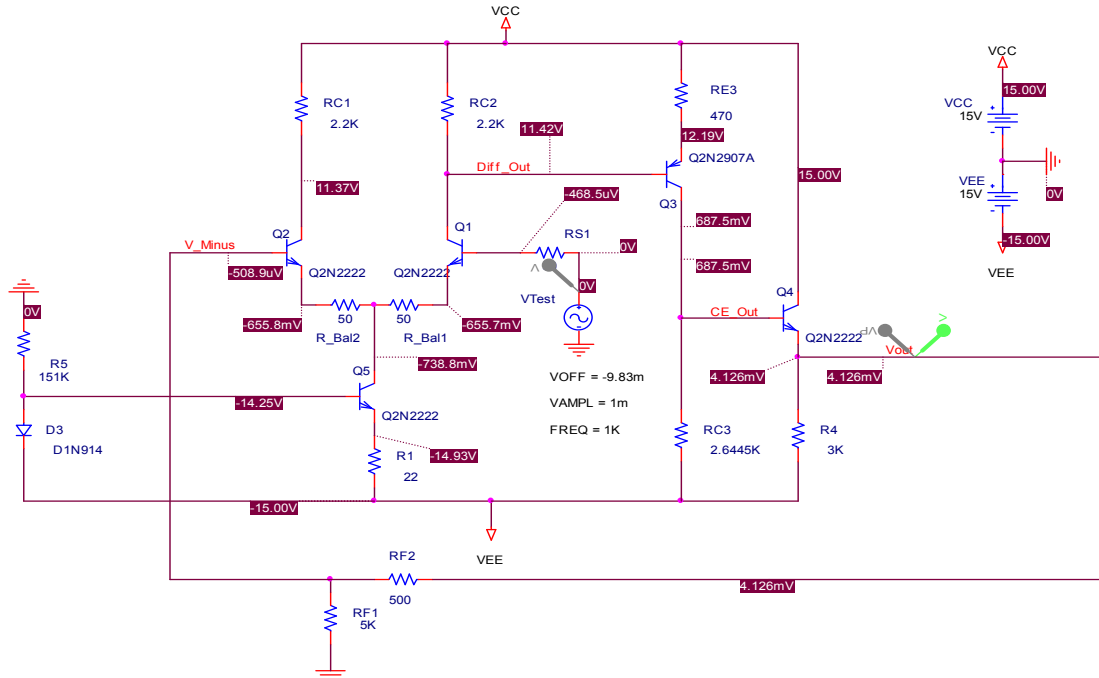

Figure 3a. Cadence OrCAD-PSPICE schematic of our amplifier in closed loop non-inverting amplifier configuration with β=0.91. The test source has been shifted to the non-inverting input and adjusted in offset and amplitude to keep all components in active mode at all frequencies of interest.
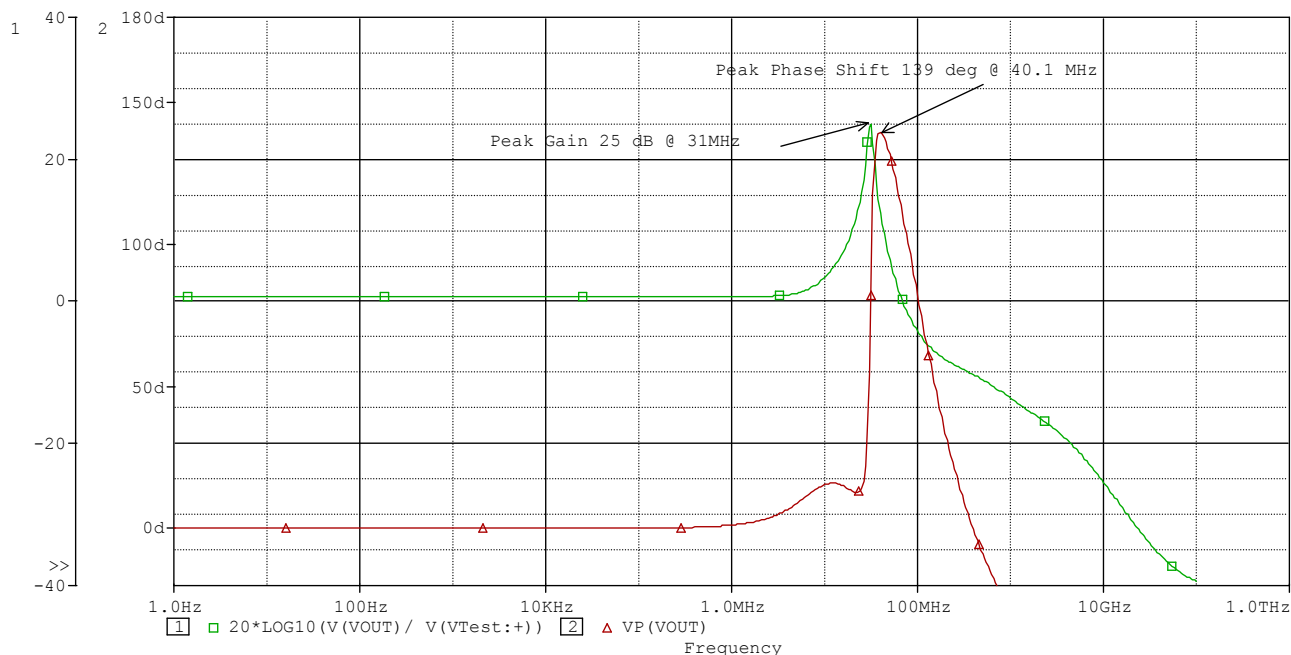
Figure 3b. Cadence OrCAD-PSPICE ac sweep of the amplifier's closed loop gain with β = 0.91. Notice the extreme peaking of the gain and the large positive phase shift. Both of these behaviors are indicative of an unstable amplifier under feedback.
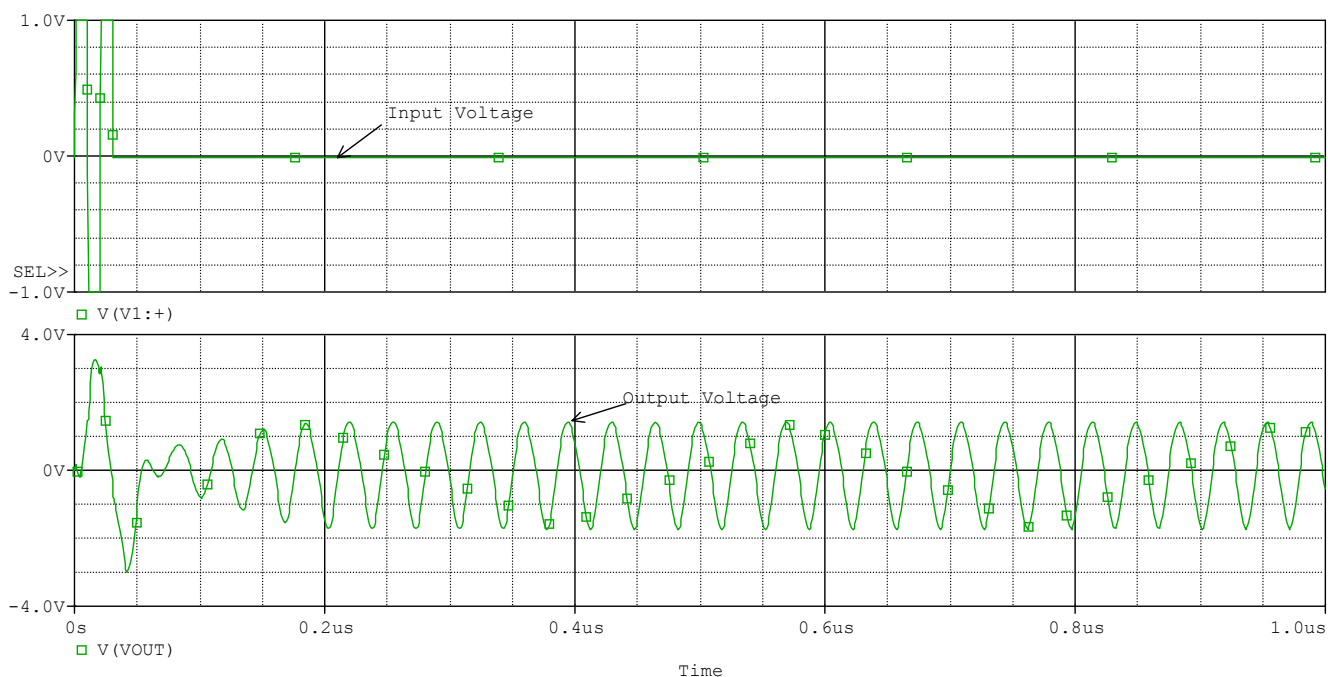

Figure 4. Cadence PSPICE Transient response of the β=0.91 configured non-inverting amplifier to an abrupt input. Notice how a sustained oscillation persists even though the input signal remains steady after the first 30nS. Instability of the circuit with feedback is clearly illustrated.

Equally important to our amplifier's behavior is the ability to improve its stability under feedback through pole compensation. It can be demonstrated that an externally capacitor applied in parallel to the differential pair transistor's $C\mu$ will create a dominant pole at sufficiently low frequency to force the amplifier to run out of loop gain well before the phase shift creates positive feedback. We ask our student to predict and then simulate this behavior through additional loop gain analysis such as that shown in Figures 5a and 5b. Here again the $\beta = 0.91$ feedback factor is applied along with 220pF pole shifting capacitor. A very generous 73 degrees of phase margin is predicted.
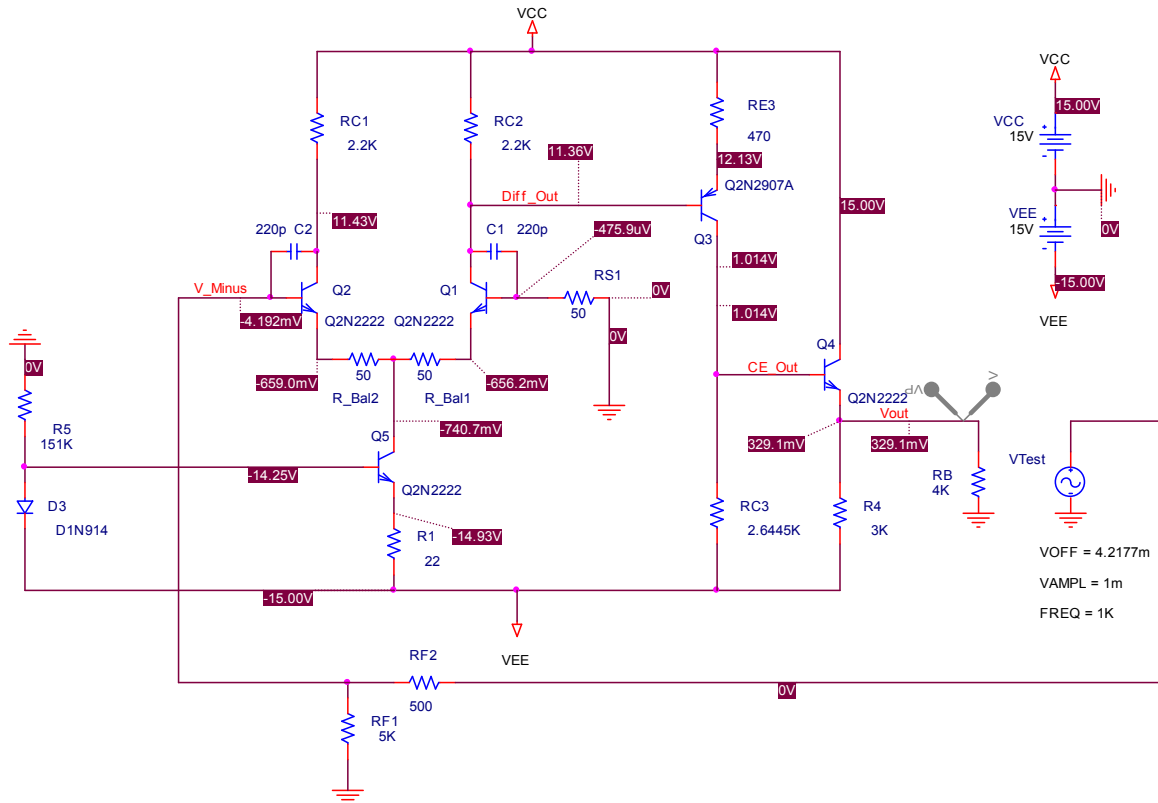

Figure 5a. Cadence OrCAD-PSPICE simulation of our amplifier with pole compensation applied. β = 0.91 as before. C1 and C2 complement the Cµ of transistors Q1 and Q2 creating a dominant pole.

In the interest of brevity, simulation of the amplifier's ac behavior under closed loop operation with compensation is not included in this paper. However, only a modest gain peaking vaguely reminiscent of Figure 3b is predicted by simulation. Transient simulation of the circuit's closed loop response to a rapidly varying input (as Figure 4) produces, as expected, a non-oscillatory behavior.
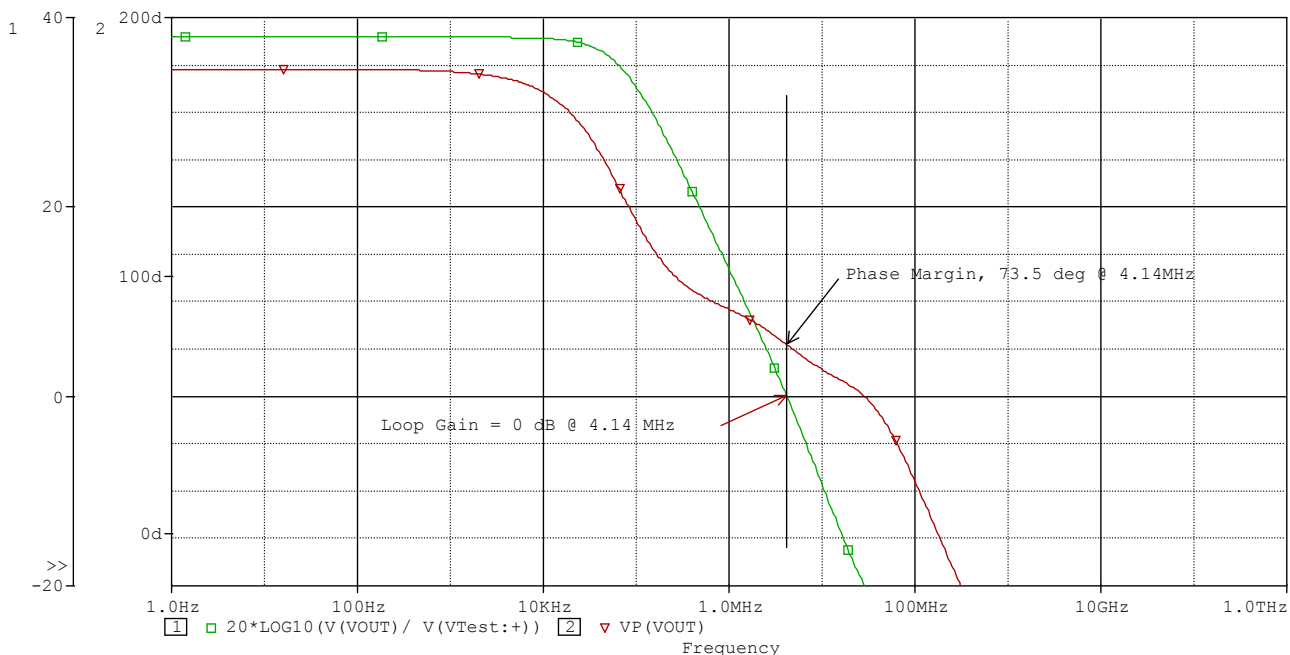
Figure 5b. Loop gain analysis of our amplifier with pole compensation. A classic - 20db/decade gain decay is exhibited at frequencies above the dominant pole set at about 100KHz. A generous 73.5 degrees of phase margin is predicted.

Hardware Performance

　　　　The strength of this exercise comes through student evaluation of amplifier performance. As explained in the appendix, our amplifier was fabricated in such a fashion that access to major nodes is possible through the PCB jack. It is therefore possible for students to evaluate and adjust the bias condition of the amplifier and apply compensation capacitors of different values. The feedback network of the student's design can be created through discrete resistors connected through the proto-board. Our laboratory equipment can then be applied to bias the circuit and subsequently measure the loop and closed loop gain of the amplifier under various conditions of feedback factor and compensation. A typical experimental arrangement for these measurements is shown below.

　　　　Although the laboratory exercise illustrated in Figure 6 includes the coupling of our amplifier to a high current output stage, we concentrate here upon the performance of the amplifier alone. Uncompensated loop gain of the amplifier with $\beta = 0.91$ is illustrated in Table 1 below.
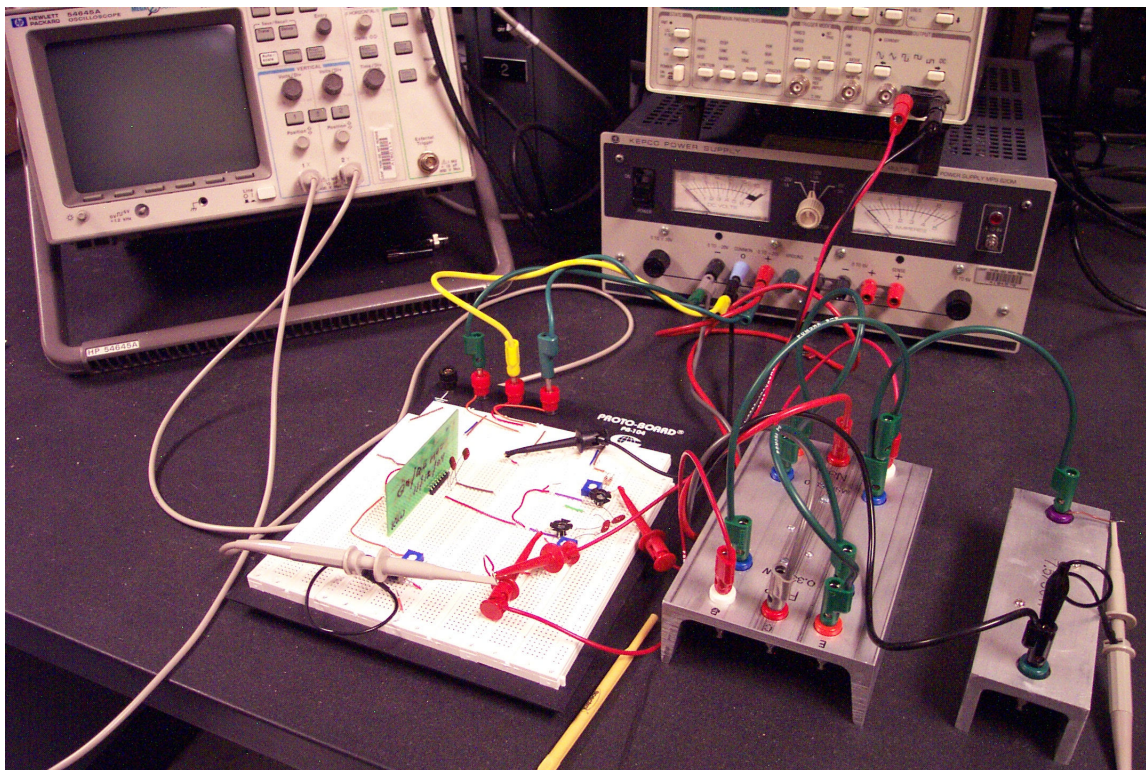
Figure 6. A typical hardware arrangement for Lab 2. Bench equipment is arranged to measure ac performance of our amplifier driving a Class AB output stage. Our PCB based amplifier appears on the left half of the protoboard. Metal channels create heat sinks for the power transistors and load resistor for the complete circuit.

These data agree reasonably well with the predictions made by PSPICE simulation. Gain of about 5 dB (vs 13dB measured) is predicted at 360 degrees of total phase shift, while a low frequency gain of about 48 db is expected at low frequencies (vs about 36 measured). The uncompensated amplifier's loop gain clearly indicates instability under feedback. Experimentally this is found to occur consistently. The same amplifier evaluated for Table 1 exhibits a closed loop oscillation of about 2.5 Vpp at 8.5 MHz, even with the input signal turned off. The addition of the pole compensation capacitors instantly eliminates the oscillation. Loop gain measurements of the amplifier with the 220pF pole compensation capacitor is presented in Table 2.

Frequency	Loop Gain	Phase (Degrees)
1 KHz	36.4 dB	180
1 MHz	34.4 dB	224
3 MHz	27.6 dB	273
5 MHz	22.2 dB	302
12.8 MHz	13.8 dB	360
20 MHz	0 dB	412

Table 1. Experimental loop gain for the amplifier without compensation. β = 0.91 using RF1 and RF2 as in the simulation. Significant gain is measured when the total phase shift will create positive feedback. Unstable operation of this amplifier is therefore expected.

Frequency	Compensated Loop Gain	Phase (Degrees)
1 KHz	36.2 dB	180
10 KHz	36.15 dB	180
100 KHz	31.5 dB	230.8
2.56 MHz	0	304

Table 2. Compensated loop gain for the amplifier with β = 0.91. The dominate pole (-3dB point) occurs at frequency somewhat lower than 100KHz, consistent with simulation. The phase margin of 56 degrees agrees reasonably well with the predicted 73 degrees.

Again for the sake of brevity, I do not include closed loop compensated gain performance data. It is worth noting however, that under feedback, the amplifier produces the expected A / (1 + A β) gain of 1.09 V/V at low frequencies. A slight gain peaking occurs at 4.3 MHz, just as predicted by simulation.

Student Experience

Several years of experience have provided some experience worth noting for this amplifier. The PCB implementation has proven relatively robust with two exceptions. At the hands of our students, the current source transistor Q5 has suffered more burn-outs than any other active device in this design. Likewise, the common collector output stage transistor, Q4, is often burnt out due to mis-biasing of the following stage. We have replaced the corresponding transistor with the Zetek FMMT497TA, which possess a higher V_{CE} maximum rating. This change has virtually no impact upon simulated performance as the roles these new transistors play in the amplifier have minimal impact upon the frequency response of the amplifier. Furthermore, we have found the application of a heat sinking tape over Q5 improves its resistance to burn-out and eliminates the bias "creep" we observed in earlier versions. We have also found it helpful to pre-align the balancing potentiometers prior to use. This practice gives our students a solid starting point upon which they can rely when first powering the amplifier. We have also found that the number of available amplifier PCBs should be about two amplifiers per student. This practice assures us that sufficient hardware will be available for all students to complete the exercise successfully. Finally we have made it a practice to forewarn students to avoiding a continuously oscillating circuit condition in the relatively close quarters of out electronics laboratory. Unstable circuits will easily radiate RF signals to adjacent workstations, resulting in confusing interference for other students.

Conclusion

We have presented a pedagogical framework and implementation method for illustrating analog amplifier concepts via a prepared differential amplifier. This custom amplifier is intentionally designed to permit students to observe the behavior of an inherently unstable design under feedback and experience stability compensation methods first hand. We have found this methodology to produce hardware data relatively consistent with predictions, to be robust enough to survive student mis-handling and an excellent complement to our combine classroom - laboratory program in electronics.

Bibliography

[1] Adel Sedra and Kenneth Smith, "Microelectronic Circuits", 5th Edition, Oxford University Press, 2004, Section 8.7, pg. 831.

Biography

KENNETH J. SODA. Dr. Soda is the first permanent civilian faculty member of the USAF Academy's Department of Electrical Engineering, where he directs education in VLSI circuits, electronics and project design. He holds an advanced degree from University of Illinois, Urbana-Champaign. Dr. Soda is the 1997 Recipient of the Tau Beta Pi Teacher of the Year Award (Colorado Zeta Chapter) and the 1988 Recipient of the USAF Academy Outstanding Educator Award.

Appendix
Pre-Amplifier Hardware Implementation

The actual hardware implementation of this design includes three potentiometers. The first, R_Pot_Bal, permits compensation of for differential pair asymmetry. The second potentiometer, R_Pot_Bias, controls the reference current for the pseudo-Widar current source. The final potentiometer, R_Pot_Out controls the total collector resistance of the Common Emitter and therefore also controls the DC bias of the output voltage. In all cases, the potentiometers have been placed in series with a fixed value resistor, thus preventing short circuits. The value of each resistance value called for in the nominal design can be achieved through the combination of the fixed resistor and potentiometer. A schematic of the hardware implementation of the circuit appears below.
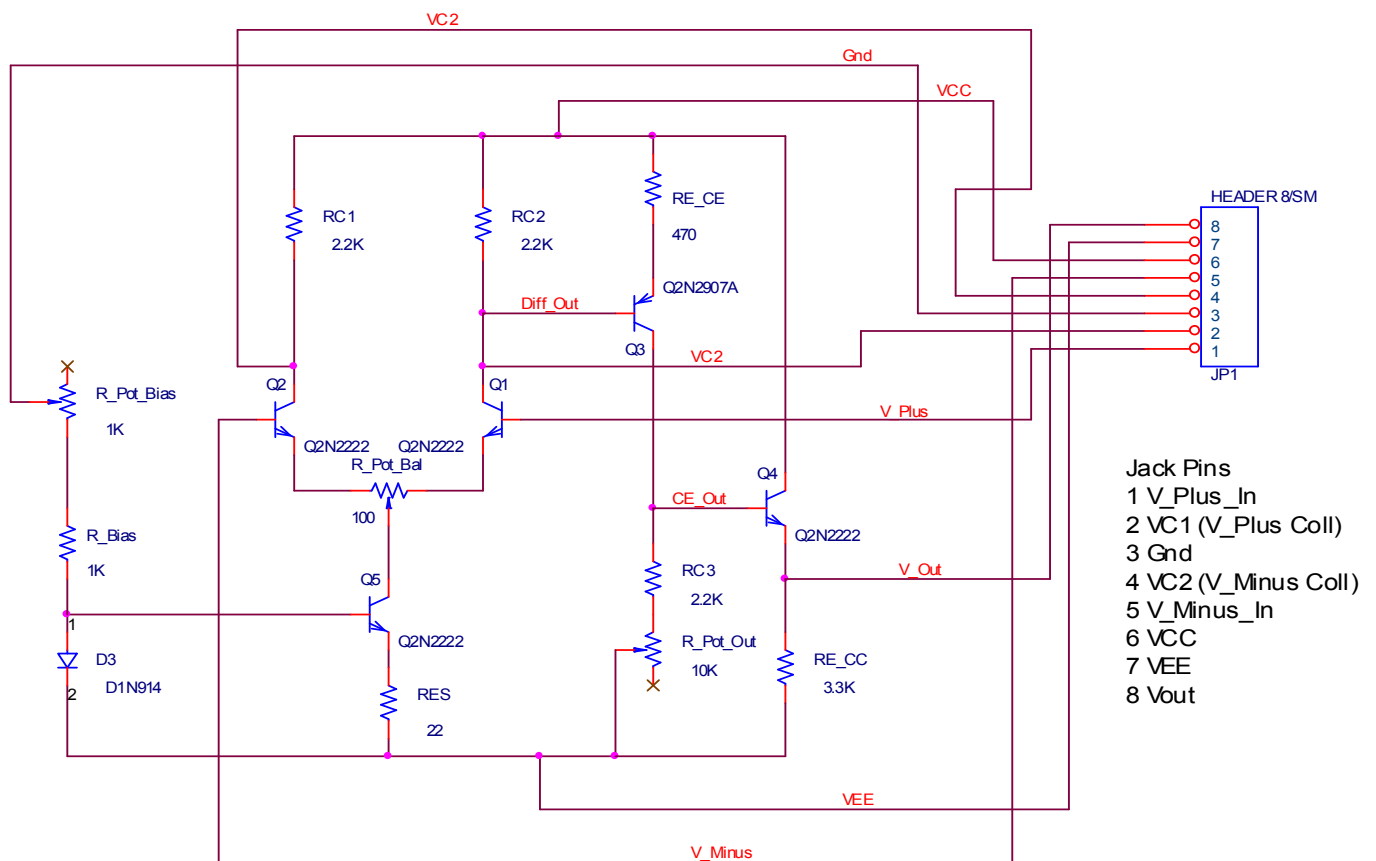
Pre-Amplifier Printed Circuit Board

The pre-amplifier circuit has been implemented on a custom single sided printed circuit board. Miniature "surface mount" components are used throughout. This implementation reduces the magnitude of parasitic impedances and the variability inherent in plug boards. A single jack interfaces signal and power according to the pin connections described above. The orientation of parts is shown in the layout diagram below. Pin 1 of the jack appears at the top of the header (see diagram below) and is further designated by the square (versus round) metal pad. The angled jack pins have been designed so the pre-amplifier can be connected directly to a standard proto-board with 0.1 inch pitch sockets.

The power dissipation ratings of the components have been chosen so that burn out of components is unlikely when it is properly operated with +/-15 volt supplies.

Lab 2 Pre-Amp PCB
Front Surface View

Pin 1

Pin 8

Amplifier with metal scale for comparison