AC 2010-255: EMULATING INDUSTRIAL PRINTED CIRCUIT BOARD DESIGN PRACTICE BY DESIGNATING THE COURSE INSTRUCTOR AS THE FABRICATOR: A COST EFFECTIVE DESIGN EXPERIENCE FOR ELECTRONICS CIRCUITS LABORATORIES AT THE JUNIOR LEVEL

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Emulating Industrial PCB Design Practice By Designating The Course Instructor As The Fabricator: A Cost Effective Design Experience For Electronics Circuits Laboratories At The Junior Level

Abstract

For two years, the University of San Diego has included Printed Circuit Board (PCB) layout design and test in the laboratory portion of the second of two junior level electronic circuits courses that is required of all electrical engineering majors. A replication of PCB design and standard industry Gerber file export experience encountered in industry was developed. A model was developed for the PCB design experience that emulated real-world situations and cost criteria. In this model of the industrial design situation, the instructor served as the fabricator. Students individually used industry standard schematic capture and layout software to develop a PCB for a simplified discrete μA741 operational amplifier. The layout designs were submitted as Gerber files electronically to the instructor/fabricator for evaluation.

Grades were assigned by evaluating the accuracy and cost effectiveness of the design by minimizing traces, reducing PCB geometry, and limiting the number of vias. Feedback was provided by the instructor acting as the fabricator to individual students and a single fabricated printed circuit board, designed by the instructor (and fabricated by a commercial PCB manufacturer), was delivered to students for assembly and test. Although the PCB delivered is different than the one design by students, it is common for PCB fabricators to recommend changes to the original design and deliver a board that is not the same as the original design. By delivering a single PCB design to students, fabrication costs can be minimized and students can inspect the delivered board as an exemplar.

Assessments of the student perceptions of knowledge of and confidence in applying printed circuit board techniques in designing and releasing a printed circuit board were conducted prior to and after the PCB layout design and test. On a 5-point scale, overall student-reported knowledge increased by 2.79 and overall student confidence increased by 1.25 points. Faculty assessment of knowledge, as measured by scoring short answers to knowledge statements, correlated well with student report and showed an average increase of 2.85.

The instructor/fabricator model for PCB layout design experience allowed for a low cost and realistic design experience for students. As such, this model could be implemented economically in many programs as a means for introducing PCB layout design in their curriculum.

I. Introduction

It is typical that electrical engineers design printed circuit boards (PCB) during the prototype stage of product development in addition to that for the actual sellable mass produced product. It is therefore important that students are exposed to the process for releasing printed circuit board designs to board fabricators. Modern fabricators accept electronic transmission of PCB designs using industry standard Gerber (RS-274) files. The PCB is priced using several criteria including geometric area, number of copper trace layers, number of vias that intersect the copper trace layers, number of drilled holes, and number of hole sizes. To reduce fabrication cost, the design engineer strives to reduce all of the parameters that determine the price of the PCB.

At the same time, the importance of copper trace current carrying capacity must be taken into account. A signal trace does not necessarily require large copper trace widths. However, current-carrying copper traces (power distribution lines) may require wider traces to reduce heating and to provide noise immunity. Signal trace lengths must be considered since long lengths may impact performance. Ground distribution must also be considered.

Once design and cost reduction aspects are considered, the designer must upload the PCB design files to the fabricator for a quotation. Good fabricators typically review the uploaded Gerber files for design errors and often suggest changes to the layout design. The PCB is fabricated upon agreement of any changes or revisions.

In most cases, the engineer will not be intimately involved with the actual fabrication process but interacts with the fabricator. The primary challenge faced in this project was to create an environment that simulated an industry-like atmosphere for PCB design. In many instances, the fabricated PCB is altered by the fabricator after consultation with the original designer to reduce cost and/or to increase performance. An additional constraint was the departmental budget: it was cost prohibitive to allow each individual student to submit their design for development by a fabricator.

To address the challenges, a model was created and tested over two years in which the instructor of the laboratory portion of the second of two required junior-level electronics courses took the role of the fabricator. Each student submitted a design to the instructor electronically and, in order to include other educational aspects of the exercise, also submitted schematics, the actual layout layer files, and a three dimensional rendition of the finished PCB created by the layout software. The software used was the National Instruments Electronics Workbench® suite of software design tools. Multisim® was used to capture the schematic and Ultiboard® was used as the layout design software platform.

The instructor interacted with the student designers and evaluated the layout and schematic designs according to fabrication pricing parameters. An altered optimized layout was provided to students as feedback. All students received the same altered layout. That optimized layout was manufactured by external fabricators.

While each student fully experiences the PCB design experience, the advantage of this new instructor/fabricator model is that only one PCB design is manufactured by the fabricator. By having only one PCB design fabricated, the cost of the laboratory exercise is significantly lower than that incurred if individual designs were sent to the fabricators, students experience realistic interaction with a fabricator, and there is essentially no delay between design and test.

Other Models of Fabrication

While PCB design and fabrication has been introduced to students at many institutions, it is typical that the experience allows for individual boards to be fabricated[1, 2, 3]. Alternatives explored in past publications to reduce fabrication costs are to use in-house chemical etching methods and micro-milling copper traces. While these methods to reduce fabrication cost are important, they do not addressed the requirements encountered in real interactions with industry PCB fabricators. The new instructor/fabricator model of PCB instruction directly addresses cost and manufacturability issues that have not been addressed in past publications on student PCB design experiments.

This paper directly addresses issues of PCB design and cost criteria associated with industry PCB fabricators with the instructor acting as the fabricator. A single PCB layout design is fabricated and tested by all students, thus reducing fabrication cost for the laboratory experience.

II. Goals of the Design Experience

The basic goals of the design experience were:

- To develop a meaningful printed circuit design laboratory
- To improve student knowledge of schematic layout techniques
- To introduce students to good layout criteria and to become familiar with industry standard practices
- To introduce students to the design "hand-off" process to fabricators and their pricing parameters
- To give students confidence in applying the knowledge obtained
- To develop experiments to test the fabricated circuit

In order to meet these goals, the course team:

- Selected an appropriate circuit to be implemented for layout
- Provided instruction on schematic capture and its interaction with layout software
- Provided instruction on good layout practices
- Evaluated the test procedure upon completion of the fabrication and component population of the PCB.

The learning objectives of the laboratory experience included :

- Designing transistor amplifier circuits incorporating feedback to meet design goals.
- Designing level shifting circuit stages
- Designing output (power amplifier) stages
- Using a circuit simulation tool (*Electronics Workbench Multisim*®) to enter schematics with footprint geometries used in PCB design

- Using a circuit simulation tool (*Electronics Workbench Multisim*®) as an aid in the analysis of a discrete op amp circuit
- Using a PCB design tool (Electronics Workbench Ultiboard®)
- Designing appropriate trace widths, trace spacing, via formation and other geometry related topics in PCB design
- Using design rule checkers for PCB design
- Generating PCB reports in Gerber and other formats
- Constructing electronic circuits and verifying performance characteristics experimentally.
- Writing a PCB test plan with verification test procedures.

III. Schematic Capture

The goal of the laboratory experience was to design a PCB for a simplified discrete transistor version of the 741 operational amplifier. The design chosen is shown in Figure 1. The design also allowed exploration of the operation of the different segments of the operational amplifier design.

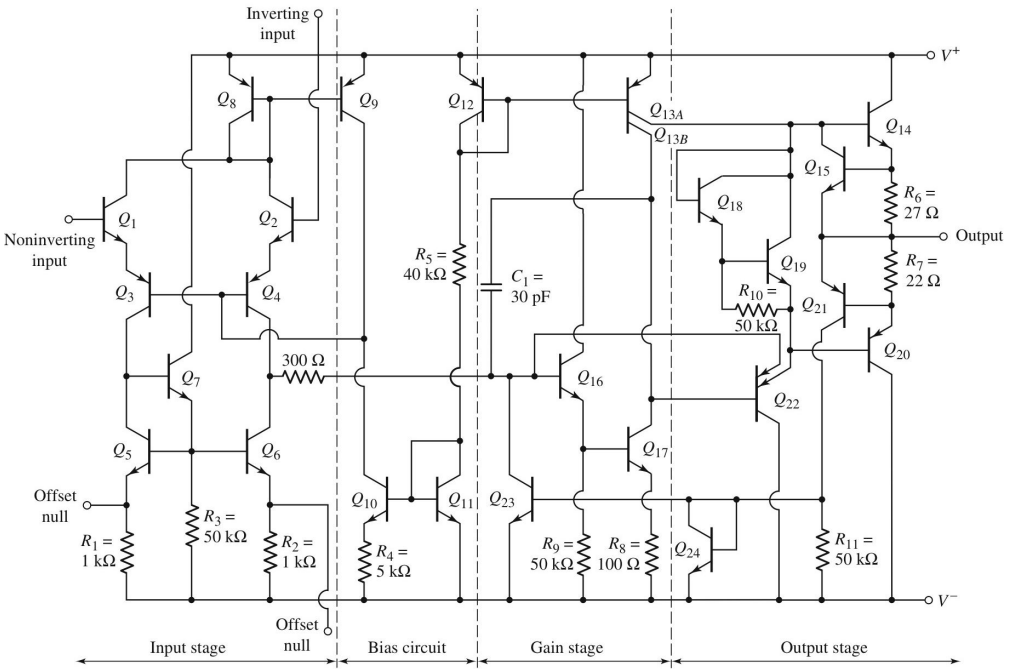


Figure 1. 741 Operational Amplifier Equivalent Circuit

While the schematic is complete, capturing the schematic requires that:

- Component geometries must be included in the captured schematic to allow seamless interface to the PCB layout software
- Inputs to and outputs from the PCB must be included as connectors or, as in this exercise, header pins
- Traces that interconnect components should be labeled accordingly

The instructor's captured schematic is shown in Figure 2. For comparison, an example of a student schematic is shown in Figure 3. Although each student's captured schematic varies from that of the instructor, the general techniques for entering the schematics is consistent.

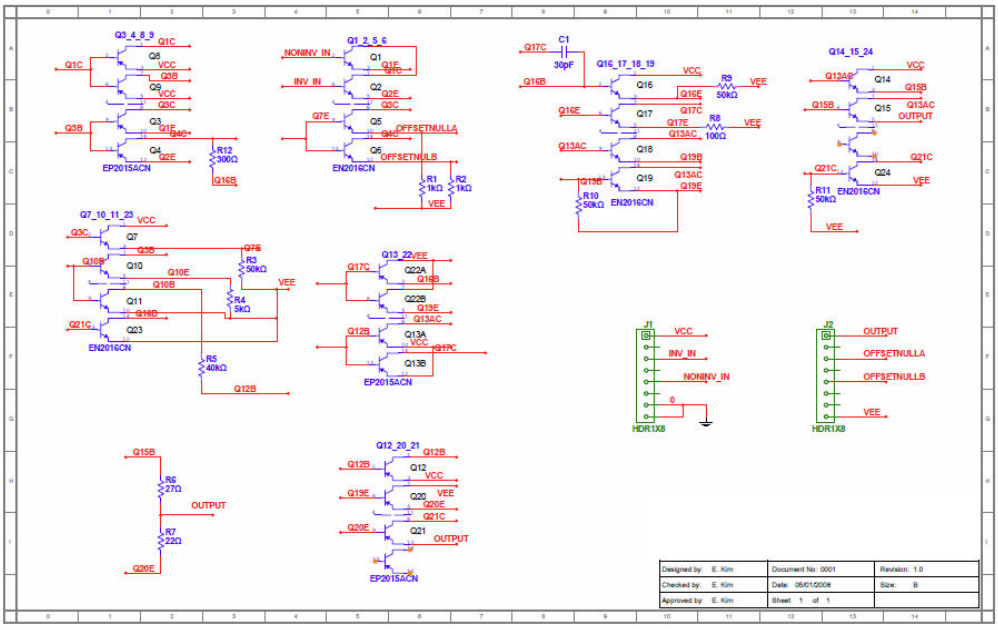


Figure 2. Instructor's Captured Schematic

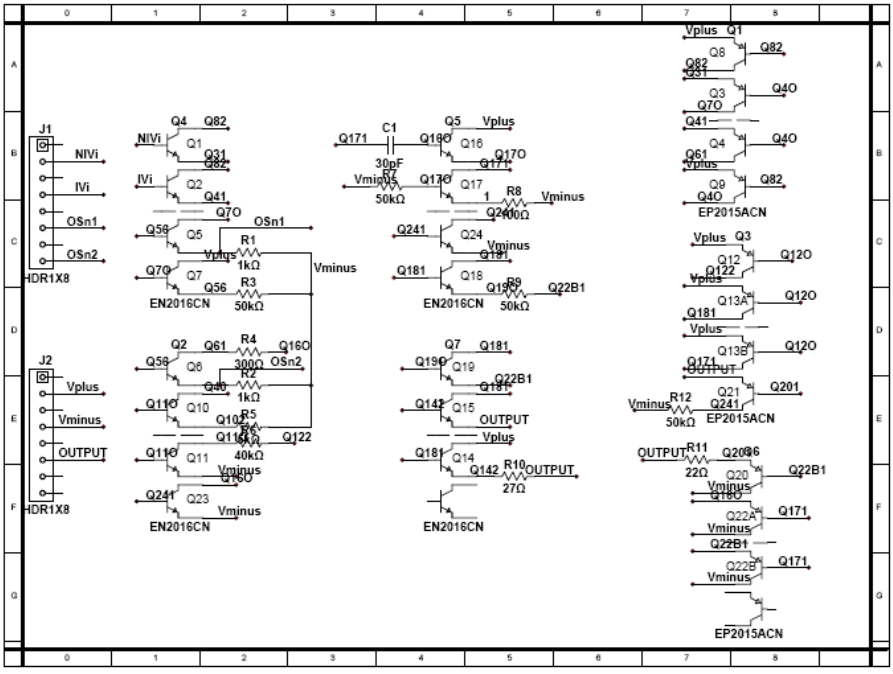


Figure 3. Example Student's Captured Schematic

In order to reduce the complexity of the PCB layout and to improve transistor matching, quad NPN and PNP transistor packages in DIP packages were used. All resistors were either 1/8 or1/4

watt rated carbon film resistors and all capacitors were ceramic disc capacitors. All components were thru-hole components to reduce assembly complexities that may be encountered with assembling surface mount devices.

Proper component geometries were included in the properties of each component to allow seamless interface to the Ultiboard® layout software.

IV. Layout Design

Using the completed schematic, the students were instructed to design a two layer printed circuit board while considering cost implications of increasing:

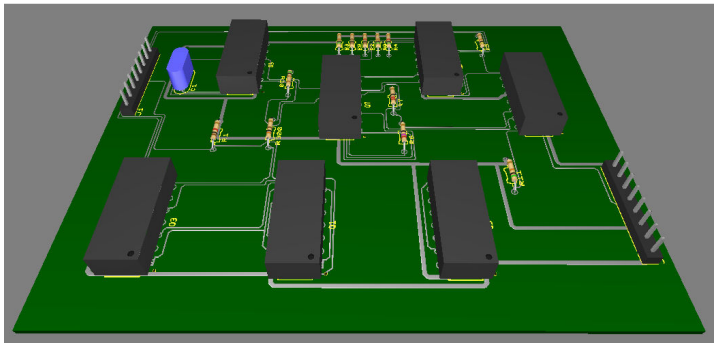
- Board area and geometry
- Number of thru-holes
- Number of different hole sizes
- Number of vias

Additionally, trace width requirements were to be considered. Power and ground traces need to be wider than signal traces. Placing of input and output pins from the PCB was to be considered. Spacing between components was to be sufficient for manual assembly using a soldering iron.

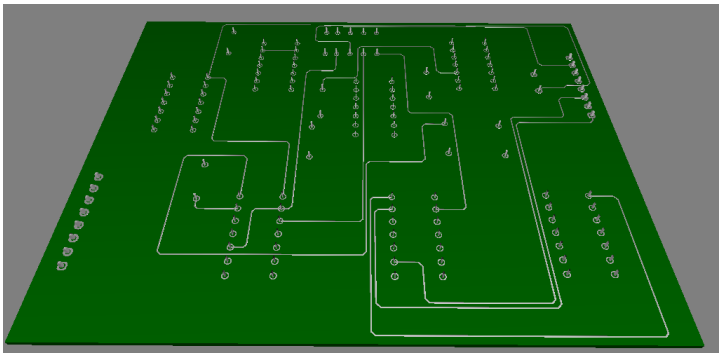
The laboratory experiment procedure given to students is summarized below:

- Use National Instruments/Electronics Workbench MSim®. Use the EN2016CN for the npn BJT quad DIP-16 (16 pin DIP) package geometry and the EN2015ACN for the pnp BJT quad DIP-16 package geometry for the MPQ2222 and MPQ2907, respectively.
- Familiarize yourself with the Ultiboard® layout package by working though the Ultiboard® Tutorial.
- Provide ports in and out of your circuit – use a header(s) for ease of interfacing
- Export the file to Ultiboard® after completing your MSim schematic.
- The maximum board size is 4" x 6". Make the board smaller so that the cost is lower.
- The board is two layers of G-10 standard 63 mils thick.
- Minimize the number of vias.
- Increase the thickness of power and ground traces – make them at least 20 mils wide. Signal traces can be 10 mils wide.
- You will be using quad-pack MPQ3904 npn BJTs and MPQ3906 npn BJTs in DIP-16 packages.
- Upon completion of the Ultiboard® layout, provide the instructor with Gerber files of the layers, board, drill sizes, and any other PCB manufacturer required information.
- The instructor will act as the PCB manufacturer and grade as if the design is going to fab.
- A fabricated PCB will be returned to you for stuffing and test.
- Provide collegial support to members of your laboratory team and others. However, all designs should be unique.
- You will do an evaluation of the team member's design.
- You will be constructing and testing the circuit so begin simulating the equivalent op amp Circuit.
- You will be asked to write a test plan for the PCB.

Top and bottom three dimensional top and bottom layer views of an example student PCB design is shown in Figure 4.



(a)



(b)

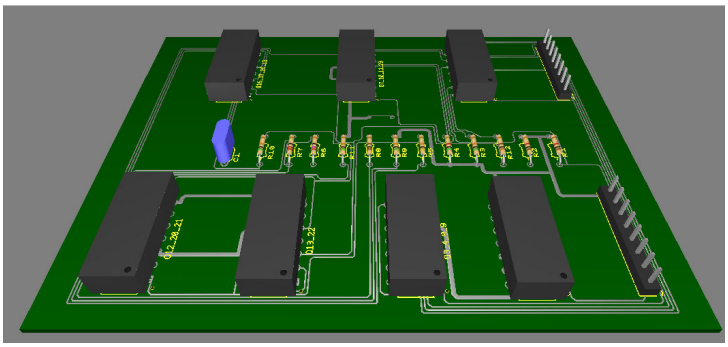
Figure 4. (a) Top Layer View of a Student PCB Design. (b) Bottom Layer View of the PCB Design

The PCB statistics for this design shown in Figure 4 are calculated by Ultiboard® and is given in Table I. This particular design is excellent in that it has no vias or jumpers.

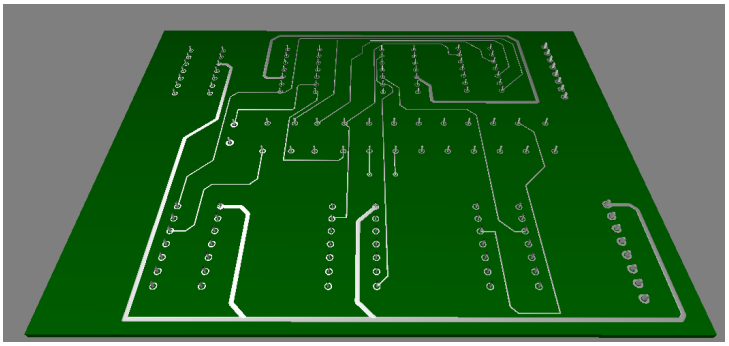
Table I. Statistics for the PCB in Figure 4.

STATISTICS		
Parts :	22	
Vias :	0	
Pins :	140	
Test pins :	0	
Jumpers :	0	
Nets :	27	
Pins in net :	110	
Connections :	83	
Unrouted connections :	0	
Router completion rate :	100	%
BOARD OUTLINE		
Length (x) :	1.02E+08	nm
Width (y) :	76.7E+06	nm

The instructor/fabricator's three dimensional layout view is shown in Figure 5.



(a)



(b)

Figure 5. (a) Top Layer View of the Instructor/Fabricator's PCB Design. (b) Bottom Layer View of the PCB Design

The PCB statistics for the instructor/fabricator's design shown in Figure 5 are given in Table II. The student design (Figure 4) is excellent because it did not incorporate any vias or jumpers. While this particular student's design was superior in terms of fabrication cost, testability issues favored the instructor's design and it was used as the fabricated design.

Table II. Statistics for the PCB in Figure 5

STATISTICS	
Parts :	22
Vias :	4
Pins :	140
Test pins :	0
Jumpers :	0
Nets :	29
Pins in net :	113
Connections :	84
Unrouted connections :	0
Router completion rate :	100 %
BOARD OUTLINE	
Length (x) :	1.02E+08 nm
Width (y) :	76.2E+06 nm

V. Test

The PCB was assembled by individual students using the instructor/fabricator's designed PCB. The procedure for testing the PCB is:

- Power up the VCC and VEE slowly to +15V and -15V respectively. If there are no large current draws, then the circuit has probably been assembled correctly.
- Implement a unity gain buffer with your PCB op amp. Let VCC and VEE equal +15V and -15V, respectively. Input a 1 V signal to the non-inverting input. Comment on the results.
- Implement an inverting amplifier with a gain of -10 with your PCB op amp. Let VCC and VEE equal +15V and -15V, respectively, and let the series input resistor be 1k and the feedback resistor equal 10k. Input a 1 V signal to the non-inverting input. Comment on the results.
- Using a the circuit of Part (C) and use a 1 kHz input sinusoid, check the INPUT STAGE and the BIAS STAGE: Confirm the voltages and currents for the input, bias, and gain stages of the operational amplifier (as shown in Figure 1).

VI. ASSESSMENT

One of the aims of this study was to assess student learning in laboratory concerning the design and fabrication of bipolar junction transistor circuits on a PCB. Specifically:

- Does this design laboratory activity increase basic understanding of PCB design and design tools?
- Does student confidence in applying the concepts learned and using PCB design tools increase?

Short questionnaires were designed to provide insight into the student level of knowledge concerning the design of analog circuits and PCB boards and their confidence in applying that

material. At the beginning of the multi-week design exercise, students were asked to score (on a scale from 1 to 5) their prior knowledge. To provide further insight into actual student knowledge level, students were asked to respond with a short answer to the knowledge questions, and these short answers were scored by the investigators at a later time. After the design exercise was completed, the questionnaires were again completed by the students and the post-exercise written responses scored by the investigators to measure changes in knowledge level. In order to track individual student incremental changes, each survey was coded with a secret number, thereby preserving student anonymity. In spring 2009, five students completed both surveys, and eight students, "seniors" who took the class the previous year, completed only the second survey of the pair. The exercise will be repeated in spring 2010 for a group of approximately sixteen students. The use of student-assigned scores to assess gains in student knowledge and confidence has been successfully used by the investigator team in previous studies[4, 5].

The following eight questions concerning knowledge of the PCB design and test process were asked before and after the lab exercise:

- What are the best ways to interconnect layers on a PCB?
- When designing a PCB, at what stage are component geometries specified?
- How should ground and power traces differ from signal traces on a PCB?
- Where should off-board interfaces be most effectively placed?
- What design factors are major contributors to the cost of PCB fabrication?
- What are the primary factors in determining where specific components are placed on a PCB?
- When soldering, where should the soldering iron be placed to create the most effective electrical connection?
- What are some of the major fabrication/build factors that increase the potential for circuit failure?

The knowledge score was based on the following scale:

1 = No clue, this concept is new to me
2 = Low, I have only heard about the concept
3 = Moderate, I know about the concept, but have not applied it
4 = High, I know the concept and have tried it
5 = Superb, I know the concept and have successfully applied it

The distribution of students' answers on their knowledge of PCB design concepts and practice before and after the exercise is given in Table III for each statement on the questionnaire. A histogram of the aggregate students' knowledge before and after the experiment is shown in Figure 6.

Table III. Knowledge of the subject matter survey statements with student responses pre-experiment and post-experiment with tabulated incremental changes.

Knowledge Statements student responses	When	Distribution					Incremental Change								
		1	2	3	4	5	-4	-3	-2	-1	0	1	2	3	4
What are the best ways to interconnect layers on a PCB?	pre	4											3	1	
	post			4	1										
When designing a PCB, at what stage are component geometries specified?	pre	4										1		3	
	post		1	1	3										
How should ground and power traces differ from signal traces on a PCB?	pre	4												1	3
	post				2	3									
Where should off-board interfaces be most effectively placed?	pre	4											1	3	
	post			1	4										
What design factors are major contributors to the cost of PCB fabrication?	pre	3		1							1			1	2
	post			1	2	2									
What are the primary factors in determining where specific components are placed on a PCB?	pre	4			1						1			2	2
	post				3	2									
When soldering, where should the soldering iron be put to create the most effective electrical connection?	pre	4	1										2		3
	post			1	1	3									
What are some of the major fabrication/build factors that increase the potential for circuit failure?	pre	4											1	3	
	post			1	4										

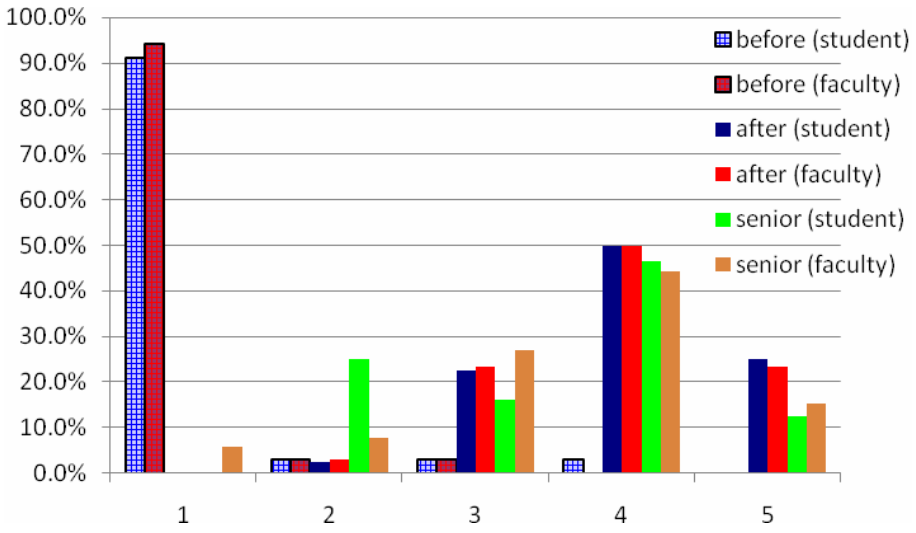


Figure 6. Histogram of Overall Student Knowledge

Students reported very low levels of knowledge prior to the beginning of the exercise with 91.2% of the student responses at the lowest level ("No Clue") and an overall average knowledge score was 1.18. Faculty assessment of the student's short responses (IV) correlated well with 94.1% of the short-answer responses rated at the lowest level and an average score of 1.09. Students reported significant gains of almost three full levels in knowledge averaging: the final student reported average score was 3.98. Faculty assessment of the short responses correlated nicely with the student report and the final faculty-assessed average score was 3.94. The distribution of

individual incremental scores is show in the right columns of III and IV. A summary of the overall individual incremental change in knowledge scores is shown in Figure 7.

Table IV. Faculty scoring of student responses to knowledge questions pre-experiment and post-experiment with tabulated incremental changes.

Knowledge Statements faculty scoring	When	Distribution					Incremental Change								
		1	2	3	4	5	-4	-3	-2	-1	0	1	2	3	4
What are the best ways to interconnect layers on a PCB?	pre	4											1		
	post			2											
When designing a PCB, at what stage are component geometries specified?	pre	4										1			
	post		1		1										
How should ground and power traces differ from signal traces on a PCB?	pre	4											1	2	1
	post			2	2	1									
Where should off-board interfaces be most effectively placed?	pre	4											1	3	
	post			2	3										
What design factors are major contributors to the cost of PCB fabrication?	pre	3	1									1		2	1
	post			1	3	1									
What are the primary factors in determining where specific components are placed on a PCB?	pre	4		1								1		2	2
	post				3	2									
When soldering, where should the soldering iron be put to create the most effective electrical connection?	pre	5											1	1	3
	post			1	1	3									
What are some of the major fabrication/build factors that increase the potential for circuit failure?	pre	4												4	
	post				4	1									

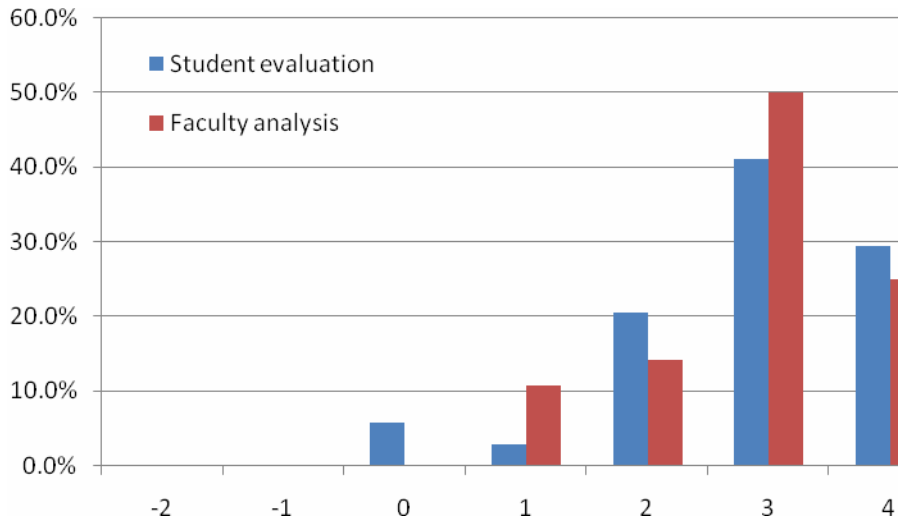
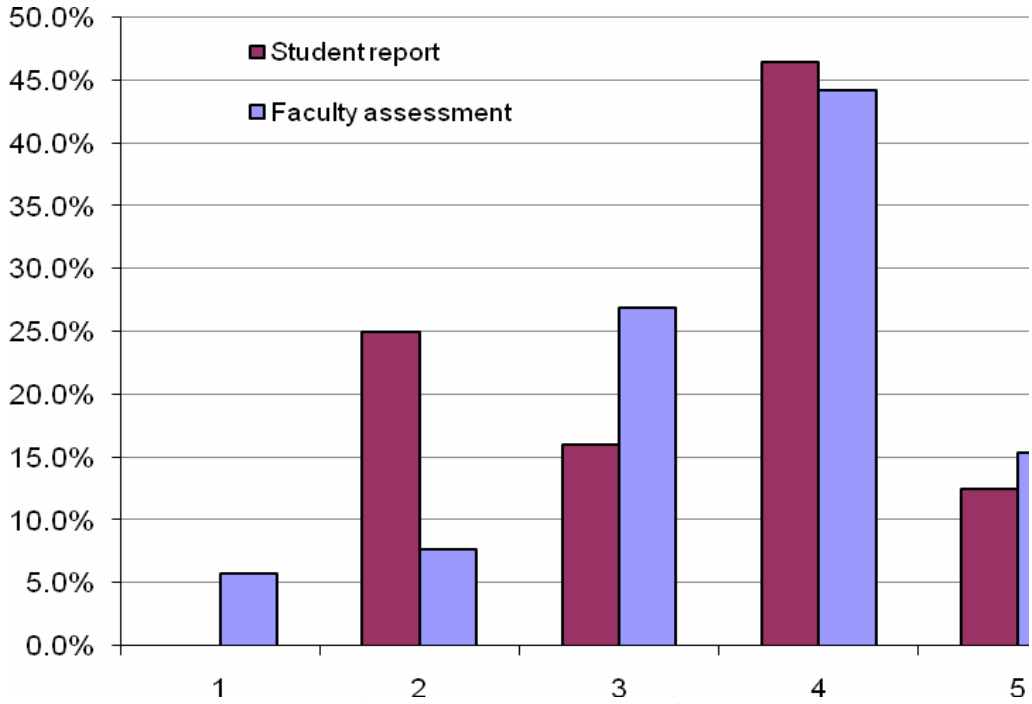


Figure 7. Overall Student Knowledge Increments

Since the 2009 offering of the PCB design exercise was the second offering of this design exercise, it was decided to additionally evaluate the knowledge level of those students who experienced the exercise in 2008. Those eight senior-level students completed only the second portion of the survey. Overall retention of the material was extremely good with all questions

achieving an average score of between 3.0 and 4.0. The overall knowledge score distribution for this group of students is shown in Figure 8.



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Another portion of the questionnaire was designed to assess student confidence in applying the concepts of the design process. The following eleven questions were asked before and after the exercise was performed in order to assess student confidence:

- I can design transistor amplifier circuits incorporating feedback to meet design goals.
- I can design level-shifting circuit stages.
- I can design output (power amplifier) stages
- I can use a circuit simulation tool to enter schematics with footprint geometries used in PCB design.
- I can use a circuit simulation tool as an aid in the analysis of analog electronic circuits
- I can use a PCB design tool.
- I can design appropriate trace widths, trace spacing, via formation, and other geometry-related topics in PCB design.
- I can use Design Rule Checkers for PCB design.
- I can generate PCB reports in Gerber and other formats.
- I can construct electronic circuits and verify performance characteristics experimentally.
- I can write a PCB test plan with verification test procedures**.**

The confidence score was based on the following scale:

1 = No Clue, I have no idea if I can apply the concept
2 = Low, I have heard of the concept, but have little confidence that I can apply it
3 = Moderate, I think I understand the concept, but am unsure about applying it.
4 = High, I am fairly sure I understand the concept and am fairly sure I can apply it.

5 = Superb, I am very confident that I understand the concept and can apply it to a new problem

The distribution of student responses on their confidence in applying the concepts of the course material is given in Table V for each statement on the questionnaire. A histogram with the students' aggregate confidence in applying the concepts of the PCB design exercise material is shown in Figure 9. Students reported a wide range of initial confidence ranging from average confidence scores of 1.2 (use of design rule checkers) to 3.6 (construct and verify performance). The initial overall average confidence score was 2.22. After the design exercise the average confidence jumped to between 2.6 (design of level shifting stages) and 4.6 (use of a PCB design tool). The final overall average confidence score was 3.67: an average confidence increase of 1.45 points. One year after the design exercise, the "senior" students remained highly confident with an overall average confidence score of 3.57 points.

Table V. Confidence in applying the concepts statements with student responses pre-experiment and post-experiment with tabulated incremental changes.

Confidence Statements student responses	When	Distribution					Incremental Change								
		1	2	3	4	5	-4	-3	-2	-1	0	1	2	3	4
I can design transistor amplifier circuits incorporating feedback to meet design goals.	pre	1		3	1						2	2		1	
	post			2	2	1									
I can design level-shifting circuit stages.	pre	3	1		1					1		3	1		
	post		2	3											
I can design output (power amplifier) stages.	pre		2	3						1	1	1	2		
	post		1	2	1	1									
I can use a circuit simulation tool to enter schematics with footprint geometries used in PCB design.	pre		2	3							1	3		1	
	post			2	2	1									
I can use a circuit simulation tool as an aid in the analysis of analog electronic circuits.	pre	1	1	1	1	1					2	1	1	1	
	post				4	1									
I can use a PCB design tool.	pre	2	1	1		1					1		2	1	1
	post				2	3									
I can design trace widths, trace spacing, via formation, & other geometry-related topics in PCB design.	pre	4		1								1	1	2	1
	post			1	3	1									
I can use Design Rule Checkers for PCB design.	pre	4	1									4			1
	post		3	1		1									
I can generate PCB reports in Gerber and other formats	pre	3	2									3	1		1
	post		1	3		1									
I can construct electronic circuits and verify performance characteristics experimentally	pre			3	1	1					3	2			
	post			1	3	1									
I can write a PCB test plan with verification test procedures	pre	4	0	0	1	1					1		1	2	1
	post			1	3	1									

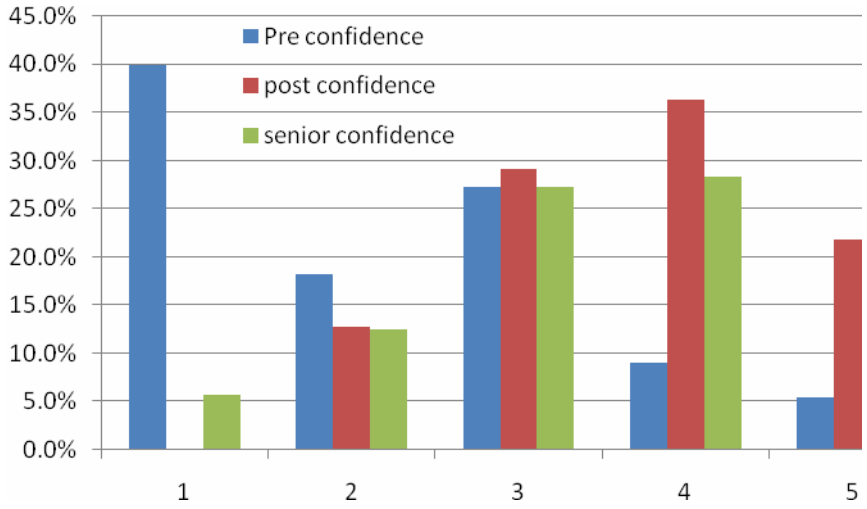

Figure 9. Student Confidence Levels

A summary of the individual student incremental change in confidence scores is also shown in Table V. On individual confidence questions, students reported significant incremental gains. Construction and verification of circuits (the question with the highest beginning confidence level) experienced the lowest average incremental gain (0.4) while the question relating to PCB design geometries achieved the highest average incremental gain (2.6). A histogram of the overall individual confidence increments is shown in Figure 10.

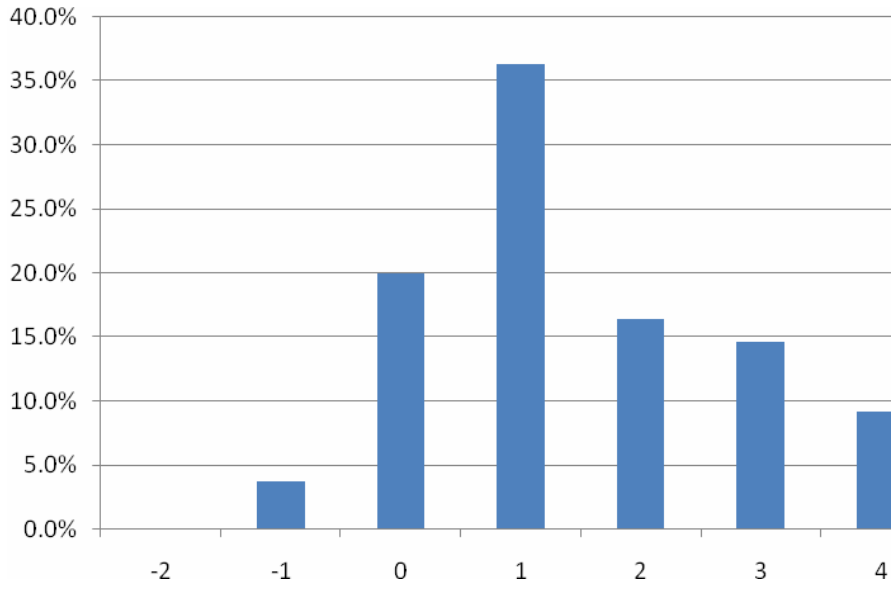

Figure 10. Overall Student Confidence Increments

VI. Summary

The development of a meaningful student laboratory experience in PCB design using the instructor as the fabricator met all its goals. Students were able to progress through all phases of the circuit design process including schematic capture, layout design, assembly, and test. The department was able to limit its purchases for this experiment by releasing to a PCB fabricator only one layout design.

Assessment of student learning showed a significant increase in both student knowledge and student confidence in the application of that knowledge. On a 5-point scale, overall student-reported knowledge increased by 2.79 and overall student confidence increased by 1.25 points. Faculty assessment of knowledge, as measured by scoring short answers to knowledge statements, correlated well with student report and showed an average increase of 2.85.

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