AC 2011-1484: DEVELOPMENT OF AN INPUT POWER FACTOR CORRECTED VARIABLE SPEED MOTOR DRIVE SYSTEM FOR THE ELECTRIC MOTOR DRIVES COURSE

Shiyoung Lee, Pennsylvania State University, Berks Campus

Dr. Shiyoung Lee is an Assistant Professor of Engineering Technology at Penn State Berks. He has many years of industrial experiences as a Senior Power Electronics Design Engineer with various industries before joining the college. Since Dr. Lee's major research area is in Power Electronics, his primary research interest will be the development of software configurable and fully digital controller for the three-phase permanent magnet brushless motor drives. The MATLAB/Simulink based control algorithms will be studied and developed. Other research interests include, but are not limited to the following topics: efficient power converter topologies, input power factor correction, switched reluctance motor drives, alternative energy production, such as solar energy and wind power generation, and digital power processing for numerous industrial, medical and defense applications. He has published numerous papers through ASEE, IJME, EMCW, and IEEE in the Power Electronics area. He is a Senior Member of IEEE and member of ASEE, ATMAE and IAJC.

Development of an Input Power Factor Corrected Variable Speed Motor Drive System for the Electric Motor Drives Course

Abstract

An active input power factor correction (IPFC) is introduced as a front-end converter for the variable speed induction motor drive (IMD) system. This paper provides the involvement of the system power quality which involves a high power factor (PF) and low total harmonic distortion (THD). The necessity for efficient utilization of generated electrical energy is growing in order to optimize the usage of utility power plant capacity. Moreover, awareness of minimizing harmonic contamination in the electric power line is rising due to the increased use of electronic equipment powered by an ac-to-dc bridge rectifier with large filter capacitors and/or a switch-mode power supply (SMPS). The variable speed motor drive (VSMD) saves more electrical energy than the fixed motor drive under the assumption that both are operating on the same load factor. Almost all of the small VSMDs have no IPFC circuits to save their production costs. Emerging applications of fractional horsepower IMDs - such as compressors, appliances, blowers, hand tools, and heating, ventilating, and air-conditioning (HVAC) - invoke the urgency of studying the effects of the IPFC on the VSMDs. A three-phase inverter-fed IMD with a single-phase source and an active IPFC circuit is proposed in this paper to study the impact of IPFC circuit experimentally. The foremost subject in the study of an input PF corrected VSMD are the effects of an IPFC circuit on overall system efficiency and input PF. Empirical comparisons between the conventional bridge rectifier circuit and IPFC circuit in terms of PF and efficiency against motor speed are developed. The overall system performance with an IPFC circuit is better than the system performance without it in terms of harmonic contents and PF. The system efficiency, however, shows marginal inferiority with an IPFC circuit because the front-end IPFC circuit and the three-phase inverter are connected serially. It should be emphasized that the IMD with IPFC is desirable in utilizing the generated electrical energy effectively and minimizing the harmonic contamination. The developed system may be useful as a hands-on experiment for the Electric Drives course. In conclusion, various teaching components are defined with the developed IPFC-IMD system.

Introduction to IPFC VSMD

One of the most active research and development areas in the power electronics field is VSMD. As power semiconductor devices become cheaper, faster, and more reliable, the use of energy saving VSMDs in industry and residential applications has been increasing. VSMDs utilizing induction and dc motors make up the majority of industrial and domestic drives. Although these VSMDs require an initial investment and generate current harmonics, they provide significant improvements in performance such as better control, wider speed ranges, soft start, and enormous energy savings in various kinds of applications. The selection of VSMDs is an application-specific matter. There are many factors to be considered when we select VSMD systems, including cost, output torque, speed ranges, performance, and power ratings.
The emerging requirement in the VSMD application for drawing near sinusoidal current from the utility and less harmonics injection into the utility lines is the motivation for investigating the

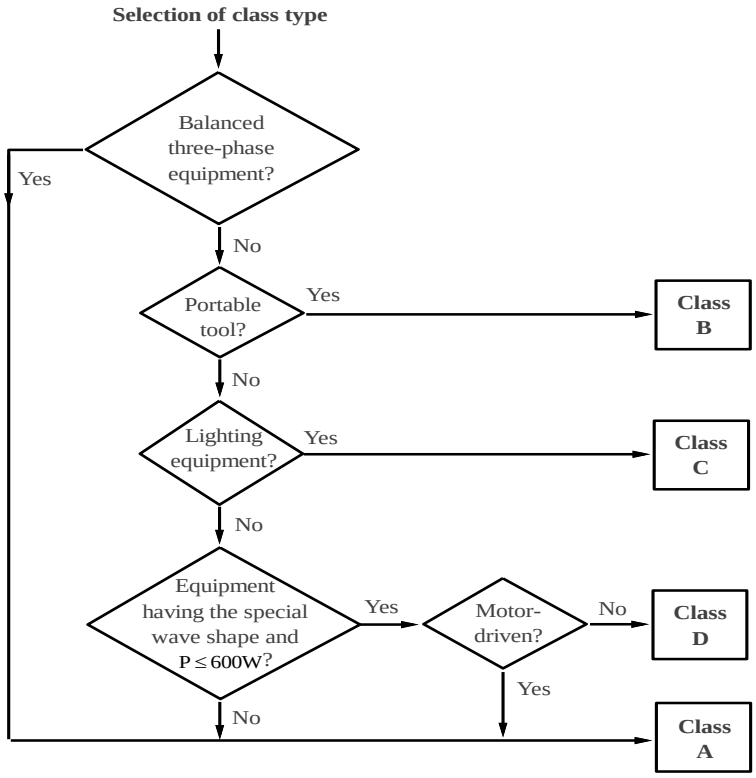
PF-corrected motor drive system. The impact of IPFC on system efficiency and power converter ratings will be studied for high volume but low-cost applications such as washers, dryers, refrigerators, freezers, hand tools, and process drives. The power ratings for most of these high volume applications are less than one-horsepower.

All off-line VSMDs have rectifiers and storage capacitors in their front-ends to get dc voltage from an ac power source. This input circuitry lowers the PF of the VSMD systems and pollutes ac power systems. The PF is the ratio of real power in watts to apparent power in volt-amperes (VA). The PF becomes unity when the input ac current and voltage are sinusoidal and in phase. In an off-line VSMD system, the input current is distorted and even out of phase with input voltage, the power factor is less than unity, and less real power is transmitted to the load. However, the rms input current is increased due to the harmonic currents plus the current required by the load must still be carried, thus requiring the wiring of the ac power system to be heavier and more expensive than necessary[1].

The most common problem that disturbs ac power systems is caused by electric motors operating in industries. The inductive component of the motors causes the ac current to lag the ac voltage. This results in a low power factor. Assuming the loads are linear, the power factor can be corrected to near unity by connecting a bank of capacitors across the ac power line. The low PF gives rise to a number of serious problems in VSMD systems. The size of the input fuses and circuit breakers of the input circuitry must be increased. The distorted input current waveform, which causes interference with other equipment, must be filtered to reduce the magnitudes of harmonic frequencies. Consequently, to increase the output power from ac power systems, it is necessary to correct the PF. This substantially reduces peak and rms input current and makes it possible to achieve higher output power.

With the proliferation of nonlinear loads such as SMPSs, standards agencies around the world are developing requirements for harmonic contents of the electronic power conversion systems to reduce the overall distortion on the main supply line. One of these standards is the IEC 1000-3-2 (same as EN 61000-3-2 published in 1995 and the latest version of IEC 555-2 published in 1982)[2] from International Electrotechnical Commission (IEC) to set the limits for input harmonic currents in the electrical equipment. The standard describes general requirements for testing equipment as well as the limits and the practical implementations of the test. For the purpose of harmonic current limitation, the standard divides electrical equipment into four classes as shown in Figure 1. Each class has different harmonic current limits. The balanced three-phase equipment and other electronic apparatus which is excluded one of three classes are included in the Class A classification. To apply a Class D limit, the following two requirements should be satisfied:

- Input power should be less than 600 W.
- Input current waveshape of each half cycle is within the envelope shown in Figure 2 for at least 95% of the duration of each half period.



Note. Motor-driven: Phase Angle Controlled

Figure 1. Flowchart for class determination of electrical equipment by IEC 1000-3-2 standards

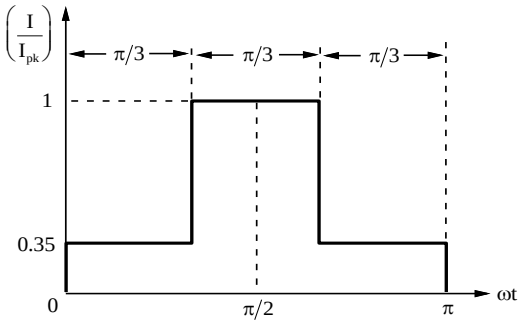


Figure 2. Class D waveform envelope

The center line in Figure 2 coincides with the peak value of the input current. The second requirement implies that the waveform having a small peak outside the envelope is considered to fall within the envelope. In Class D limits, for equipment with input power greater than 75 W, relative limits (mA/W) should be applied; otherwise, absolute limits will be applied.

The specified limits of the IEC 1000-3-2 standards are applicable to electrical equipment having an input current up to 16 A per phase with nominal voltages of 230 V at 50 or 60 Hz single-phase, and the harmonic currents of interest are from the 2^{nd} to 40^{th} harmonic.

Table 1
Original harmonic current limits for Class A and D equipment
by the IEC 1000-3-2 Standards.

	Class A	**Class D**	
	Absolute limit (P > 600 W)	Relative limit (P > 75 W)	Absolute limit (P ≤ 75 W)
Harmonic order (n)	Maximum permissible harmonic current (A)	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
Odd Harmonics			
3	2.30	3.4	2.30
5	1.44	1.9	1.14
7	0.77	1.0	0.77
9	0.40	0.5	0.40
11	0.33	0.35	0.33
13	0.21	Use following equations	
15 ≤ n ≤ 39 (Class A)	0.15 × 15/n		
13 ≤ n ≤ 39 (Class D)	Use preceding equation	3.85/n	0.15 × 15/n
Even Harmonics			
2	1.08	-	
4	0.43	-	
6	0.30	-	
15 ≤ n ≤ 39 (Class A)	0.23 × 8/n	-	

The appliance VSMDs fall into the Class A or D category, depending on whether they use phase-angle controlled VSMD, and their input power range is less than or greater than 600W. The VSMDs, which are investigated in this study, have front-end rectifier circuits to convert ac voltage into dc voltage. The ac input current of the VSMD has pulse type waveform which falls into the Class D envelope regardless of the magnitude of its input power because the pulse current is normalized based on its peak value. If the input power of a VSMD is over 600W, a Class A limit should be applied. Otherwise, Class D limit will be applied. Therefore, in this study, only the Class A and D limits are employed to verify the effects of IPFC and IEC 1000-3-2 standards, as shown in Table 1.

Although the IEC 1000-3-2 standards have different designations, such as EN 61000-3-2 for the European Union published by CENLEC (European Electrical Standardization Committee) and BSEN 61000-3-2 for the United Kingdom, all versions have same IEC standard.

Single-Phase IPFC Topologies

The study of IPFC topologies is limited to the single-phase version in this study because most of the appliance VSMD is powered by a single-phase utility source. The classification of single-phase off-line IPFC topologies for VSMDs[3-12] is shown in Figure 3. Among these IPFC topologies, low frequency active, resonant and isolated types are not considered in this study.

A passive IPFC[4] is more reliable than an active IPFC because no active devices are utilized. However, a passive PFC has bulky capacitors and inductors operating at line frequency, and it is sensitive to the line frequency, line voltage, and load. Therefore, this method is not suitable for appliance drives.

The most popular active IPFC method is the boost topology. This topology is a universal solution from SMPS to small-motor drive applications. It has a smooth input current because an inductor is connected in a series with the power source, showing a low level of conducted electromagnetic interference (EMI) noise. This topology has a high output voltage that is greater than the peak input voltage. The overload and start-up current cannot be controlled in this topology because there is no series switch between the input and output path. Also, isolation between the input and output cannot be easily implemented.

The buck type IPFC has lower output voltage than input voltage, and it has a pulsating input current, which generates high harmonics into the power line. This circuit is not practical for low-line input because it does not draw the input current when input voltage is lower than output voltage. Therefore, it has a relatively low power factor compared to the boost IPFC circuit. The buck type IPFC is suitable for charger applications due to its voltage step-down nature.

The SEPIC (single-ended primary inductor converter) IPFC circuit has a single power switch driven at high frequency, as in the boost IPFC topology, but it needs extra inductive and capacitive passive components for energy storage and transfer. The input current of SEPIC is smoothed by employing an inductor in a series with the power source. This circuit can be easily modified to the isolated version.

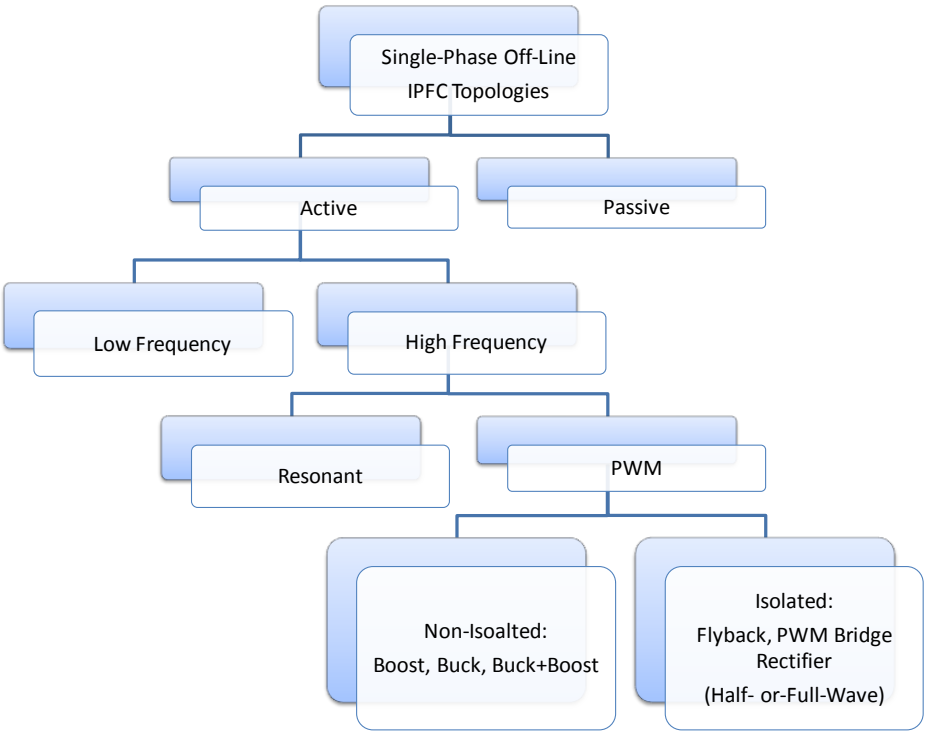


Figure 3. Classification of single-phase IPFC topologies for small VSMD systems

A cascaded converter, which has a buck circuit in the front and boost circuit in the second stage, is introduced[3]. The buck switch is turned on when the input voltage is below the output voltage. This causes the circuit to operate as a boost converter. When the input voltage is higher than the output voltage, the boost circuit is stopped and the buck circuit restarts. This converter can supply step-up or step-down outputs; thus, it can operate for wide input range.

Another non-isolated IPFC topology is the pulsewidth modulation (PWM) bridge rectifier. This topology can also supply step-up or step-down outputs as the buck-boost circuit. The PWM bridge rectifier circuit needs two or four power switches to make a unity power factor because it employs half- or full-bridge configuration. It also needs a more complicated control than the boost topology, but for high power applications, it may be a good candidate.

Proposed IPFC-IMD System

The proposed IPFC-based IMD system for this study is shown in Figure 4. Note that the IPFC circuit is replaceable with a single-phase diode rectifier bridge circuit for comparison study. IPFC has both input current and voltage feedbacks to obtain the sinusoidal input current. The output voltage sensing circuit rejects the adverse effect of load variation in the dc link voltage. The inverter power circuit is made of MOSFET devices and operates at 2.78 kHz with PWM control. The control strategy is a constant V/Hz with the offset adjustment. In this study, the offset is fixed at a value equal to the rated stator resistive voltage drop. The drive has an inner rotor speed feedback loop to control the slip speed. This limits the stator current effectively over the range of speed variation.

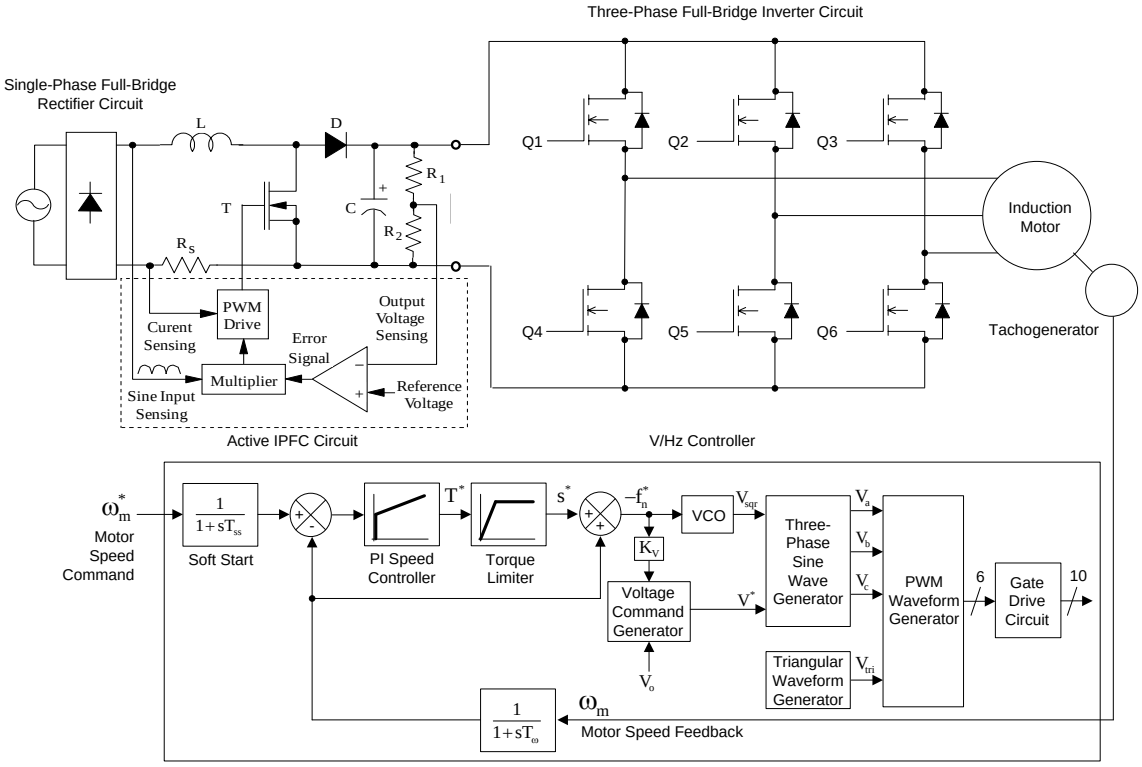


Figure 4. Proposed IPFC-IMD system

Principle of Operation of the Boost IPFC Circuit

The principle of operation of the boost IPFC circuit, which is selected for VSMD system, is explained in this section. The predicted efficiency of the boost PFC preregulator is obtained with derived analytical equations and compared with experimental results. The harmonic contents in the input current of the boost PFC circuit are compared with the IEC 1000-3-2 standards.

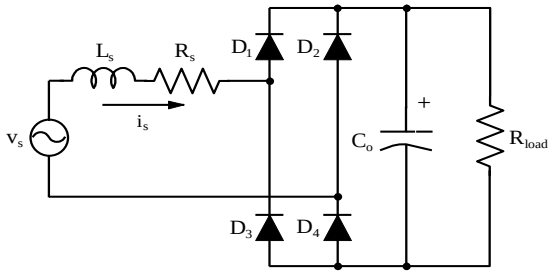
In a VSMD, the ac utility input voltage must be converted to dc with a rectifier circuit as shown in Figure 4. This circuit has the advantages of simplicity, low cost, high reliability, and no need of control. However, it has the disadvantages of low PF due to the presence of rich harmonics in its current and high peak current magnitude as shown in Figures 5(i), (ii), and (iii). This relationship is shown in Figure 5 which is obtained by PSpice simulation of a single-phase diode bridge rectifier circuit and is normalized to the peak value.

The input circuitry of an off-line VSMD consists of rectifier diodes to convert ac into pulsating dc and filter capacitors to smooth the pulsating dc voltage, as shown in Figure 4. This input circuitry presents rich harmonic currents to ac power systems that are quite different from motor loads because it appears as a nonlinear load to ac power systems. In the input circuitry, ac current pulses occur because the filter capacitor remains charged to nearly the peak value of the ac input voltage. During most of each half cycle of input voltage, the rectifier diodes remain reverse biased; thus, no current flows. Because the filter capacitors partly discharge during each half-cycle, the input voltage exceeds the capacitor voltage for a short time near the peak value of the input voltage. As the input voltage surpasses the capacitor voltage, the input current begins to flow abruptly into the capacitor. After the capacitor is charged to near the peak value of the input voltage and the input voltage begins to decrease, the input current falls to zero.

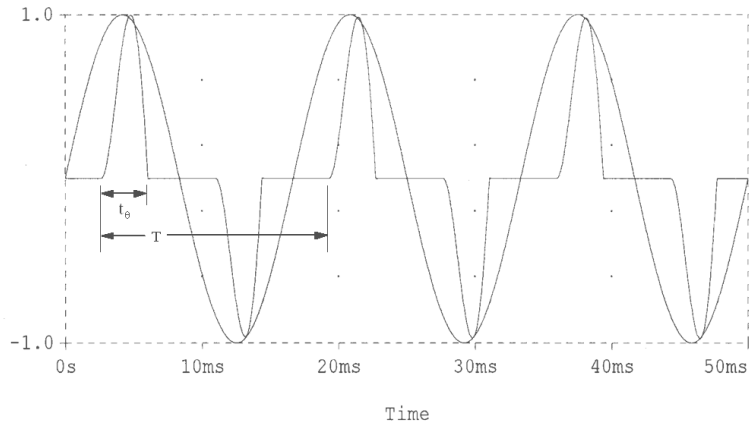
The input current pulse has a high peak value and is extremely distorted with respect to a sinusoidal waveform. It contains high amounts of harmonic components. These harmonic currents cause added current drain from the ac power line, imposing the need for higher wiring capacity and contributing to the resultant low power factor. Any harmonic currents except the fundamental component do not deliver the power to the load. However, these harmonic currents increase the total line current more than actually required by the user. As a result, it requires a higher current rating of the wire and circuit breaker in the utility resulting in additional installation cost to the utility company.

As required by various standards, the line harmonics produced by a VSMD must be below certain limits, which increase the input PF. The high PF is desirable to both the user and the utility company because it is possible to get maximum power from an ac service outlet and to utilize the generated power efficiently and cleanly. It is possible to reduce the wiring and power transformer losses in the utility network with high PF. With increasing demand for more power usage and better power quality from a standard power line, the IPFC circuit will become an integral part of a VSMD in the near future.

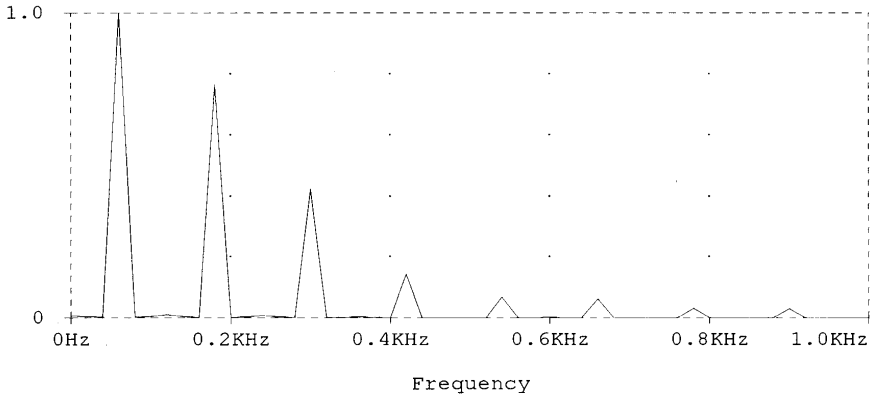
The boost IPFC circuit is an economical solution to comply with the regulations. It can be implemented with a dedicated single chip controller; therefore, the circuit becomes relatively simple with a minimum number of components. The boost inductor in the boost PFC circuit is in



(i) A single-phase diode rectifier circuit with capacitor



(ii) Normalized input ac voltage, v_s and current, i_s.



(iii) Normalized harmonic spectrum of current i_s.

Figure 5. Analysis of current harmonic contents in the diode bridge rectifier circuit with capacitor by PSpice

a series with the ac power line; thus, the input current does not pulsate, so the conducted EMI at the line is minimized. This allows the size of the EMI filter and the conductors in the input circuit to be reduced. This topology inherently accepts the wide input voltage range without an

input voltage selector switch. For example, the UC3854 PF controller chip from Texas Instruments[13] accepts an input voltage of 75 – 275 V ac and a frequency of 50 – 400 Hz. It can't limit overcurrent at start-up or fault conditions because there is no switch between the line and the output. The output voltage of a boost PFC circuit should be higher than the peak value of the maximum input voltage. Even though this is a simple topology, it must be designed to handle the same power as the main power converter. Only the single-phase boost PFC circuit operating in the continuous inductor current mode will be discussed in this study.

The simplified block diagram of the boost IPFC circuit is shown in Figure 4. This circuit has two control loops. One is the fast acting internal current loop, it defines the input current shape to be sinusoidal and make it in phase with the input voltage. The other is the external voltage loop which regulates the output dc voltage. The voltage loop should not react to the 120 Hz rectified mains variations, so its bandwidth is lowered to 10 to 20 Hz. The current loop usually has a bandwidth frequency of less than one tenth of the switching frequency.

Derivation of the Steady-State IPFC-IMD System Model for Analysis

Steady-state loss models of the induction motor, load, inverter, IPFC circuit, and bridge rectifier are developed. The load and its requirements are known and, hence, they constitute the starting point for the steady-state performance computation. Using the rotor speed and the load power with the inverter output voltage equation, induction motor equations, and load equations, the overall system equations are assembled.

As the stator phase current is given, the inverter losses can be computed with switching and conduction loss equations. The input power to the inverter can be calculated with the inverter losses combined with the induction motor input power. The sum of inverter input power and the IPFC circuit losses give the input power from the ac mains supply. The solution of the input power leads to a complete solution of the steady-state performance of the IPFC-IMD system.

Experimental Setup

The voltages, currents, and powers are measured at the system input, IPFC circuit output, dc link, inverter output, and dc motor output as shown in Figure 6.

The symbols with I are the ammeters, with V are the voltmeters, and with W are the wattmeters. From the experimental data containing the friction and windage losses, the parameters of the induction and dc machines are calculated, and, in conjunction with other measurements, the induction motor output is determined for each operating point. Then, the system and induction motor efficiencies, system input PF, system line current, motor currents, and IPFC circuit efficiencies are calculated from the empirical data.

The speed of the induction motor is varied from 500 r/min to 3,000 r/min (0.87 p.u.), and the output power at the base speed (3,450 r/min) is 1 hp. The empirical data are obtained for the system with and without the IPFC circuit, and by keeping the input system voltage at 230 V.

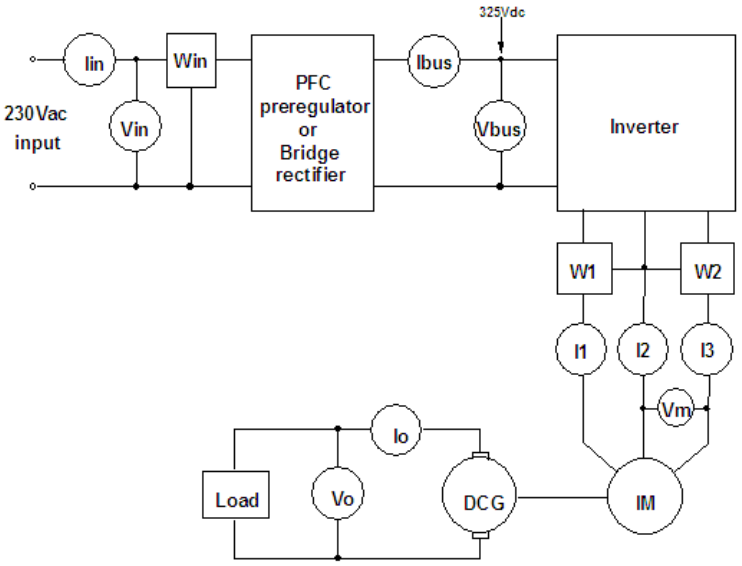


Figure 6. Experimental setup for the proposed IPFC-IMD VSMD system

Discussion on Experimental Results

Input Current Harmonics in the Boost IPFC Preregulator

The sample input current waveform and its harmonic contents of the prototype 2 kW IPFC preregulator with 1400 W load are shown in Figures 7 and 8. The steady-state harmonics are measured by the fast Fourier transformation (FFT) with rectangular windowing function. The input ac current closely follows the sinusoidal voltage waveform, as designed. The PF of this operating point is calculated as 99% with the following equations;

$$Power\ \ Factor = \frac{Real\ Power}{Apparent\ Power} = \frac{V_{rms} \cdot I_1 \cdot \cos\phi}{V_{rms} \cdot I_{rms}} = \frac{I_1}{I_{rms}} \cdot \cos\phi \qquad (1)$$

$$I_{rms} = \sqrt{I_1^2 + I_3^2 + \cdots + I_n^2}\ \text{, A} \qquad (2)$$

where, V_{rms} is the ac input rms voltage, I_{rms} is the input ac current, I_1 is the fundamental component of I_{rms} and $\cos\phi$ is the phase angle between input ac voltage and the fundamental current.

The harmonic spectra of the input current with IPFC circuit are intensely improved compared with one in the bridge rectifier circuit with capacitor shown in Figure 5(i). This validates the effectiveness of the IPFC.

Experimental waveforms of the system input current and induction motor stator current at 1 p.u. speed and load torque are shown in Figures 9 and 10, for both the bridge rectifier- and IPFC-based VSMD systems along with their frequency spectra.

The IPFC-IMD system is free of harmonics in the system input current. The induction motor stator currents are practically the same with minor variations in their frequency spectra. The speed variation hardly affects these waveforms.

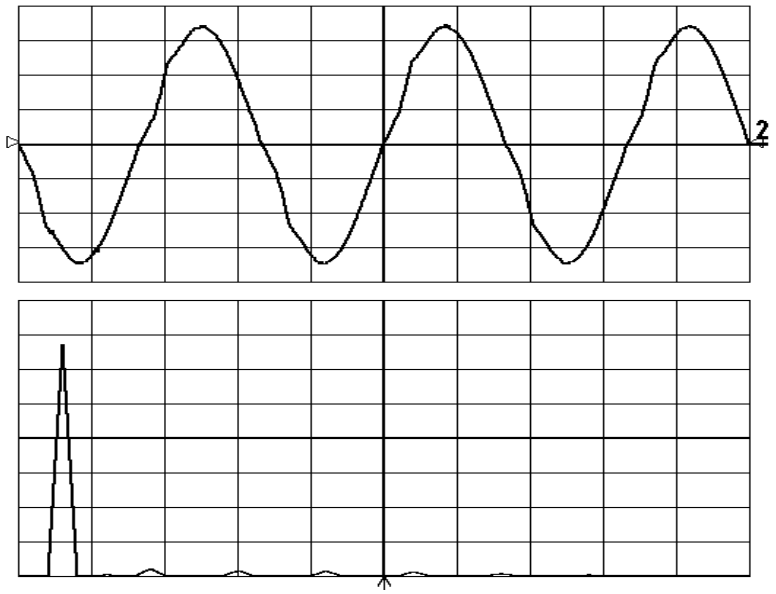


Figure 7. Experimental waveforms of the 2 kW PFC preregulator with 1.4kW load (Top) input current (5A/div , 5ms/div) (Bottom) input current harmonic spectra (2.5A/div , 0.1kHz/div)

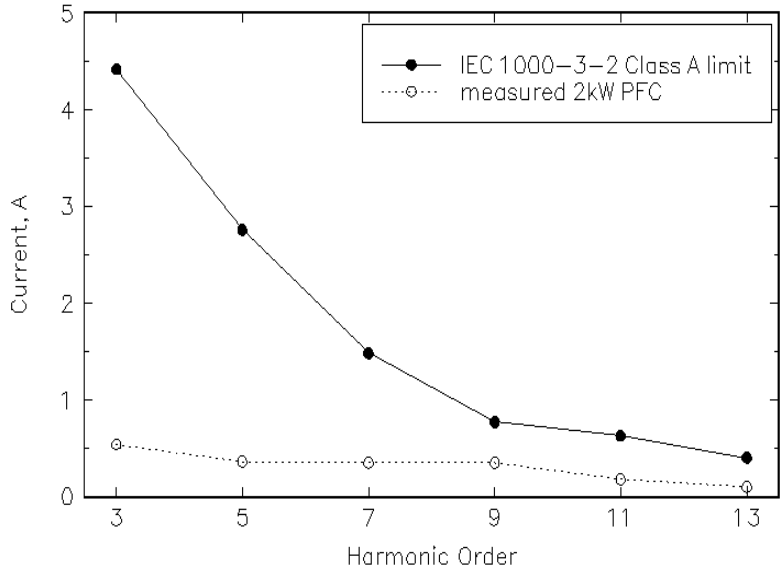


Figure 8. Comparison of measured input current harmonic spectra from Figure 8 with modified IEC 1000-3-2 Class A harmonic current limit

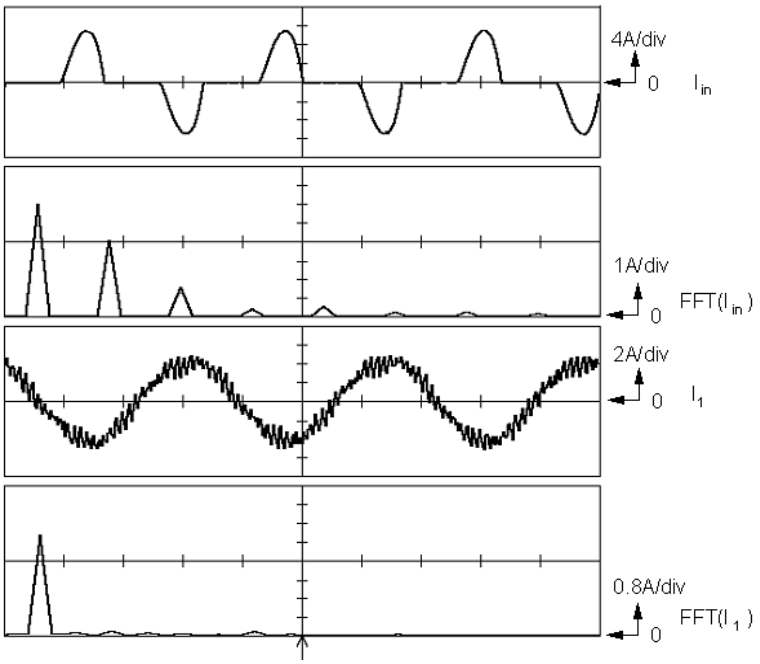


Figure 9. System ac input current (top) and motor stator current (bottom) and their FFT with diode bridge rectifier front-end

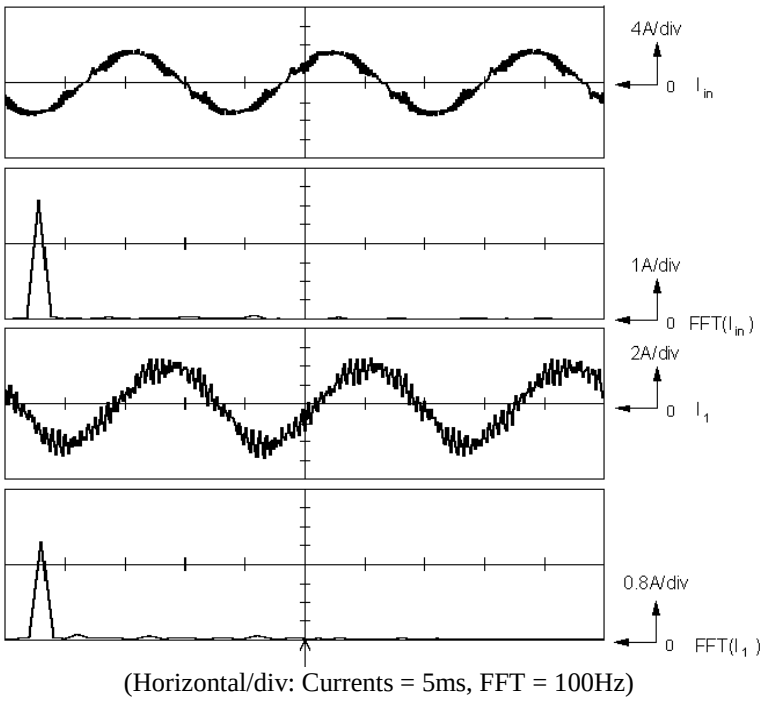


Figure 10. System ac input current (top) and motor stator current (bottom) and their FFT with IPFC circuit

Efficiencies of the IPFC-Based IMD System

In Figure 11, the efficiency of the 2 kW IPFC circuit employed in this study shows evenly above 95% over the entire output power range. The predicted efficiency matches closely with the measured one over the entire power range. This validation of the derived loss models is practically useful to estimate losses in the boost IPFC preregulator.

The system input PF, input current, and overall IMD system efficiency versus motor speed for both with and without the IPFC preregulator are shown in Figures 12(i), (ii), and (iii) for the friction load. The IPFC-based IMD shows higher input PF over the entire speed range than one with a non-IPFC system. Hence, the IPFC-IMD system requires lower input current to generate the same output than a non-IPFC system. The benefit of less input current requirement is noticeable over 0.4 p.u. speed.

The non-IPFC system shows a higher system efficiency up to 0.75 p.u. speed, but the IPFC-based system shows higher system efficiency beyond that speed with friction load. This is attributed to the fact that the stator current decreases with the decreasing stator voltage of the non-IPFC system. The non-IPFC system efficiency is approximately 2 to 4 % higher than that of the IPFC-based system.

The system and motor efficiencies are very poor for speeds lower than 0.3 p.u., as the output is very small in this region and the losses are multiple times that of the output in that speed range. The usual variation of speed range is 0.4 to 1 p.u. for the friction load; hence, the low speed operation with low efficiency may not be of immense importance.

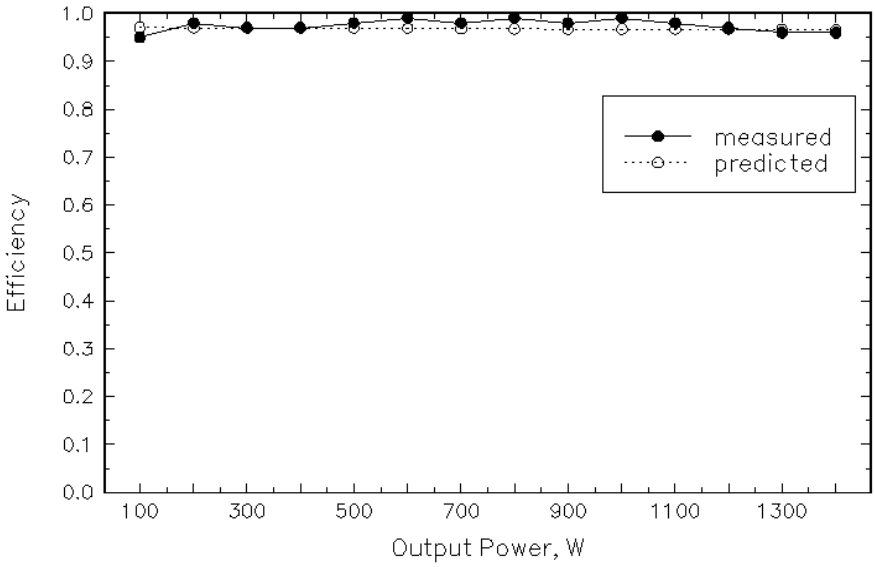
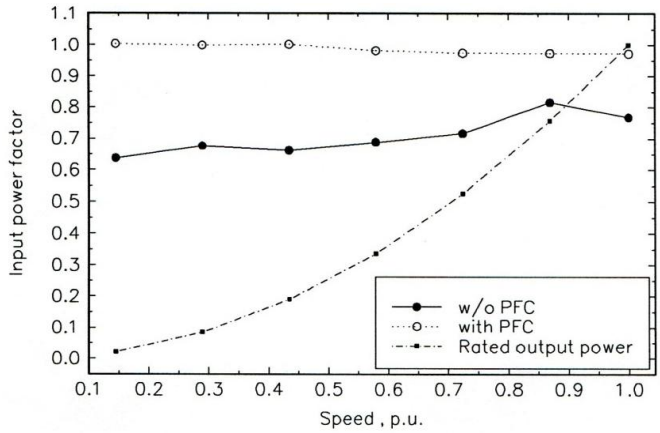
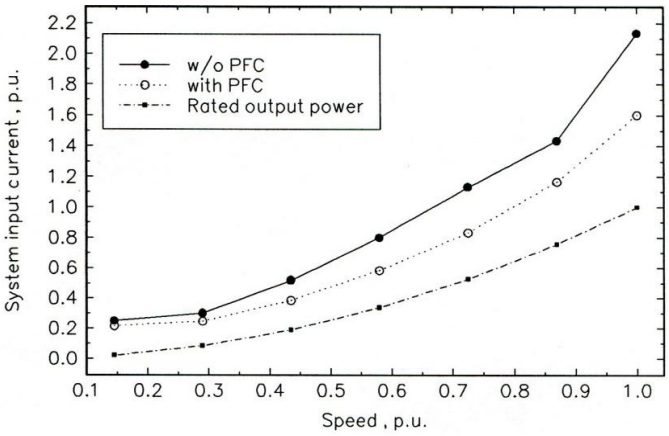


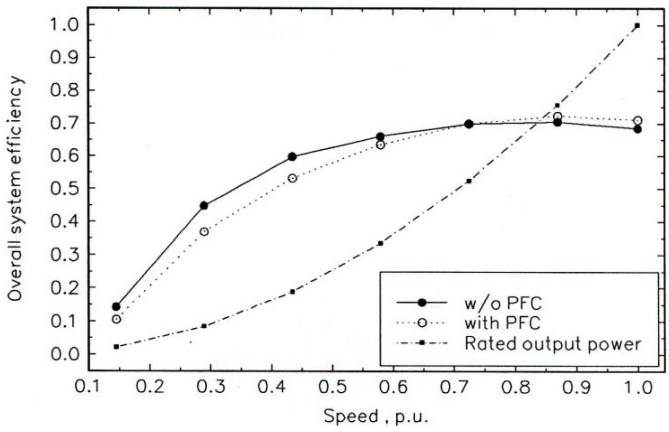
Figure 11. Measured and predicted efficiencies for the developed 2kW boost IPFC preregulator



(i) System input PF



(ii) System input current



(iii) Overall system efficiency

Figure 12. Input PF, input currents, and system efficiency with and without IPFC for IMD system with friction load

Integration of Developed IPFC-IMD System to EMET 325 Electric Drives Course

EMET 325 Electric Drives is a required course for junior-level students in the Electro-Mechanical Engineering Technology (EMET) baccalaureate degree program at Penn State Berks and other commonwealth campuses. The purpose of the course is to familiarize students with the function, operation and control of practical electrical actuators used in industrial systems to manipulate equipment and products. The primary focus will be on the kinds of units typically found in automated production and manufacturing systems. Devices covered include permanent magnet and separately-excited dc motors; stepper motors; ac induction and permanent magnet synchronous (or brushless dc) motors; and ac synchronous motors. Capabilities, control methods, power converter systems, and practical applications and limitations for each device are covered.

Students are expected to have the following topical knowledge upon entering this course: Satisfactory completion of courses in basic electric circuits and analog electronics. Students are expected to use computers to perform calculations, to conduct out-of-class problem assignments, and to prepare engineering graphs/tables to report analysis results. Knowledge of word-processing, mathematical (viz., Excel, Matlab, Mathcad, etc.), and electronic analysis software (viz., PSpice, MultiSim, MicroCap, etc.) is expected.

Suggested topic list consists of following:

- *Fundamentals of Magnetic Circuits and Materials*: Basics of Ampere's law, magnetic induction, magnetic forces, and magnetic materials properties.
- *Ac Motor Operation*: electrical characteristics and mechanical performance of ac induction and permanent magnet synchronous (a.k.a. brushless dc) motors.
- *Dc Motor Operation*: electrical characteristics and mechanical performance of dc permanent magnet motors and separately excited dc motors.
- *Stepper Motors*: stepper motor principles; motor types; switching and drive methods; starting, stopping, and speed control.
- *Switched Reluctance Motors*: switched reluctance motor principles; motor types; switching and drive methods, and speed control.
- *Practical Dc Drive Systems*: Dc control concepts and methods; Dc drive technology; drive specification, selection and ratings; Dc drive control methods. Torque, speed, and position control.
- *Practical Ac Drive Systems*: Ac drive control concepts and methods, universal drives; open-loop, closed-loop, and servo systems; starting, stopping, and torque, speed, and position control.
- *Power Conversion Devices*: concepts, functions, operation, capabilities, and limitations of Dc-Ac, Dc-Dc, Ac-Dc, and Ac-Ac power converters.

This course contributes to the following EMET program outcomes:

- Students will have an ability to design systems, components, or processes for broadly-defined electro-mechanical engineering technology problems appropriate to program educational objectives.

- Be able to use electrical/electronic devices such as amplifiers, motors, relays, power systems, and computer and instrumentation systems for applied design, operation, or troubleshooting electro-mechanical systems.

The following may be useful methods for assessing the success of this course in achieving the intended outcomes listed above:

- Traditional exams and out-of-class problem assignments covering lecture materials generally can be used to assess many of the expected outcomes.
- Some classroom and out-of-class exercises should require students to conceptualize, design, and present electric-drive based systems. Where appropriate, these exercises should involve team-based work among students. Effectiveness and practicality of designs should be key components of the evaluation of students' work.

If design projects are used, students should be required to develop, follow, and periodically progress report on their design developments. Evaluation should consider the quality of the presentations and the professionalism demonstrated by the students.

The proposed IPFC-IMD system, which is implemented mainly with discrete components, provides various teaching components to enhance EMET 325 Electric Drives course. It will be useful for the practical dc and ac motor drive systems sections. Possible teaching topics and their brief explanations are listed below:

- *IEC1000-3-2 harmonic standard*: Complete explanation of the standard is made to apply to the VSMD system in terms of classification of the standard, limitation of the magnitudes of harmonic contents, and compliance testing methods.
- *Classification of the single-phase IPFC for small VSMDs*: Various types of active IPFC circuitry are classified and reviewed to select a proper topology for the fractional horsepower VSMD application.
- *Boost active IPFC circuit design and implementation*: Insight into the design and implementation of the boost active IPFC circuit is completely described based on UC3854 high performance IPFC controller chip from Texas Instruments Inc.
- *Operation of the single-phase diode bridge rectifier*: PSpice simulation of the single-phase diode bridge rectifier is shown with its harmonic spectra.
- *Three popular load types*: Constant, friction, and fan type loads are explained, and the experimental results with the friction load are discussed.
- *Modeling of the steady-state IPFC-IMD system*: Various models of the single-phase bridge rectifier, IPFC circuit, three-phase inverter, induction motor, and load are derived for the steady-state analysis of the IPFC-IMD system and non-IPFC with a diode bridge rectifier IMD system.
- *Electromagnetic Interference (EMI) or Radio Frequency Interference (RFI)*: The EMI/RFI issue directly relates to the clock and PWM frequency in the proposed IPFC-IMD system. The proper management of the printed circuit board (PCB) design is required to minimize the EMI/RFI effect. It is important to address this issue and examine the PCB design. The grounding technique, the use of power and ground planes in a multilayer PCB design, and the elimination of the ground loop may be worthy topics for discussion.

Conclusion

The three-phase downstream inverter can be applied to any type of three-phase VSMD. Various teaching components for the electric drives course are justified from the proposed IPFC-IMD system. The system steady-state model for both the bridge rectifier- and IPFC-based IMD has been formulated, and a steady-state computational procedure has been developed. The model has been experimentally verified with a 1-hp laboratory prototype IPFC-IMD system and is found to be fairly accurate. A comparison between the non-IPFC and IPFC-based system is made for the friction-type load. The non-IPFC system is preferable in terms of the system efficiency; however, the IPFC-based system is highly preferable for the minimum input harmonics and maximum PF. The IPFC-IMD system may not be quite as attractive due to additional cost, even though there are operational advantages with a stiff dc bus voltage for a possible flux-weakening. These results may enhance course materials for any motor drives courses.

Bibliography

[1] Ned Mohan, "Electric Drives an Integrative Approach," MNPERE, 2003.
[2] Agilent Technologies, "Compliance Testing to the IEC 1000-3-2 (EN 61000-3-2) and IEC 1000-3-3 (EN 61000-3-3)," AN1273, 2000.
[3] B. Singh and S. Singh, "Single-phase power factor controller topologies for permanent magnet brushless DC motor drives," The Institution of Engineering and Technology Power Electronics, vol. 3, issue 2, pp. 147-175, 2010.
[4] Supratim Basu and Math Bollen, "A Novel Common Power Factor Correction Scheme for Homes and Offices," IEEE Transactions on Power Delivery, vol. 20, no. 3, July 2005, pp. 2257-2263.
[5] Gwi-Geun Park, Kee-Yong Kwon, and Tae-Woong Kim, "PFC Dual Boost Converter Based on Input voltage Estimation for DC Inverter Air Conditioner," Journal of Power Electronics, vol. 10. No. 3, pp. 293-299, May 2010.
[6] Wanfeng Zhang, Guang Feng, Yan-Fei Liu, and Bin Wu, "A Digital Power Factor Correction (PFC) Control Strategy Optimized for DSP," IEEE Transactions on Power electronics, vol. 19, no. 6, pp. 1474-1485, November 2004.
[7] Freescale, "3-Phase AC Induction Motor Control with PFC Using MC9S08MP16," Design Reference Manual, DRM115, Rev. 0, 11/2009.
[8] M. Aware, S. Tarnekar, and A. Kothari, "Unity power factor and efficiency control of a voltage source inverter-fed variable –speed induction motor drive," IEE Proceedings Electrical Power Application, vol. 147, no. 5, pp. 422-430, September 2000.
[9] Jui-Yuan Chai and Chang-Ming Liaw, "Development of a Switched-Reluctance Motor Drive with PFC Front End," IEEE Transactions on energy Conversion, vol. 24, no. 1, pp. 30-42, March 2009.
[10] Hung-Chun Chang and Chang-Ming Liaw, "Development of a Compact Switched-Reluctance Motor Drive for EV Propulsion with Voltage-Boosting and PFC Charging Capabilities," IEEE Transactions on vehicular Technology, vol. 58, no. 7, pp. 3198-3215. , September 2009
[11] Hiralal Suryawanshi, Abhishek Kulwal, Madhuri Chaudhari, and Vijay Borghate, "High Power Factor Operation of a Three-Phase Rectifier for an Adjustable-Speed Drive," IEEE Transactions on Industrial electronics, vol. 55, no. 4, pp. 1637-1646, April 2008.
[12] Jürgen Reinert and Stefan Schröder, "Power-Factor Correction for Switched Reluctance Drives," IEEE Transactions on Industrial electronics, vol. 49, no. 1, pp. 54-57, February 2002.
[13] Philip Todd, "UC3854 Controlled Power Factor Correction Circuit Design," U-134, Texas Instruments Incorporated, 1999.
[14] R. Krishnan, "Electric Motor Drives – Modeling, Analysis, and Control," Prentice Hall, 2001.