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Attached Learning Model for First Digital System Design Course in ECE Program

Seemein Shayesteh P.E., Indiana University Purdue University - Indianapolis

Lecturer in the department of Electrical and Computer Engineering at Purdue School of Engineering at Indianapolis

Dr. Maher E. Rizkalla, Indiana University Purdue University - Indianapolis

Dr. Maher E. Rizkalla: received his PhD from Case Western Reserve University in January 1985 in electrical engineering. From January 1985 until August 1986 was a research scientist at Argonne National Laboratory, Argonne, IL while he was a Visiting Assistant Professor at Purdue University Calumet. In August 1986 he joined the department of electrical and computer engineering at IUPUI where he is now professor and Associate Chair of the department. His research interests include solid state devices, applied superconducting, electromagnetics, VLSI design, and engineering education. He published more than 175 papers in these areas. He received plenty of grants and contracts from Government and industry. He is a senior member of IEEE and Professional Engineer registered in the State of Indiana

Lauren Christopher, Electrical and Computer Engineering, IUPUI

Dr. Lauren Christopher attended Massachusetts Institute of Technology, where she received her S. B. and S. M. in Electrical Engineering and Computer Science in 1982, specializing in digital signal processing and chip design. She worked at RCA's David Sarnoff Research Labs in the 1980's developing chips for early digital television, and in the 1990s joined Thomson Consumer Electronics, where she led the first DIRECTV receiver design. She received her PhD from Purdue University in 2003, developing image segmentation techniques in 3D medical ultrasound images toward automatic cancer detection. In 2010, Dr. Christopher has been inducted into the Consumer Electronics Hall of Fame for her work in leading the development of the DIRECTV set top box. Dr. Christopher joined IUPUI in 2008, and is currently heading the 3D imaging and VLSI research in the Electrical and Computer Engineering Department. Her research continues the 3D medical image registration and image segmentation from her PhD work. Her research interests include real-time 3D systems, 3D image sensors and 3D image processing algorithms.

Dr. Zina Ben Miled, ECE Department, Purdue School of Engineering and Technology, Indiana University Purdue University - Indianapolis

Zina Ben Miled received her B.S. in Computer Engineering from Oregon State University in 1988, her M.S. and Ph.D. also in Computer Engineering from Purdue University in 1990 and 1997, respectively. She has co-authored several technical papers in journals and conference proceedings and holds one patent. Her research interests include data analytics, knowledge discovery, data models and computational frameworks. She was the recipient of the Indiana Women in High Tech Award and the National Science Foundation Career Award.

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I. Introduction

Digital hardware design in industry is increasingly dependent on Hardware Description Languages (HDLs) for implementing complex digital systems. Many universities have incorporated Hardware Description Language in their curriculum [1-4]. In our institute also to better follow and anticipate the newest industry trends, the first digital system design course in the electrical and computer engineering (ECE) department was updated in 2009 to include the topics of Hardware Description Language and Field Programmable Gate Array (FPGA). This Sophomore-level course, "Introduction to Digital System Design," is a 4 credit-hour course consisting of a lecture and a lab and is a required course in the electrical engineering and the computer engineering programs. The course was revised in Fall 2014 to enhance students' hands-on HDL and FPGA design learning experience. The revised course's goals were the following:

1) Improving students' performance in the Introductory course;
2) Enhancing students' interest in future digital design courses and improving student retention;
3) Preparing students adequately for upper level courses with HDL components: Senior level "Advanced Digital System Design," , Graduate level "Advanced Systems on a Chip (SoC) Designs" and "MOS VLSI Design" courses;
4) Enabling electrical and computer engineering students to engage in senior design projects involving HDL and FPGA's;
5) Preparing graduate as well as undergraduate ECE students for research opportunities in the area; and
6) Providing hardware design tools for computer science major students who choose to take the course as one of their elective courses.

This paper addresses the revised course structure and its impact on students' learning.

II. Revised Course Structure

As mentioned, this Sophomore-level 4 credit-hour course, "Introduction to Digital System Design," is a required course in the electrical engineering and the computer engineering programs. The lecture and lab sessions are closely synchronized in the attached learning model. The lecture topics include number systems, VHDL, CMOS logic, combinational logic design, sequential logic design and arithmetic circuits. The new course structure after the revision is shown in Table 2. For comparison purposes, the course structure prior to the revision is shown in Table 1.

Course Upgrade

Newer FPGA hardware, the Xilinx Nexys4, was purchased and the labs were upgraded based on the new hardware. In the older version of the course (Table1), Hardware Description Language learning was incorporated in only 1/3 of the labs. Furthermore, it was supported with very little HDL in-class learning. The revised-course covers HDL in the lecture as well as several laboratory sessions (Table 2). Furthermore, a design project that integrates various components of the course was added. To address HDL in-class learning, a new textbook was selected that better supports

the use of HDL in logic design and emphasizes the relationships between HDL statements and the corresponding digital hardware. It is also worth noting that, in order to prepare students for the subsequent laboratory exercises, an introduction to VHDL is covered earlier in the revised course.

Table 1: Course Structure before Course Revision in 2014

Lecture Topic / Week	Lab / Week
Introduction, Logic, CMOS Transistors	
Basic Gates, Boolean Algebra	Lab 1 - Xilinx Board
Canonical Forms, K-maps	Lab 2 - Logic Gates
4 Variable K-Maps, Quine-McCluskey	Lab 3 - Logic Minimization
Logic Hazard, AOI Gates, HDL Introduction	
Logic Technologies	Lab 4 - VHDL
Programmable Devices, Tristate	Lab 5 - Combinational Circuit
Numbers, ALU	
Latches, Flip-flops	Lab 6 - Combinational Arithmetic
Timing Registers, HDL,	Lab 7 - Propagation Delays
FSM Counters & Basics	Lab 8 - Memory
FSM Mealy & Moore	
FSM Minimization and PLD's	Lab 9 - Sequential Circuit

Table 2: Course Structure after Course Revision in 2014

Lecture Topic / Week	Lab / Week
Introduction, Number Systems	
Basic Gates, HDL Introduction	Lab 0 - Vivado Tutorial
CMOS Transistors, Boolean Algebra,	Lab 1 - Modeling in VHDL
Canonical, Min / Maxterms	Lab 2 - Numbers in VHDL
Karnaugh-Maps, Quine-McCluskey	Lab 3 - Multi-output Circuits
Multi-Level Gates, Simulation	Lab 4 - Tasks, Functions, Test-bench
Programmable Devices, Latches, Flip-flops	Lab 5 - Latches and Flip-flops
Registers and Counters,	Lab 6 - Registers and Counters
Analysis of Clocked Circuits, State Graphs and Tables	Lab 7 - Timing
State Tables / State Assignment	Lab 8 - IP Blocks
Sequential Circuit Design	
VHDL for Sequential Logic	Lab 9 - Design Projects: Counters, Timers, and Clocks
Arithmetic Circuits, SM Charts	Lab 10 - Finite State Machines

VHDL Lab Structure

The labs are conducted weekly and are based on the Xilinx University curriculum [5]. There are a total of 11 lab sessions. The lab typically starts in the 2nd week of classes with a Vivado tutorial. Each lab has its own report template which lists exactly what is expected for that lab report submission. Each lab starts with approximately a 10-minutes introduction about the lab's objectives and methodology. The lab work is done individually. However, students are encouraged to collaborate. Each lab manual includes background information and step-by-step

instructions for the students. In most labs, a VHDL skeleton code is provided and each student is responsible for completing this code to achieve the required design. The students are asked to prepare before the lab by reading the background material for each lab session and thinking about the design and the underlying components. The students then carefully follow the step-by-step instructions while in the lab and demonstrate board functionality at the end of each lab session.

The students have access to the Xilinx Nexys4 schematic and users' manual, and are asked to review them. The course instructor typically familiarizes the students with the board during the lab introductory lecture. Furthermore, the early homework assignments focus on exploring the Xilinx board. This exercise gives the students sufficient background knowledge that enables them to successfully conduct the subsequent laboratory exercises.

As shown in Table 2, the students start the laboratory component of the course with a tutorial that guides them through the design flow using the Xilinx Vivado software in order to create a simple digital circuit by using VHDL. In this tutorial, the students create a Vivado project, analyze the provided VHD and XDC source files, perform RTL analysis, simulate the design using the XSIM simulator, synthesize the design, implement the design, perform the timing simulation and finally verify the functionality in hardware using the Nexys4 board.

The first laboratory module consist of four structured labs related to combinational logic design. In lab 1, students learn about VHDL behavioral and structural models for multiplexers. In lab 2, students use behavioral modeling to convert a 4-bit binary input number to a 7-segment display on the board, and use structural modeling to create a 4-bit ripple carry adder. In lab 3, students complete the provided behavioral model VHDL codes to design 3-to-8 line decoder and an 8-to-3 priority encoder. In lab 4, students learn about functions, procedures and test-benches. They specifically develop a test-bench to verify the 4-bit ripple carry adder functionality using the ripple carry design (and its associated full adder module) that they developed in lab 2. This latter lab is important because it allows the students to reflect back on a previous lab exercise and enables the reinforcement of previously acquired knowledge. In all of the above mentioned labs, the students not only simulate the design, but also synthesize and implement the design, generate the bit stream, and download it onto the board in order to demonstrate its functionalities.

The second laboratory module also consists of four structured labs starting with lab 5. This module focuses on sequential circuit design. During the lecture, students are taught about hierarchical component progression from CMOS NOR-gates to SR-latches, gated D-latches and finally D flip-flops as highlighted in Figure 1.

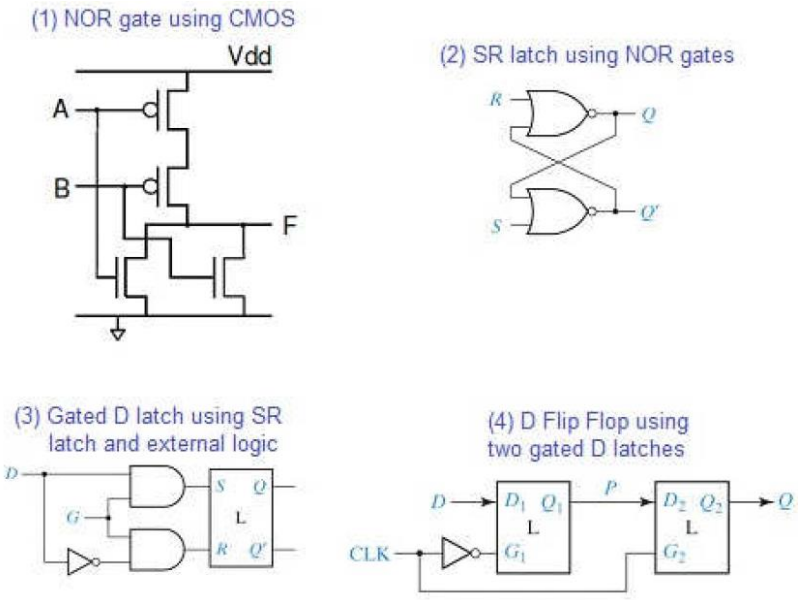


Figure 1: Hierarchical Component Progression

In lab 5, students model latches and flip-flops using behavioral modeling. For each segment of this lab, as in the previous module, students synthesize the design, view the RTL schematic, develop a test-bench to test and validate the design, simulate and implement the design and verify the functionality in hardware. In lab 6, students learn about modeling registers and counters. In lab 7, students learn about the various language constructs such as the **if** statement and **case** statement in behavioral modeling. Finally, in lab 8 students learn about the Architectural Wizard and the IP Catalog system available in the IP Catalog of the Vivado tool. They use the Architectural Wizard to generate a 5 MHz clock from the on-board 100 MHz clock source and use the IP Catalog to generate a simple 4-bit counter core which counts up from 0 to 9. The IP Catalog is a powerful tool that includes various functional blocks enabling higher productivity. For instance, the students use the IP catalog to design a one-second pulse generator by dividing the 5 MHz clock discussed earlier using a clock divider and behavioral modeling. Another example consists of instantiating the 4-bit counter core generated using IP Catalog system twice to create a two digit BCD counter which counts up every second. The Architectural Wizard is used to generate a 5 MHz clock and then behavioral modeling is used to generate 1 Hz precise signal to drive the counters. For this segment, the BCD to 7-degment display .vhd file from lab 2 is used as the starting point.

Lab 9 is the design project and it builds upon the knowledge of the Architectural Wizard, the IP Catalog (lab 8) and the earlier labs. Students are given three design projects ideas and are asked to choose one for implementation, using VHDL. Typical examples for design projects are a stop watch timer, a count down timer, and a real time clock. The students can use the two functional circuits to generate a desired clock frequency and to generate counters to design any of the three design choices.

Finally in lab 10 students learn how to model Mealy and Moore finite state machines. Students design a sequence detector implementing it first as a Mealy machine and then as a Moore machine.

III. Results and Discussion

Improved Students' Performance:

Each student's grade percentage in the course is determined based on the student's performances in homework assignments, quizzes, exams, and labs. There are typically twelve homework assignments, four quizzes, three midterm exams, one final exam, and eleven labs. The typical grading scheme is shown below:

Table 3: Grading policy

Three exams	50%
Final Exam (Comprehensive)	20%
Labs (a failed lab results to an F grade in the course)	20%
Homework Assignments and Quizzes	10%

In order to establish a base performance, the average GPA of students prior to taking the course in different semesters were compared as shown Table 4 below.

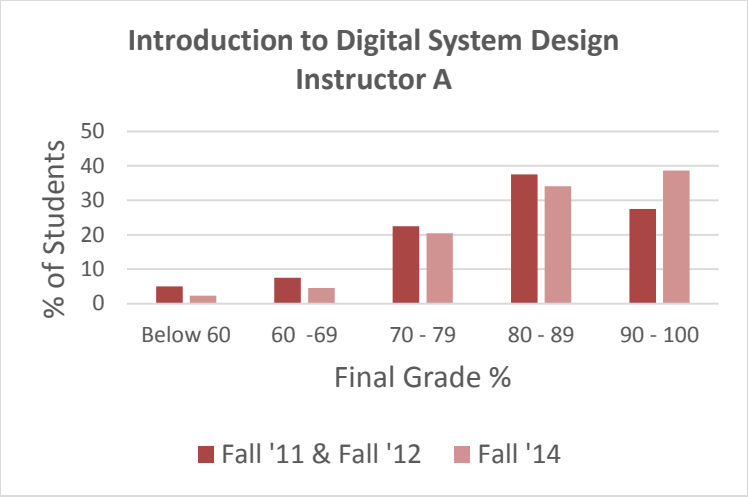
Table 4: Average GPA of students just before taking the course

	Fall 2011 & 2012	Fall 2014	% Difference	Spring 2013	Spring 2015	% Difference
Average Students' GPAs / 4.0	2.9	3.3	+11%	3.0	3.1	+3.8%

Just prior to taking the course, the average GPA of students in Fall 2014 was 11% higher compared to average GPA of students in Fall 2011 and Fall 2012. Similarly, just prior to taking the course, the average GPA of students in Spring 2015 was 3.1% higher compared to average GPA of students in Spring 2013.

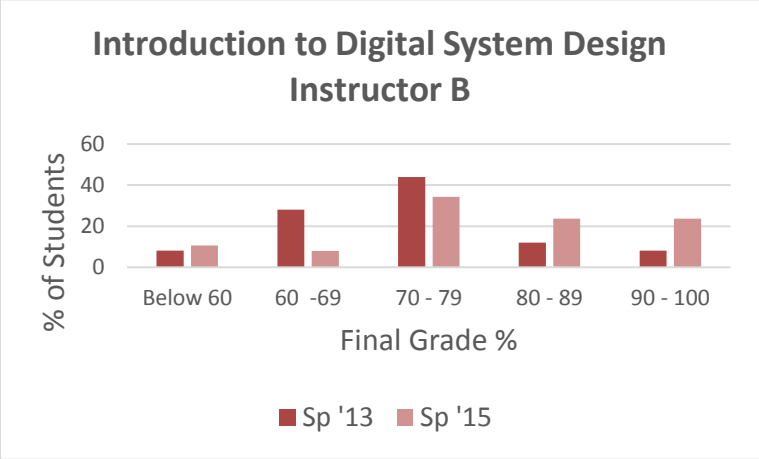
Figure 2 shows the percentages of students in different grade categories in Fall 2011 and Fall 2012, compared to Fall 2014, when instructor A taught the introduction digital system design course. Figure 3 shows the percentages of students in different grade categories in Spring 2013, compared to Spring 2015, when instructor B taught the introduction course. The revised course was first taught in Fall 2014. As shown in the figures, after the course was revised, there was a significant increase in the percentage of students with a percentage grade ranging between 90 -100 with both instructors A and B.

Figure 4 combines the data for both instructors and compares the percentages of students in different grade categories before and after the course revision. This overall data shows the shift in the grades of students towards higher percentages. Indeed the number of students with scores greater than 90% increased by 59%. Conversely, the number of students with scores less than 70% decreased by 60%.



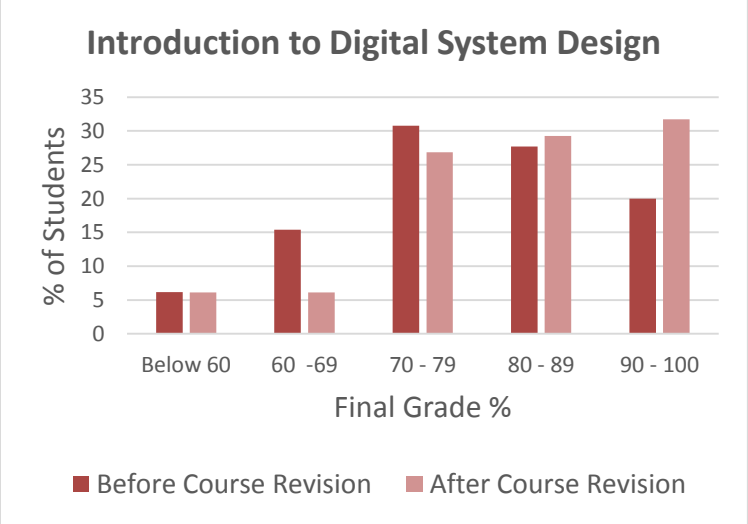
% of Students Final Grade %	Fall '11 & Fall '12 (40 Students)	Fall '14 (44 Students)	% Diff
Below 60	5	2	-55
60 -69	8	5	-39
70 - 79	23	20	-9
80 - 89	38	34	-9
90 - 100	28	39	**40**

Figure 2: Percentages of Students in Different Grade Categories (Instructor A)



% of Students Final Grade %	Sp '13 (25 Students)	Sp '15 (38 Students)	% Diff
Below 60	8	11	32
60 -69	28	8	-72
70 - 79	44	34	-22
80 - 89	12	24	97
90 - 100	8	24	**196**

Figure 3: Percentages of Students in Different Grade Categories (Instructor B)



% of Students Final Grade %	Before Course Revision (65 Students)	After Course Revision (82 Students)	% Diff
Below 60	6	6	-1
60 -69	15	6	-60
70 - 79	31	27	-13
80 - 89	28	29	6
90 - 100	20	32	**59**

Figure 4: Percentages of Students in Different Grade Categories (Combined)

In summary, the data shows that after the revised course was presented in Fall 2014 and Spring 2015, student performance improved with both instructors. In addition to the above benefit, other positive performance indicators were observed. These are listed below.

High student satisfaction:
A large percentage of the students (74%) indicated that the VHDL labs helped them better learn digital electronics as it relates to both combinational and sequential logic circuit design. Also, 74% of students indicated they feel comfortable using VHDL and FPGAs in future projects.

High interest and performance in the follow-up undergraduate course:
The next course in the series is the 3 credit-hour "Advanced Digital System Design," which is offered once every Fall semester in the department. The course covers advanced topics in digital design including Boolean logic, logic optimization, VLSI and ASIC design, design simulation, placement and routing, logic synthesis, FPGA implementation and design flow, and Verilog and VHDL coding. The Advanced Course enrollment doubled in Fall 2015 compared to Fall 2014. In addition, 54% of students achieved an A grade in the Fall 2015 Advanced class, compared to 36% of students in Fall 2014 Advanced class. These indicators seem to show improved retention of the material achieved through the revised course.

IV. Conclusion and Future Work

This paper shows that the restructuring and enhancement to a required sophomore digital system design course have led to improved students' performance and increased students' interest in the subject. The course provides students with the essential theoretical background and hands-on experience in digital design. The course was revised to include modular, well-structured, hands-on HDL and FPGA design learning experience.

V. References

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