

AC 2008-2139: EXTENSIVE USE OF ADVANCED FPGA TECHNOLOGY IN DIGITAL DESIGN EDUCATION

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Extensive Use of Advanced FPGA Technology in Digital Design Education

Abstract

The design tools, methods, and technologies used in industry to design digital hardware evolve quickly and continuously. Since the inception of wide-spread CAD tool use to define digital circuits around 40 years ago, revolutionary tool changes have occurred every 5 to 10 years. Although many of the foundational concepts are relatively unchanged, educational programs must nevertheless keep pace with technologies in common use in order to produce graduates who are competitive in the marketplace.

A study conducted at Rose Hulman Institute of Technology measures changes in student performance when all students have unlimited access to state of the art design tools and hardware systems. Data are collected from surveys, exams, and course assignments such as project and lab reports. Quantitative data are analyzed by comparison to historical data gathered from student groups that did not have unlimited access to hardware systems, and qualitative data are used to determine the subjective quality of each student's experience. Specific outcomes include: assessing whether the overall learning process was improved; whether students have a better knowledge of modern technologies and design methods; whether their comprehension of founding concepts has improved or faltered.

Introduction

The design tools, methods, and technologies used in industry to design digital hardware to evolve quickly and continuously. Revolutionary tool changes occur every 5 to 10 years, and educational programs must keep pace with technologies in common use in order to produce graduates who are competitive in the marketplace. Today, although roughly 60% of University-based educational programs in the United States use some form of programmable logic devices and associated CAD tools, many programs use them only in more advanced or project-based courses. Further, the vast majority of undergraduate programs that use programmable logic technologies provide only limited access to these technologies in 2 or 3 hour weekly lab sessions. During these lab sessions, students have to master new concepts previously taught in theoretical lectures, use laboratory equipment to build experiments, develop software and hardware debugging skills and learn how use complex CAD tools. The limitation of this traditional approach is the fact that 2 or 3 hours of lab sessions prove insufficient to meet all the lab objectives. Consequently, students do not develop the right skills required by industry.

A new approach, where every student owns his or her own programmable hardware system and CAD tool suite, is now feasible due to decreased costs. Programmable logic systems capable of hosting circuits that range in complexity from simple logic circuits to complete 32-bit microcomputer systems can be purchased for less than \$100, and required CAD tools are free. A study currently underway at Rose Hulman Institute of Technology, Electrical and Computer Engineering Department, is attempting to measure the effect on student learning when students own their own programmable hardware system, and have unrestricted access to programmable technologies.

Starting in the winter quarter of the 2007-2008 academic years, every student enrolled in the Junior-level Digital Systems course at Rose Hulman Institute of Technology (RHIT) was given an FPGA-based circuit board. The Nexys board, available from DigilentInc was used because it is self-contained and USB powered, making it suitable for use with a notebook computer, and because it contains a large FPGA (a Xilinx Spartan 3-400), several memories, and several I/O devices. Each student was allowed to keep the board for the entire quarter, and each student downloaded a free copy of the Xilinx CAD software that provides schematic and HDL circuit definition tools, a simulator, a synthesizer.

The study is being conducted by the instructor and the Office of Research, Planning, and Assessment (IRPA) at RHIT. The study measures changes in student performance when all students have unlimited access to state of the art design tools and hardware systems, with the primary goal of determining whether the extensive use of programmable technologies improves the overall learning process, the attainment of specific knowledge and skills, and the proper use of technological tools. Secondary outcomes include more qualitative measures, including student's perceptions of the relevancy and completeness of their knowledge and skills, their enthusiasm and willingness to learn, and their overall impression of their educational experience.

Data are collected from surveys, exams, project reports, and laboratory assignments. Quantitative data are analyzed by comparison to historical data gathered from student groups that did not have unlimited access to hardware systems, and qualitative data will be used to determine the subjective quality of each student's experience. Specific outcomes include an assessment of whether the overall learning process was improved; whether students gained a better knowledge of modern technologies and design methods; and whether their comprehension of founding concepts has improved or faltered.

In addition to the program currently underway at RHIT, other universities are also adopting the model that every student must own their own programmable logic board and CAD tools. For example, at Washington State University, in Pullman, students have been purchasing their own FPGA-based circuit boards for use in several classes since 2002. In the Introductory Logic course (EE 214), the instructor has documented in unpublished data that mean scores on standardized tests increased 18% in the second semester of 2002, the first semester that all students were required to purchase their own programmable logic board. Since 2002, design projects in that class have required more complex and open-ended designs, and virtually all class assignments involve building and demonstrating physical circuits. Over that time period, students have reported greater confidence in their skills, greater satisfaction with their learning experience, and an increased willingness to engage in further learning opportunities. The course coordinator also reports that fewer TA and laboratory technician hours are required to keep all equipment running.

In a second example at the Technical University of Cluj –Napoca, Romania, students in graduate level design classes in the 2004 and 2005 academic years had access to programmable logic boards only during 2-hour laboratory sessions, but students in the 2006 and 2007 academic years were given unrestricted access to their own boards. The class required simpler, introductory design projects in the first half of the class, and then more complex individualized projects in the

second half of the class. In unpublished data collected over the four years, the class instructor noted two distinct trends. First, student groups with their own boards (in the latter two years) had increased failure rates, increasing from about 20% to about 30%. Second, the students who completed the course in the 2006 and 2007 academic years completed far more challenging projects than students in the 2004 and 2005 academic years, and they showed more interest, more creativity, more general knowledge, and more often extended their designs beyond the initial requirements.

Digital Logic Sequence of courses at Rose Hulman Institute of Technology

ECE 333-Digital Systems course is the second course in the Logic Design sequence of courses at RHIT. This course is a required undergraduate junior level course for Electrical and Computer Engineering students. The prerequisite for this course is ECE 130-Introduction to Logic Design course, a freshman level course. ECE 130 provides the students with basic knowledge necessary for designing and analyzing combinational circuits, sequential circuits and Register Transfer Level Systems.

Important course objectives for ECE 333- Digital Systems course include:

- (i) designing synthesizable Verilog HDL code fragments implementing basic combinational and sequential hardware and Finite State Machines
- (ii) implementing Algorithmic State Machines with handshaking
- (iii) understanding the difficulties of asynchronous inputs to a Finite State Machine and how to design circuits to mitigate the problem
- (iv) understanding metastability of digital circuits
- (v) partitioning a system into the control unit and data path unit
- (vi) understanding the importance of functional verification, implementing testing strategies using an HDL based test bench and interpreting the results.
- (vii) understanding the architectures of different Programmable Logic Devices

The present format of the ECE 333- Digital Systems course includes 3 lectures and 3 hours of laboratory per week, during 10 weeks, in a quarter formats. Detailed information about the course can be found in reference ³. Laboratory experiments include use of discrete CMOS logic (1 lab session), programmable GAL ICs (2 lab sessions), programmable logic boards based on Xilinx FPGA Spartan 3 chip (2 lab sessions and a 3 week project) and 2 lab sessions dedicated to analog characteristics of CMOS circuits. Traditionally, working in teams of two, students were checking their FPGA boards for the lab sessions and returned them at the end of the 3 hours lab. For work outside the lab sessions, they were allowed to recheck the boards, having one week to accomplish a specific lab and 3 weeks to finish the project.

The challenges teaching this course are: the mixture of students with different backgrounds, different exposure to digital design related concepts (EE majors versus CPE majors), and the time gap of almost two years since they took their first course in the Logic Design sequence of courses.

The present format of the ECE 130-Introduction to Logic Design course includes 4 lectures week, during 10 weeks, in a quarter formats. Detailed information about the course is given in reference ⁴. This course underwent changes starting two years ago. The traditional use of LogicWork CAD tool was replaced with Digilent boards based on Xilinx Spartan 3 FPGA. Very early in the curricula, at the freshman level, students are introduced to CAD tools such as Cadence NC-Sim for simulation of logic circuits and Xilinx Foundation Tools for implementation of their circuits. They are also introduced to schematics and basic HDL concepts. The changes initiated at the freshman level in the Logic Design sequence of courses at RHIT, are noticed as positive changes, this academic year, at the level of the Digital Systems course. Both courses use similar Digilent programmable boards and the same design flow.

In the Digital Systems course, after mastering all the essential concepts during the first five weeks of the quarter, the concepts are incorporated into a design project, which is an essential part of this course. The projects assigned over the past four years were: Analog-to-Digital Converters, based on the SAR (Successive Approximation Register); Controller for Two-Floors Elevator; Controller for Traffic Lights; Controller for a Pig Game. The degree of difficulty and the specific requirements for the projects were gradually increased over the past four years.

Assessment of the Impact of Extensive Use of FPGA Technology

To assess the effect of adding extensive use of advanced FPGA technology into the Digital Systems course, a research study was conducted by the instructor and the Office of Institutional Research, Planning and Assessment (IRPA) at RHIT. The study was designed to determine if extensive use of programmable logic devices improved the attainment of discipline specific knowledge and skills and the proper use of technological tools. The collected data are both from self-reported (i.e., surveys) and course-based (i.e., exams, projects, etc.) sources and are qualitative and quantitative in nature.

Due to RHIT's small student population and small class size (less than 25 students), a blind study was not possible. Ideally, two sections of the class should be taught in parallel, by the same instructor, one in the traditional way and another one with the new paradigm, but this was not possible due to the limited enrollment. For this reason, multiple assessment techniques are used to gain support for the conclusions of the study. Methods include: exam scores; student survey scores; student survey comments; instructor's surveys. The experiment was conducted at RHIT over the past four consecutive years. The experiment will continue the next academic year also. The course was taught by the same instructor, using the same syllabus, the same textbook¹, and the course was offered regularly each academic year.

A. Methodology

Participants: The assessment involved students in the academic years 2004-2005, 2005-2006, 2006-2007, 2007-2008.

Assessment tools: Exam averages for students in all four years are compared to investigate statistical difference. Surveys were conducted in the final year of the study to investigate the effect of the extensive use of FPGA technology in the course. Surveys contain a quantitative measure to indicate the effect of extensive use of FPGA technology on students' perception of their learning core concepts. Specific comments on the effect of extensive use of FPGA

technology on the students' perception of their learning are achieved by short answer questions on the same survey.

B. Results of the Assessment

B.1. Student Grades

The average of student grades on exams 1 and 2 covering concepts impacted by the use of programmable boards were compared over four consecutive academic years. Exams in all these years were of similar difficulty, to allow the comparison. The winter quarter 2007-2008 represents the quarter when extensive use of FPGA boards was introduced, and the fall quarter 2007-2008 represents the quarter when over 80% of students, mostly juniors, enrolled in the course, had previous experience using FPGA programmable boards and specific CAD tools from the prerequisite course ECE 130- Introduction to Logic Design. Project grades are also presented and explanations for the trend given below.

Table 1
Mean Grade

	Fall 2004- 2005	Winter 2004- 2005	Spring 2004- 2005	Fall 2005- 2006	Winter 2005- 2006	Spring 2005- 2006	Fall 2006- 2007	Winter 2006- 2007	Spring 2006- 2007	Fall 2007- 2008	Winter 2007- 2008
Exam 1	75.63	87.3	73.5	86.68	87.2	88.93	86.1	90.06	91.05	94.5	93.15
Exam 2	68.91	77.85	73.91	88.45	83.5	81.3	87.97	91	88	86	87.15
Project	89	100.65	100.49	97.25	100.63	97.8	102.9	94.3	94.04	96.6	97.13

There no statistically differences over the past three years regarding the exams. There are differences between the academic year 2004-2005 and the following academic years. Possible explanations for the trend are:

- RHIT's students are high achievers, RHIT being a highly regarded engineering school in USA.
- Class size is small, allowing valuable interaction between the students and instructor.
- Starting in the 2005-2006 academic year, extensive functional verification of HDL designs was introduced in the Digital Systems course, improving students performances in this class (as proved by another educational research study conducted at the level of this class ²).
- Students project scores are high due to several reasons. Students were strongly encouraged to add extra features to their projects, (showing creativity and desire of innovation), receiving extra credit for these additional features. Having a completely functional project implemented on the Digilent boards at the end of three weeks dedicated to the project, was a must in order to pass this class. Project topics were carefully selected, to allow students to have fun while mastering important digital design concepts. The degree of difficulty and the specific requirements for the projects were gradually increased over the past four years. A Controller for the Pig Game proves to be very successful this academic year.

The trend of the exam mean grades over the past four years, due to changes in the Digital Logic Sequence of courses, shows that the ECE 333-Digital Systems course is ready for changes in the syllabus, introducing more advanced topics, more difficult exams, and especially project assignments.

B.2. Student Survey Scores

Fifteen students (83% of the total enrollment) enrolled in Digital Systems course participated in the assessment during the 2007-2008 Fall quarter and 29 students (54 % of the total enrollment) participated in at least one portion of the assessment in the 2007-2008 Winter quarter. 24 students (52 % of the total enrollment) completed both surveys in the winter quarter.

As part of the assessment, *pre-* and *post-course* student surveys were designed and implemented. The survey was administered anonymously, meaning that no identifying information was collected with the survey. The *pre-course* survey serves as a baseline for the level of understanding each student came to the course with, while the *post-course* survey assess the level of understanding students left the course with. The pre-course survey contains 12 items. In these items, students indicated their ratings of their *knowledge of* and *confidence in the ability to solve problems* in 12 course concepts. The post-course survey contained these same 12 items as well as items concerning the use of logic boards in the class and the impact on their learning.

Results of the post course surveys from the fall quarter and winter quarter 2007-2008 are presented in table 2. The responses in the knowledge category were greater than the responses in the confidence category. This result is expected since confidence in the ability to solve problems in the area indicates a higher level of understanding than knowledge in the area.

Table 2
Post-Course Survey Means for Fall 2007-2008 and Winter 2007-2008
(Rating Scale: 3 point scale ranging from 0 = none to 3 = high)

Learning Objective	Knowledge		Confidence	
	Fall	Winter	Fall	Winter
Understand architectures of different programmable logic devices	2.00*	2.67*	2.07*	2.58*
Design HDL code fragments that will implement basic hardware elements	2.93	2.83	2.79	2.88
Design Mealy and Moore Finite State Machines	2.73	2.83	2.79	2.79
Understand the concept of Algorithmic State Machines	2.67	2.71	2.64	2.83
Determine what hardware would be synthesized from an HDL code fragment	3.00	2.96	2.93	2.88
Explain the concept of handshaking between Finite State Machines	2.87	2.83	2.71	2.83
Explain the impediments to synchronous design	2.47	2.67	2.36	2.63
Discuss clock skew and metastability of digital circuits	2.47	2.79	2.29*	2.75*
Explain why asynchronous inputs to a Finite State Machine are problematic and how design circuits mitigate the problem	2.47	2.54	2.50	2.50
Design a system using a control unit/data unit partition	2.27	2.63	2.29	2.63
Discuss the concept of functional testing and testing strategies	2.73	2.92	2.57	2.79
Design a HDL based test bench	2.73	2.79	2.71	2.75

Notes: * indicates statistically significant difference between means.

There were three statistically significant differences on post-course items from the fall 2007 to the winter 2008 quarters. There was a statistically significant increase from fall to winter on student ratings of their knowledge of and confidence in “Understand[ing] architectures of different programmable logic devices.” There was also a statistically significant increase from fall to winter on student ratings of their confidence in “Discuss clock skew and metastability of digital circuits.” There is an increase at the knowledge and/or confidence level in different concepts from Fall to winter. Such examples are: “Design a System using a Data Unit/Control Unit partition”, “Design Mealy and Moore Finite State Machines”, Understand the concept of Algorithm State Machines”, “Explain impediments to synchronous design”.

Possible explanations for the trends are:

- Having their own board during the entire quarter to “play with”, definitely helped the students to better understand the architectures of programmable logic devices.
- Working on their project, several students experienced difficulties with asynchronous inputs (using slides switches and push buttons as user inputs). They were forced to think more about the concept of metastability and to try to find solutions using synchronizers (and debouncers). Having their own boards, students were able to split the tasks and work on different aspects of the project, getting a better knowledge of and confidence in these concepts.
- Concepts such as Design a System using a Data Unit/Control Unit partition, Design Mealy and Moore Finite State Machines, Understand the concept of Algorithm state machines were strongly reinforced during lab sessions and especially in the project.

There was a statistically significant increase from pre- to post course survey in the winter on student ratings of their knowledge of and confidence in all course learning objects for winter quarter 2007-2008. In the table3 below are the pre- and post-course mean ratings for these items.

Table 3
Pre- and Post-Course Survey Means for Winter 2008
(Rating Scale: 3 point scale ranging from 0 = none to 3 = high)

Learning Objective	Knowledge		Confidence	
	Pre	Post	Pre	Post
Understand architectures of different programmable logic devices	1.15	2.65	1.25	2.60
Design HDL code fragments that will implement basic hardware elements	1.45	2.80	1.50	2.85
Design Mealy and Moore Finite State Machines	1.30	2.85	1.30	2.80
Understand the concept of Algorithmic State Machines	1.25	2.75	1.30	2.85
Determine what hardware would be synthesized from an HDL code fragment	1.80	2.95	1.70	2.85
Explain the concept of handshaking between Finite State Machines	.90	2.90	.85	2.90
Explain the impediments to synchronous design	.70	2.65	.75	2.70
Discuss clock skew and metastability of digital circuits	.85	2.85	.80	2.75
Explain why asynchronous inputs to a Finite State Machine are problematic and how design	.80	2.65	.75	2.60

circuits mitigate the problem				
Design a system using a control unit/data unit partition	1.10	2.70	1.15	2.75
Discuss the concept of functional testing and testing strategies	1.45	2.90	1.84	2.84
Design a HDL based test bench	1.40	2.80	1.55	2.80

Notes: * all means statistically significant.

B.3 Students Comments

Additionally, in the post-course survey, students responded to open ended questions regarding the impact of extensive use of programmable boards on their learning and effort, acquiring discipline specific skills (hardware and software skills), intention to continue staying in the engineering program. Student perspectives concerning the amount of and emphasis placed on use of Programmable boards and impact of on their learning were investigated. The results, presented in Table 4, suggest that the extensive use of FPGA boards had a positive impact on acquiring discipline specific skills (hardware and especially software skills), creativity and spirit of innovation, intention to continue staying in the engineering program.

Table 4
Post course Survey- fall and winter 2007-2008-impact of the use of FPGA boards

FPGA Board Impact	Number of Response Fall 2007-2008	Percentage of Responses Fall 2007-2008	Number of Response Winter 2007-2008	Percentage of Responses Winter 2007-2008
The amount of emphasis placed on the use of FPGA boards during the quarter was:				
Too Little	4	27%	1	4%
Just Right	11	73%	20	83%
Too Much	0	0%	3	13%
Unsure	0	0%	0	0%
How much did the use of FPGA boards impact your learning of course content?				
Little	0	0%	0	0%
Somewhat	5	33%	7	29%
Much	8	53%	12	50%
A Great Deal	2	13%	5	21%
How much did the use of FPGA boards impact the amount of effort you put into learning course material?				
Little	2	13%	0	0%
Somewhat	2	13%	11	46%
Much	8	53%	9	38%
A Great Deal	3	20%	4	17%
How often did you use the FPGA boards during the quarter?				
A few times per day	1	7%	0	0%
Once a day	0	0%	0	0%
A few times per week	4	27%	13	54%
Once a week	5	33%	5	21%
A few times per month	5	33%	5	21%
Once a month	0	0%	1	4%

Less than once a month	0	0%	0	0%
Which of the following attributes did the use of FPGA boards help you develop?				
Generate new ideas (creativity)	10	67%	17	71%
Make improvements by introducing something new (innovation)	12	80%	19	80%
Hardware skills	14	93%	21	88%
Software skills	12	80%	24	100%
After taking this class, how likely are you to stay in your current engineering program?				
Very Likely	11	73%	20	83%
Likely	4	4	3	13%
Unlikely	0	0%	0	0%
Very Unlikely	0	0%	1	4%

In summary, IRPA educational research study indicates that the extensive use of the FPGA boards in ECE 333-Digital Systems class seems to have increased students' understanding of course content in different key areas. This is supported by the increase in student ratings of their knowledge of and confidence in various course concepts as well as their ratings of items directly asking about the impact of the logic boards.

C. Instructor's Surveys

The following survey was initiated by the instructor during the academic year 2007-2008, fall and winter quarter:

-The time needed to accomplish specific tasks, like specific labs and project milestones were measured. At this point, no significant differences were noticed regarding students' performance in the 2007-2008 fall and winter quarter, but significant differences were noticed between this academic year and the previous ones. The changes in the introductory logic design class at the level of freshman year impacted students' performance two years later, in the junior level course Digital Systems. About 80% of the groups finished their laboratory assignments at the end of the 3 hours dedicated to the lab, requiring minimum guidance from the instructor. In the previous years, about 50- 60% finished at the end of the 3 hours of lab, and requiring much more guidance from the instructor, students showing rudimentary hardware and software debugging skills.

Conclusions

The results of this educational research study show that the early use of programmable logic devices, starting in the freshman year, and the unlimited access to state of the art design tools and hardware systems improve:

- (i) the learning process;
- (ii) the attainment of Digital Systems specific knowledge and skills;
- (iii) the proper use of technological tools;
- (iv) decrease students' and instructor's work load;
- (v) improve students' retention in the current engineering program.

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