An Analysis of Clock-Jitter on an Analog-to-Digital Converter Using the Signal Processing Worksystem (SPW) Environment

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ABSTRACT- *A sound fundamental understanding of electronic circuits and devices can be used as a basis to formulate an understanding of ADC computer interface devices. However, secondary effects such as offset, drift, clock-jitter, etc. may represent critical characteristics that must be understood and dealt with. The author presents an analysis of an Analog-to-Digital Converter (ADC) simulation that includes the jitter present in real ADC clock-circuitry. The paper exemplifies the in-depth analysis needed to understand some of the secondary nonlinear physical properties of electronic devices as they relate to ADC devices.*

Introduction

Digital Signal Processing (DSP) is rapidly becoming a key technology of the future as the data generated by the information age expands exponentially. This data must be acquired as well as processed. The Analog-to-Digital Converter (ADC) is a key computer interface component for acquiring data. Although the fundamental operations of these devices are relatively simple; subtle and secondary effects, such as offset, drift, clock-jitter, etc., can become critical factors in integrated applications. These effects must be understood and accounted for. For one example, the author presents an analysis of an ADC simulation that includes the jitter present in real ADC clock-circuitry.

The analysis will feature a mathematical approach needed to determine an effective method for simulating the jitter that is present in a real ADC clock. The Signal Processing Worksystem (SPW) will be used to implement a block diagram-based ADC simulation [1]. The basic approach is to use one of the *perfect ADC models* within SPW and then add the clock-jitter component to the simulation. An analysis of an ADC model will be conducted to determine the effect of clock-jitter on a signal as it passes through the ADC.

As implied, when implementing ADC interface devices, it is important that secondary effects, such as clock-jitter, produce negligible effects on an integrated system so that the system desired operational characteristics are achieved. Consequently, studying these secondary effects within a single component through computer simulations, will prove beneficial to understanding the performance of interface devices when they are integrated into complete systems or system components.

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Analog-to-Digital Conversion

In the DSP world, the design process often involves the conversion of analog signals into sampled digital signals, the execution of digital signal processing applications on these digital signals, and the reconstruction of the processed analog signals. DSP is the concept of representing analog signals in a digital format which allows signals to be processed digitally.

Since many signals are analog by nature, a conversion process is needed to convert the analog signal into its digital representation. The process of analog-to-digital conversion is one of the first stages of many communications systems. There are several devices that can be used to accomplish this conversion process. They include quantizers, sample-hold circuits, and ADCs. The ADC uses formatting techniques to digitize analog signals. It employs the concept of quantizing a signal and then assigning binary-coded values to the voltage levels at each sampled point of the signal.

An ADC uses a clock to control the sample period of each sample. Ideally, a signal is designed to maintain a uniform sample period. However, real clocks in ADCs are not perfect devices. They inherently introduce noise and error into device signals. The signal distortion error caused by the clock-noise is called clock-jitter. The effect of clock-jitter on signals is determined by the complexity of the amplitude variations on each sample. Analyses of ADC simulations can provide an illustration of the significance of ADC clock-jitter on interface devices.

An analog signal, which may represent some physical phenomenon, can generally be modeled as a continuous waveform. When an analog signal is modeled and then discretized, it is no longer continuous in time; i.e. the independent variable becomes a discrete set of points usually defined as integer values. At each of these points in time, a value is assigned which represents a quantized equivalent to the value of the analog signal at that instant in time. In summary, an ADC is a device that executes the conversion process to digitize an analog signal into a one-dimensional array of digital words.

ADC Modulation Applications

An ADC modulation application provides an ideal example for formulating a test-bed simulation to study clock-jitter. Thus, some comments on ADC modulation concepts are appropriate. Many signals that undergo analog-to-digital conversion use modulation schemes to enhance the transmission quality of signals. Modulation is a process that incorporates a signal into a carrier which is used to transmit information through channels and into demodulation devices. It is varied in accordance with the carrier signal so that it can be used in a variety of applications; for example, satellite transmission of digital data streams with high bit-per-second rates [2].

Typically, a sinusoid is used as a carrier signal because its derivatives and its integrals are known, and its amplitude and phase are relatively unaffected through linear devices. There are three characteristics that describe a sinusoid; namely, amplitude, phase and frequency. Consequently, there exists at least three different types of modulation. The information of a desired signal can be incorporated into a carrier by modulating the amplitude of the carrier, the

phase of a carrier, or the frequency of the carrier. One common type of frequency modulation scheme is frequency shift keying (FSK). This modulation produces two tones in the frequency domain. One tone produces a 'one' state and the other tone produces a 'zero' state [3]. The modulation that is used in the ADC simulation is the Bi-Phase Shift Keying (BPSK) modulation. The BPSK modulation allows a signal to shift 180° out-of-phase during each transition phase.

Analysis of ADC Simulation

The analysis of the ADC simulations was performed using a computer simulation package called Signal Processing Worksystem (SPW). Clock-jitter produces small variations in the sample time of a signal, thereby, varying the amplitude of the sample. Hypothetically, this amplitude variation results in a sampled waveform that contains amplitude modulation. Phase distortions may also exist due to variations in sample amplitudes. It may result in unwanted phase modulation of the desired signal. The determination of phase distortion and its significance on the ADC signal is the basis for the error analysis. The following ADC simulations were designed to determine the effects of clock-jitter as a function of phase modulation on the input signal. These simulations also provide a sound understanding of some fundamental concepts of ADC models.

1. The first simulation was simply used to obtain an understanding of sinusoidal input signals passing through an ADC model with a perfect clock.
2. The second SPW simulation was used to evaluate jitter error effects in an ADC model with an imperfect clock.
3. The third SPW simulation was used to model an ideal ADC with a Bi-Phase Shift Keying (BPSK) modulated input waveform for the purpose of suggesting future studies.

An ADC system with specified parameters was used as an example for the simulations. The system included a 10-bit ADC with an 80 MHz clock as basic specifications. A midtread ADC model was chosen from the SPW library. The midtread on the ADC model requires the value of the input signal to remain constant as it passed through the origin, which implies an odd symmetrical input-to-output characteristic. Using this ADC model, the clock speed was scaled such that it performed within SPW specifications. The 80 MHz ADC clock would produce an excess of samples resulting in a memory overload error. Therefore, a scaled sampling frequency of 600 Hz was arbitrarily chosen for the ADC clock. A proportionality constant, k , was used as the scaling factor, where

$$k = 80 \text{ MHz} / 600 \text{ Hz} = 1.3 \times 10^5. \quad (1)$$

In the first ADC simulation, the *perfect* ADC model with only clock-jitter errors was used to evaluate its effects on sinusoidal input signals (as illustrated in figure 1 with $\tau = 0$). A time-scaled 200 Hz input sine wave was generated using a signal generator, also illustrated in figure 1. The ADC output spectrum was observed as indicated by the signal sink block. The spectral evaluation of figure 2 (A1) reveals the 200 Hz line spectra to be approximately 70dB above the

noise spectra generated by the clock-jitter. Thus, clock-jitter errors would appear to be negligible.

The incorporation of clock-jitter into the ADC simulation features a mathematical equation that was derived to represent the effects of clock-jitter on a sampled signal. When the distance between sample points is relatively small compared to the overall signal waveform, linearity can be used to simulate the effects of slightly shifted sample times due to clock-jitter. For instance, given two arbitrary samples with known amplitudes, the clock-jitter error on a sampled value is represented by

$$x_e(n) = x(n) + [\tau * (x(n) - x(n-1))/T_s] \quad (2)$$

where, $x_e(n)$ represents the signal $x(n)$ with an added error component due to the clock-jitter τ , i.e., τ is the actual deviation from exact sample times of the signal and T_s is the ideal sample period of the ADC. For the generation of random τ variations, a uniform white noise generator was used. Clearly, the generated noise components due to clock-jitter are a direct phase modulation of the clock-jitter variations.

Equation (2) represents the change of the sample at point n due to phase modulated clock-jitter signal. When equation (2) was incorporated into the first ADC simulation model, the spectrum of the ADC output was evaluated and phase modulation was detected on the signal, as expected and as depicted in figure 2 (A1). Both the clock-jitter effects and the quantizing effects were incorporated into the second simulation. The results illustrated a peak at 200 Hz, normalized to 2, with quantizing effects in figure 2 (A2) as expected; since binary weighting of 1/2 implies 6 dB/bit and 10 bits implies approximately quantizing noise levels of 42 bits below a full scale sine wave input (1 bit for sign and ± 1 bit digital errors). The results were as expected because the first simulation revealed the clock-jitter error to be 70-40dB = 30dB below the quantizing error. Incidentally, a spectral check of the input revealed an absolutely perfect sine wave line spectrum with no quantizing errors.

In the third simulation, an ADC model with a *perfect* clock and a BPSK modulated input signal was formulated. By studying the effects of a *perfect* ADC model on a BPSK modulated signal, the analysis provides an ideal test-bed simulation for some modulation applications. The BPSK modulator used in SPW used a binary input to generate a BPSK modulated signal. Thus, a random data generator was used to represent arbitrary binary input values to the modulator.

The bit rate of the BPSK modulator was a significant factor in the evaluation of ADC signals. Variations in the bit rate of the modulator resulted in variations in the signal sampled data points, thus, altering the bandwidth of the signal. It was varied to study the effects of BPSK modulation on input signals. As a result of this variation, the bit rate of the BPSK modulator controlled the bandwidth of the input signal. Clearly these effects can be studied in more detail with simulations designed to thoroughly evaluate secondary error effects in the ADC processing of BPSK signals.

Conclusions

The most significant conclusion drawn from the ADC simulations is that clock-jitter, represented by small variations in signal amplitude, is negligible for the range of values tested by these analyses. The quantization noise produced by the ADC played a more significant role in the analog-to-digital conversion process. This conclusion is clearly supported by the data displayed in figure 2 where clock-jitter noise is in the order of 30 dB below quantizing noise, [-70-(-40)] dB.

Other observations that can be made concerning the ADC simulations are:

- Although the frequency spectrum plot of the ADC model without clock-jitter was not presented, the simulation model revealed line spectra at the sinusoidal frequency with no measurable noise. Thus, the validity of the simulation model input was assured.
- Clock-jitter can be mathematically modeled using a formula that describes small amplitude variations in signal samples as a function of phase variations as attested to by the simulation results.
- A SPW ADC simulation model was used to study the processing or conversion of BPSK signals for the purpose of illustrating that almost any ADC error analysis can be conducted with computer simulation refinements. For example, the bandwidth of a BPSK signal is controlled by the number of samples executed by the analog-to-digital conversion process.

Thus, not only do the results of this simple analysis provide the means to evaluate the effects of ADC clock-jitter on sampled signals, it also suggests that future studies with appropriate simulation analyses can be used to evaluate *imperfect* secondary ADC effects in many more advanced systems using ADCs; e.g., the conversion of BPSK modulated input signals.

References

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