Keys to Successful VLSI Realization Through MOSIS
or
How to Get Three Computers to Cooperate and Remain Sane[1]

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Abstract

Reduction to practice is the fundamental goal of engineering and a consistent focus of all engineering education. This process has become increasingly difficult to realize, especially for educators who focus upon Very Large Scale Integrated (VLSI) circuit design. The complexity and cost of modern fabrication facilities are beyond both the financial reach and scope of the vast majority of universities. The Metal Oxide Semiconductor Implementation Service (MOSIS) has, for many years, permitted educators to bridge the gap between theory and practice in VLSI circuits. This service provides a low cost method through which student integrated circuit prototypes can actually be fabricated. In a matter of weeks, packaged circuits are delivered which exactly reflect a student's design. Since commercial semiconductor manufacturers perform the actual fabrication, the consistency of the fabrication is excellent. A student's success cannot be better validated than through this reduction to practice.

As appealing as this MOSIS brokered fabrication may seem, there are many nuances in the administration, scheduling, submission and reporting process which can prove disheartening to the VLSI educator. Strict adherence to deadlines, precise formatting of transmission messages, specific computer communication protocols and set funding procedures are driven by the sheer number of MOSIS users. This paper will summarize four years of experience with MOSIS as an important educational tool. It highlights approaches, techniques and disciplines which will ensure the path to successful fabrications will be a smooth and supportive of the educational process.

Introduction

To students of Very Large Scale Integrated (VLSI) circuits, the ultimate test of competence is the actual fabrication of a physical design into a hardware "chip". This process lies outside the grasp of nearly all universities, as the cost of maintaining even a limited fabrication facility is enormous. Through the Metal Oxide Semiconductor Implementation Service (MOSIS) this fabrication process becomes reality for hundreds of students annually.

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With proper preparation, student designed integrated circuits may be transformed from computer generated files into working hardware prototypes in a matter of weeks.

Our experience has shown MOSIS' capabilities make an important and highly motivating contribution to undergraduate education in electrical engineering. The insights which students can garner from a MOSIS fabrication cycle are important enhancements to the design experience base and the maturity of students. However, there is significant preparation required of educators wishing to make use of this capability. Some of this preparation is not completely obvious or documented. In this paper I will describe design capabilities required for educational use of MOSIS. I will also describe a MOSIS fabrication cycle and process timetable an educator must master to effectively use this wonderful tool.

The MOSIS Service

Since 1981, the MOSIS has provided a low cost method through which integrated circuit prototyping can be accomplished. Today over 5,000 users from industry, government and academia choose among the eight MOSIS brokered process technologies offered by four commercial vendors. Originally created through a collaboration between the Defense Advance Research Projects Agency (DARPA) and the National Science Foundation (NSF), MOSIS has become an important vehicle for integrated circuit research and development.

The integration of a MOSIS brokered fabrication cycle into undergraduate education is possible only because of government financial support, reliability of the MOSIS brokered fabrication technologies, and timeliness of the process. Although DARPA recently ended its long standing support of MOSIS educational programs, NSF continues to provide funding for fabrication and packaging of student designed integrated circuits. Funding is based upon the number of enrolled students and covers fabrication of ICs of fixed sizes in two technologies. MOSIS concatenates the designs of multiple users into multi-product mask sets. These mask sets are sent to established commercial vendors using well characterized process controls. Consistency in fabrication is excellent. Students find that variations in the process technology are held within strict tolerances. These variations can therefore be reliably included in the circuit design process. The fabrication cycles operates on a well established cycle consistent with the academic year. Generally, NSF sponsored MOSIS “runs” are performed in late November, late March and again in June.[2] Between seven and eight weeks later, four copies of each student IC are shipped in die bonded packages, ready for testing.

The National Science Foundation currently supports MOSIS fabrication of two classifications based upon student experience. Introductory VLSI design courses are supported at a rate of one 2.3 mm x 2.3 mm “Tiny Chip” for every two enrolled students. These Tiny Chips are fabricated in Orbit Semiconductor’s 2 micron minimum geometry, double metal, double poly, n-well CMOS process. This is a low noise analog process which includes a p-base layer and CCD layer. Tiny Chips have 40 pins. Using a single shared power supply and ground pins, each

[2] Run closings are subject to change both in date and frequency. MOSIS generally sets the run dates once each government fiscal year. The current schedule is accessible through the MOSIS web-site, ftp://ftp.isi.edu/pub/mosis/info/fabrication-schedule.inf.

student has a maximum of 19 input/output pins at their disposal. Our students have conservatively designed circuits as complex as 4 bit Arithmetic Logic Units and 4-bit DACs in this area. Students enrolled in advanced VLSI design courses continue to be NSF supported with an entire Tiny Chip per student. A simple encryption/decryption system and the processor core of our undergraduate teaching computer trainer have each been fabricated using two chips funded in this way. Recently, NSF has established advanced course funding for the AMI, 1.2 micron minimum dimension geometry process. This is a double metal, double poly, n-well process. Die sizes for these chips are 2.2 mm by 2.2 mm, with gate densities approximately four times that of the 2.0 micron process. NSF funding procedures are described in detail on the MOSIS Web site and may be transferred from ftp://ftp.isi.edu/pub/mosis/info/#enroll-conf-form.inf#.

User's Computer System Requirements

In order to successfully integrate the MOSIS fabrication processes into our curriculum, we have found a three "group" computer system to be most effective. As illustrated below, the system consists of a set of student design computers, a faculty coordination computer and our anonymous FTP site mainframe. At our institution, students perform both physical design and circuit simulation on a set of LAN connected PCs. Completed student designs are transferred to a central faculty PC for final verification and conversion to a MOSIS acceptable design format. The faculty machine is then used to transfer the designs to our site FTP mainframe. The faculty PC is also used to notify the MOSIS system computer to execute electronic design transfer of the student designs and to monitor the progress of the fabrication cycle. It has been our experience that student PC-to-faculty-PC communication may also be executed through shared diskettes. No student design file we have transmitted to MOSIS has exceeded the capacity of a standard 3.5" 1.44 MB diskette. However, reliable electronic mail, internet access and file transfer protocol capabilities are absolute necessities for successful use of MOSIS.

The capability of student PCs is an issue. It has been our experience that circuit simulation, rather than physical layout, makes the greatest demands on computer speed and memory capability. PCs with clock speeds of 166 MHz or more are required if circuit simulation is to be executed thoroughly. This experience is based upon half Tiny Chip sized circuits simulated without pad cells. While the duration of simulations depends greatly upon circuit complexity, we find even the most complex sequential circuits can be completed in a few hours.

Equally important to student use of MOSIS is reliable VLSI design and circuit simulation software. Although a number of different software options exist, the availability of student personal computers has driven us to PC based software. We currently use Tanner Research L-Edit® for physical design. The libraries of default layout or "technology" files integrated with L-Edit are an important feature. These files contain layout and display settings consistent with most of the MOSIS brokered process technologies. L-Edit also has an integrated set of design rules consistent with each technology. Hence, layout editor polygons of a certain color are correctly understood to correspond to a specific fabrication mask level, and polygon sizes are correctly understood to correspond to specific physical dimensions. The editor will also know if the placement or size of a particular mask polygon violates a particular technology's design rules.

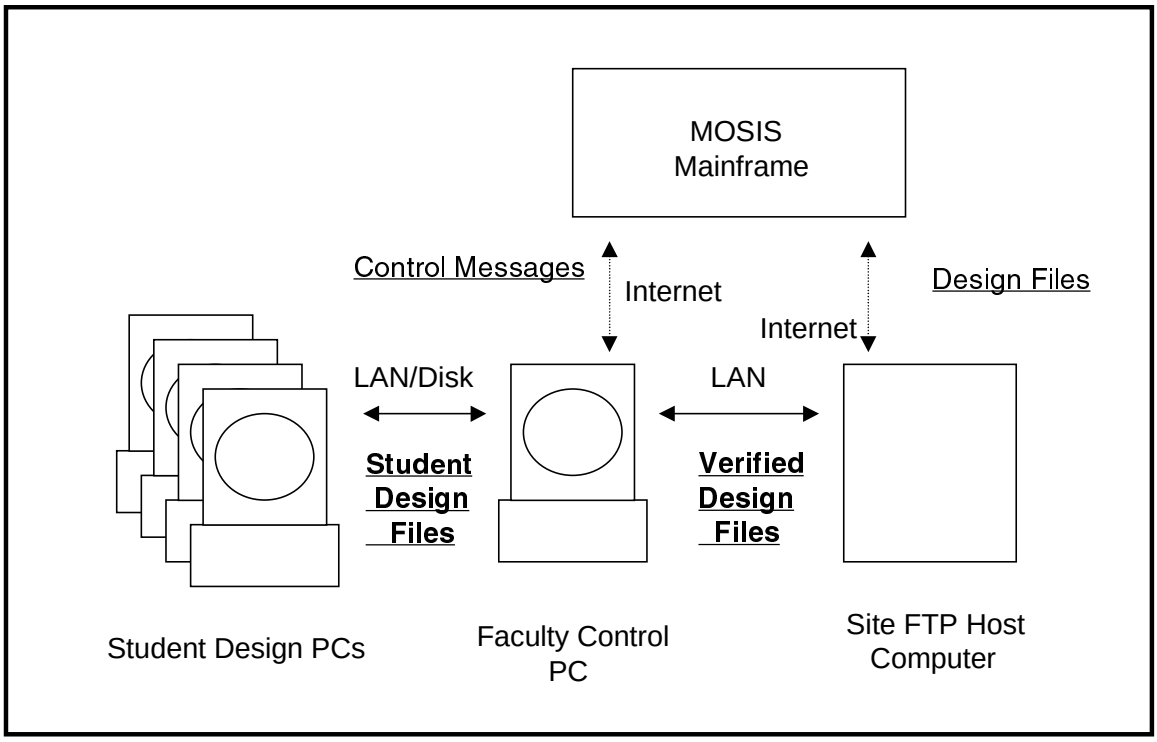

Figure 1. Example instructional computer network used for student interaction with MOSIS. Student PCs are used both for physical design and design simulation. The faculty control PC is used for student design screening as well as control and monitoring of the fabrication process. The site FTP host computer stores properly formatted student designs for FTP transfer to the MOSIS system computer. Student and Faculty computers may be LAN connected. Faculty and host mainframe must be LAN connected. Internet e-mail and FTP are required for communications with the MOSIS mainframe.

In addition to these "technology" files, L-Edit has built in "extraction" files which assure consistency between the physical design and netlist representations of a student's design. For example, the red polygon which overlays a green active outline surrounded by a light blue n-select is understood to be the gate of an n-channel MOSFET. Circuit simulation of these extracted netlists is a student's best assurance of a fully functional design. We currently use either Tanner Research T-SPICE® or MicroSim PSPICE® as our circuit simulators. We regard the availability of both of both a layout editor and a circuit simulator on each student computer as essential to efficient and successful design.

In addition to "technology" definitions, we have also found it important to provide a library of pad frame cells to our students. In mere weeks of instruction, we do not feel it reasonable for students to develop robust pads of their own. Sufficient source/sink capability, and protection from short circuited outputs and improper input voltages, should both be provided by the pad cells. This is particularly for true of Tiny Chips which will be evaluated in a student laboratory under less than ideal conditions. We have found the Tanner Research SCMOS® library pad frame cells yield in a highly consistent fashion and stands up well to student abuse. Digital input and output pads, tri-state output pads, power and ground pads, and both protected and unprotected analog input pads are all available in this library. As long as the pad frame

contains a power pad, a ground pad, and properly placed corner pads, students are free to mix and match signal pad cells as demanded by their designs.

The MOSIS Educational Fabrication Cycle

In addition to the computer hardware, software and network preparation necessary for VLSI design, an educator using MOSIS must be aware of a set of important administrative events which repeat during each fabrication cycle. These events are summarized in Table 1 below.

Establishing Fabrication Accounts

The MOSIS system tracks fabrication funding through a series of accounts. We describe these accounts in two fundamental classes; those which support circuit research and development, and those which support education. Due to the differences in support, these classes may be further subdivided. We highly recommend each new using institution establish a minimum of one R&D account and one education account with MOSIS.

R&D accounts can be classified as either "pure research accounts", or "commercial accounts". Although MOSIS refers to both types as Commercial Accounts, we make this distinction based upon the source of funding. "Pure research accounts" are supported by the using institution's DARPA or NSF sponsored research funds. "Commercial accounts" must be funded directly by the user. The former is funded from the using institution's DARPA or NSF sponsored research funds. The latter is funded directly by the user. These accounts are particularly beneficial when an educator is first using the service. A trial fabrication cycle is an excellent method for testing the user-to-MOSIS communications as well as the correspondence between a user's layout and simulation editors and the MOSIS system. NSF funded fabrication executed through education accounts must support student design. As such, a new user would be well advised to establish and fund a research or commercial account and then execute at least one test fabrication cycle. We regard this test cycle as key to the success of new MOSIS users.

Prior to the first student use of MOSIS, an NSF Sponsored Education Account must be established[3]. The National Science Foundation will review a new using institution's application for adequacy in IC design and simulation and circuit test capability as well as faculty experience. These applications should be submitted once a firm enrollment figure for the coming semester can be established, but not later than two weeks after a given semester begins. Once approved, MOSIS will establish an account along with corresponding funding and passwords. A separate education account will be established for introductory and advanced courses. Once the accounts are established, their budgets may be renewed by NSF each semester.

[3] The Application Form for Education may be down loaded from the MOSIS Web Site: ftp://ftp.isi.edu/pub/mosis/info/ #enroll-conf-form.inf#.

Event	Deadline (R/M)
Establish Commercial/Research Account at MOSIS	1 Academic Year Prior to First Student Use of MOSIS (R)
Execute Trial MOSIS Fabrication	2 Semesters Prior to First Student Use (R)
Establish New MOSIS Education Account	Within 2 Weeks of Semester (M)
All Student Designs to be Fabricated Successfully Simulated	10 Days Prior to Run Closing (R)
All Student Designs Screened by Faculty or Staff Member	7 Days Prior to Run Closing (R)
All Student Designs Placed on FTP Site for Transfer	5 Days Prior to Run Closing (R)
"New-Project" Messages Sent to MOSIS	5 Days Prior to Run Closing (R)
"OK Project-Check, In Fab Queue" Message Received from MOSIS	3 Days Prior to Run Closing (R) 1400 Hrs PST on Run Closing Date (M)
Begin Student Analysis of Fabricated Tiny Chips	Upon Receipt of Tiny Chips (R)
Transmit Tiny Chip Fabrication Report Message to MOSIS	Receipt of Chips Plus Three Months (M)
Renew MOSIS Education Account	Within Two Weeks of Start of Semester
Repeat Student Design Cycle	

Table 1: Summary of key milestones in the first use of the MOSIS. Deadlines followed by (R) are recommended by the author. Deadlines followed by (M) are required by MOSIS or NSF. Details are discussed in the text.

The Student Design Timeline and Submission Process

For institutions with semester schedules, the MOSIS Fabrication Schedule permits between 9 and 11 weeks from start of class until the corresponding semester run closing date for introductory classes. Educators must carefully pace their instruction in order to meet this time table. Students and faculty must agree to an "end of design" date sufficiently prior to the MOSIS run closing date to permit final check, and computer transfer. About ten days has proven to be adequate to perform this process. In the three days following submission, all student designs should be screened for fatal errors and corrected. These errors include improperly assemble pad frames, incorrect connections to pad cells, improperly connected well and substrate ties, incorrectly connected power or ground pads and obvious mis-connections. [1]

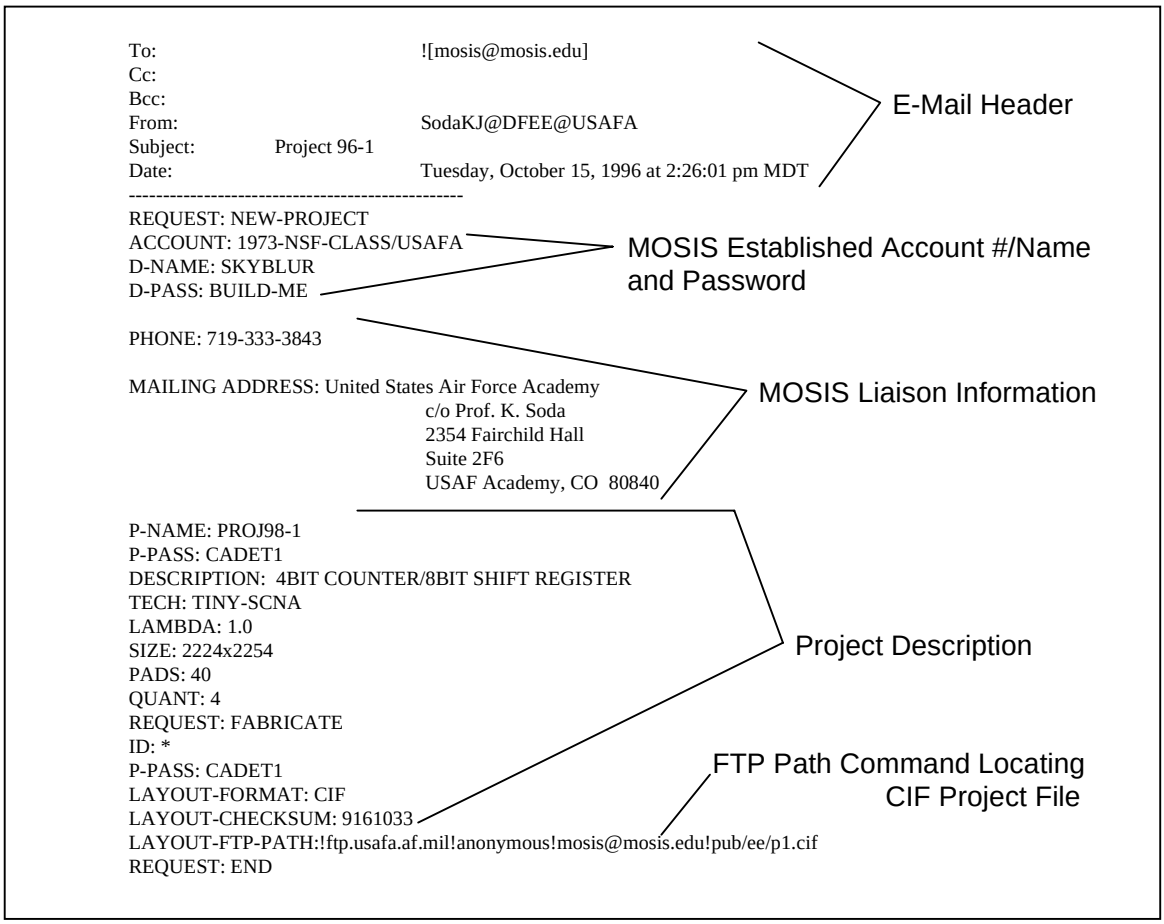

Figure 2. Sample One-Step New Project Request e-mail message. The FTP transmission option has been used in this message. The address string shown in this message is exactly the 57 character maximum which our experience as shown is accepted by the MOSIS computer.

Once adjudicated to the faculty member's satisfaction, student designs should be converted to a MOSIS acceptable format[4], either GDSII or CIF, and then placed on the users' anonymous FTP site. Immediately upon successful transfer to the host FTP site, a "New-Project" e-mail should be sent to the MOSIS system computer.[5][2] This message contains information on the user, user's account, key project parameters, and the path to the FTP host where the design file is located. One message must be generated for each Tiny Chip. A sample "New-Project" e-mail is shown in Figure 2 above. Experience has shown this process should be begun at least five calendar days prior to the run closing date. Designs which have not been accepted by MOSIS by 2:00 PM Pacific Standard Time will not be included in the subject run. Even with delays due to internet traffic, it should take no more than two calendar days for the MOSIS system computer to transfer and evaluate a student design.

[4] MOSIS accepts design files either the GDSII or CIF file formats. Most layout editors support one or both of these formats. Tanner Research L-Edit produces design files in a proprietary format which can be converted prior to transmission.

[5] This manual may be FTP transferred from; ftp://ftp.isi.edu/pub/mosis/manual.

The MOSIS system computer checks each New-Project message for validity of account number, then attempts to transfer the design file from the host FTP site. Once received, the computer compares its received file checksum value with that contained in the message (third line from the bottom). Each student project will have a checksum value established by the layout editor. Agreement between these two values assures the data transmission occurred correctly. The MOSIS system then performs a gross project check. It ensures the design file technology and chip size correspond to that described in the message. This project check in no way assures the soundness of student designs, only that the design file and the project description in the New-Project message agree. Upon the completion of each check[6], the MOSIS system computer issues an e-mail message indicating success or failure. If the project fails a step, the acceptance process ceases. If a project passes all checks, an "OK Project-Check, In Fab Queue" message is generated and the project is officially becomes part of the run.

It should be obvious from the complexity of the submission process a host of opportunities exist which will frustrate transmission. The trial submission process suggested above can significantly smooth the first student use of the MOSIS system. Thorough faculty or staff screening of student designs will also smooth the submission process. The five day lead time for design submission will give students an opportunity to re-submit their designs in the event of a transmission failure or unforeseen design error.

Post Fabrication Analysis

The most important educational benefit of MOSIS fabrication is derived through the evaluation of the fabricated prototypes. The seven week fabrication cycle places delivery of finished product in mid-January, late May or early August. As such, educators must plan to continue student involvement in the Tiny Chip process into the following semester. Direct student evaluation of their own projects offers a wealth of opportunities to enhance the total design process. We have found students often benefit more from the identification of a design inconsistency than they do from a perfectly working chip.

In addition to the pedagogical benefits of student executed testing, NSF requires reporting on the results of testing on all sponsored Tiny Chips within three months of receipt of devices. Testing for both functionality and speed, and comparison with simulation are all desired elements of these reports.[7] Electronic mail is the preferred method by which reporting can be executed. NSF sponsored education accounts will not be renewed unless reporting on all previously fabricated chips have been completed.

Words of Wisdom

Given the NSF requirement for full reporting, educational users must carefully plan for post-fabrication analysis, especially for Spring semester MOSIS submissions. Delivery of ICs in

[6] In order of receipt, the successful check messages are I) OK New Project, ii) Queued for Project Check, iii) OK FTP, iv) OK Project-Check, In Fab Queue.

[7] A sample NSF model Tiny Chip report is included with the NSF sponsorship information. FTP access to this information is: ftp://ftp.isi.edu/pub/mosis/info/ #enroll-conf-form.inf#.

the late May often conflicts with the end of the school year. MOSIS users must make arrangements so that these Tiny Chips are evaluated during the summer recess, or risk termination of support.

It should be also be clear from this description that the MOSIS submission process itself places great demands upon faculty and staff. Our experience has shown that a single faculty member or knowledgeable graduate assistant can reasonably handle no more than ten Tiny Chips during the project submission stage. As such, institutions wishing to support introductory courses with enrollments larger than twenty must make the appropriate preparation for support staff, especially during this critical stage.

The dedicated staff of the University of Southern California's Information Science Institute make this remarkable service possible. I feel it important to acknowledge two key staff members who play particularly important roles in daily operations. Mr. Sam Reynolds is responsible for general MOSIS operations and can direct technology specific questions to other specialists. Ms. Helen Thompson is responsible for account management and is highly knowledgeable about NSF funding. Both of these individuals can be assessed via e-mail at support@mosis.edu.

MOSIS - More Than An Undergraduate Teaching Aid

The process which I have described illustrates only a fraction of the capabilities and options available through the MOSIS service. Although not NSF sponsored, MOSIS offers access to silicon CMOS process technologies with minimum dimensions as small as 0.35 microns. The Vitesse gallium arsenide MESFET fabrication technology may also be accessed. Even a multi-chip module process is available. Die sizes, packages and bond pad arrangements can all be customized. The MOSIS computer can also be used to perform design submission in multiple steps, to check on the status of a design's run, to cancel a project, to transfer library data and to communicate with the MOSIS system staff. It is no wonder that MOSIS has become important to circuit developers across a wide spectrum of motivations.

In Summary

This paper has summarized the method by which the MOSIS service may be accessed by undergraduate educators of VLSI design and technology. With proper preparation MOSIS can provide the vital link between design and reality. In summary, the key to educator sanity in this process is preparation and planning. To succeed in its use, educators must brave the uncertainties of local area networks, the internet as well as the vagaries of their own student's designs. However, the great practical experience and insight this process provides students makes the integration of MOSIS fabrications in VLSI education more than worth the effort.

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3. University of Southern California Information Science Institute Web Page; http://www.isi.edu/pub/mosis

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