2006-1345: INTERPOLATION: A FIRST STEP IN TEACHING RATE CONVERSION

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Interpolation: A First Step in Teaching Rate Conversion

Abstract

The convergence of digital communications and digital signal processing is gaining emphasis in many engineering colleges today. The implementation of these communication systems using both high performance digital signal processors (DSPs) and field programmable gate arrays (FPGAs) is nothing new. In general, these concepts and techniques can be discussed under the umbrella term of software defined radio (SDR). To understand a SDR, one needs to understand rate conversion. While the basics of the rate conversion theory have been well established for decades, the inclusion of these topics at the undergraduate level can be fraught with teaching dangers. If realistic hardware projects and hardware-based demonstrations are to be included as part of a course, the cost factors escalate rapidly. With most commercially available boards costing more than $10,000 apiece, multiple boards to support such a course rapidly become prohibitively expensive.

To support our desire to teach these topics at the undergraduate level, we felt it was necessary to develop a low cost DSP board that would allow us to implement the realistic hardware projects and hardware-based demonstrations previously mentioned. This new board interconnects a Texas Instrument (TI) C6711 or C6713 DSP starter kit (DSK) to an Analog Devices (AD) quadrature modulator (AD9857). This modulator is capable of operating at up to 200 million samples per second (MS/s), with a resulting carrier or intermediate frequency of up to 80 MHz (i.e., 40% of the system's sample frequency). An onboard 32-bit direct digital synthesizer (DDS) is used to generate the carrier waveform values. Baseband 14-bit in-phase and quadrature (I/Q) data are presented to the modulator, which can be programmed to interpolate the data at rates of 4x to 252x. The AD9857 is interfaced to the DSK using an Altera Cyclone FPGA. The FPGA provides queuing of the I/Q data, and the logic for control/programming of the modulator.

This paper will detail the hardware and software issues associated with this system and briefly describe the classroom utilization of this system in an undergraduate environment.

1 Introduction

The convergence of digital communications and digital signal processing is gaining emphasis in many engineering colleges today. The implementation of these communication systems using both high performance digital signal processors (DSPs) and field programmable gate arrays (FPGAs) is nothing new. In general, these concepts and techniques can be discussed under the umbrella term of software defined radio (SDR). To understand a SDR, one needs to understand rate conversion. While the basics of the rate conversion theory have been well established for

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2 Description of the Hardware

As shown in Figure 1, this new board interconnects a Texas Instrument (TI) C6711 or C6713 DSP starter kit (DSK) to an Analog Devices (AD) quadrature modulator (AD9857).

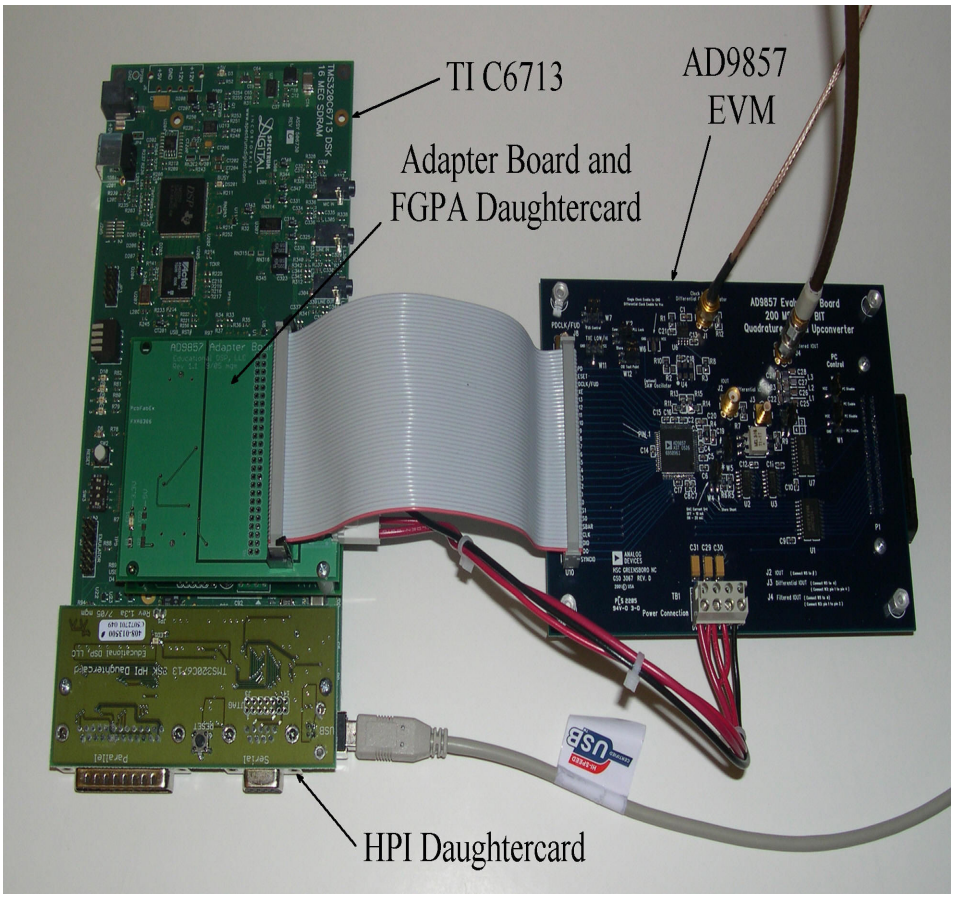

Figure 1. The complete TI C6713 and AD9857 based rate conversion system.

This modulator is capable of operating at up to 200 million samples per second (MS/s), with a resulting carrier or intermediate frequency of up to 80 MHz (i.e., 40% of the system's sample frequency). An onboard 32-bit direct digital synthesizer (DDS) is used to generate the carrier waveform values. Baseband 14-bit in-phase and quadrature (I/Q) data are presented to the modulator, which can be programmed to interpolate the data at rates of 4x to 252x. The block diagram of the modulator is shown in Figure 2.

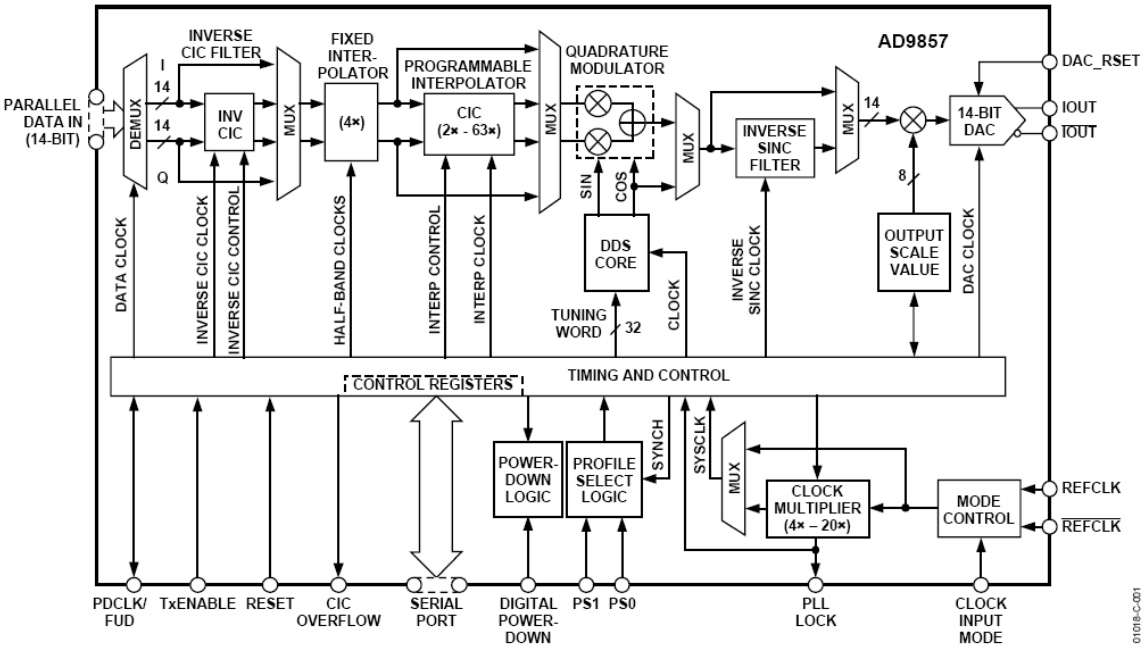

Figure 2. The block diagram of the AD9857 (courtesy of Analog Devices).

The AD9857 is interfaced to the DSK using an Altera Cyclone FPGA. The FPGA provides queuing of the I/Q data, and the logic for control/programming of the modulator. The FPGA daughtercard and the required adapter board are shown in Figure 3.

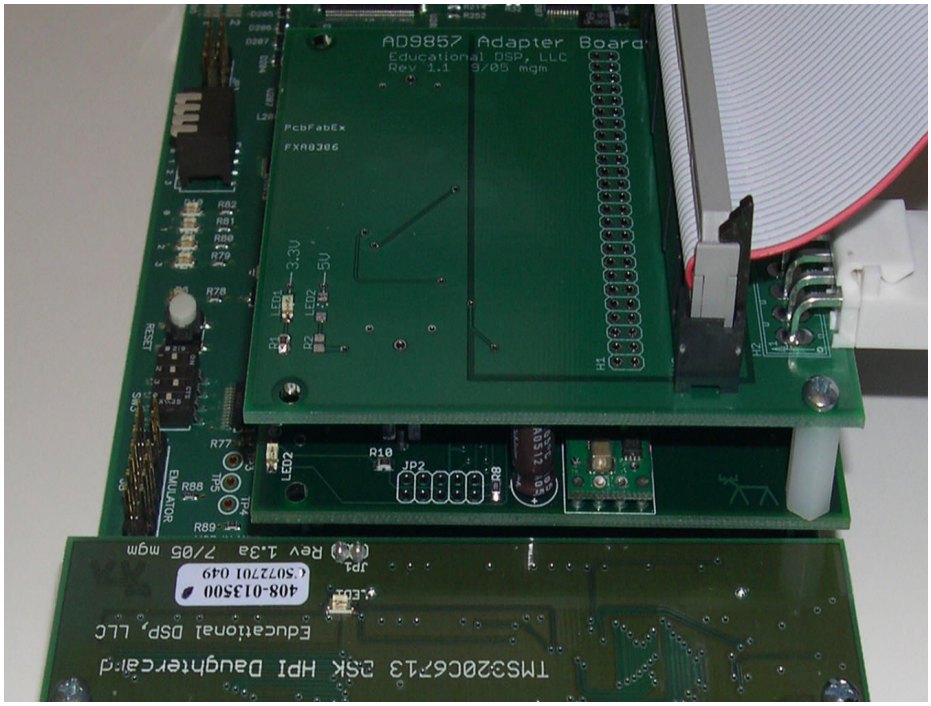

Figure 3. Adapter board and FPGA daughtercard stacked on top of a TI C6713 DSK. The HPI daughtercard visible in the foreground is required to operate this system from winDSK6.

3 The Interface and Control Software

For ease-of-use and to allow for both rapid experimentation and demonstration the winDSK6 program and its Windows-based interface (shown in Figure 4) were modified to allow for direct control of the hundreds options and register settings that control the AD9857 EVM (evaluation module).

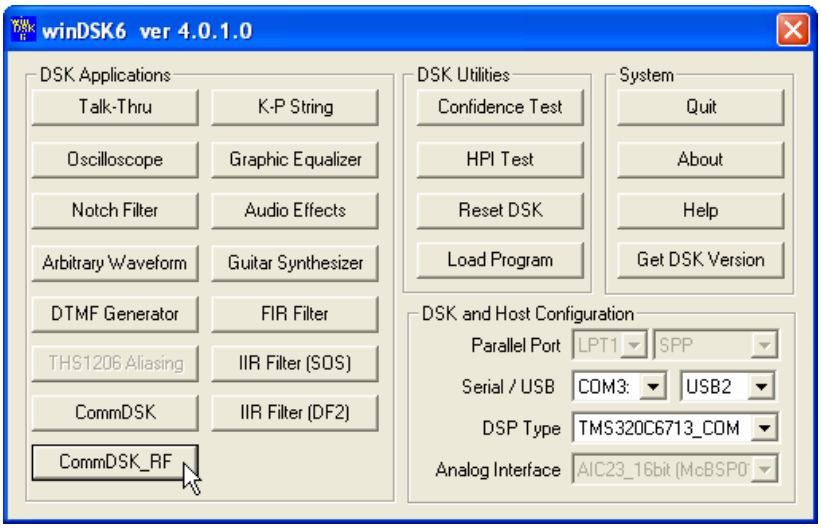

Figure 4. The winDSK6 graphical user interface (GUI).

In Figure 4, notice that the cursor is resting on the "CommDSK_RF" button. Click on this button opens a window similar to that shown in Figure 5.

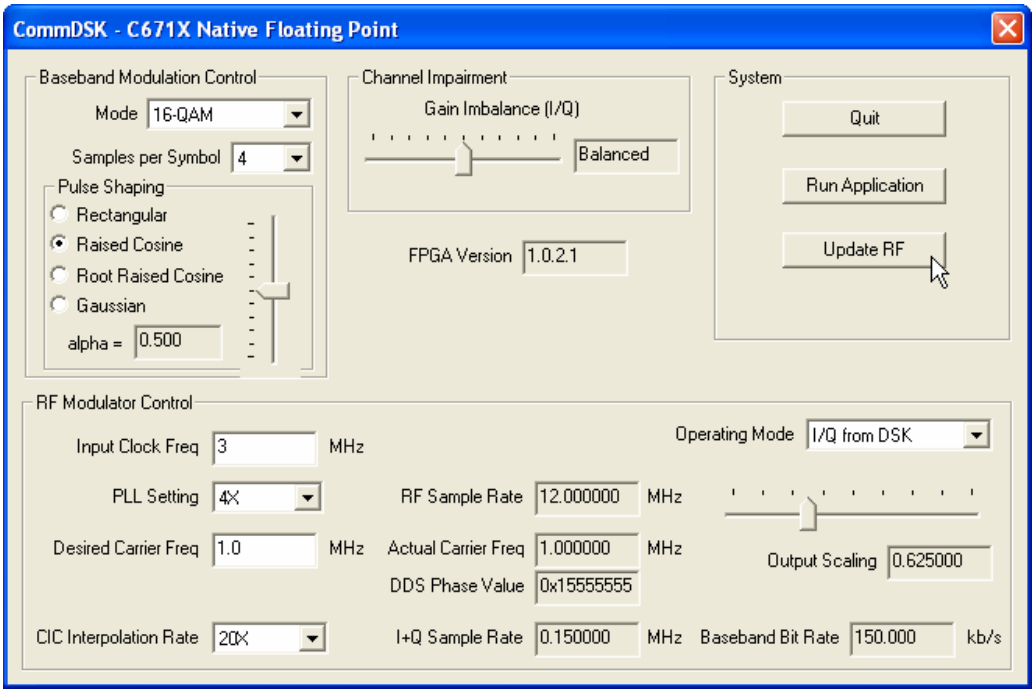

Figure 5. Controls for the AD9857 modulator and the TI C6713 baseband data generator.

4 System Operation

The AD9857 quadrature digital up-converter device has three distinct operating modes; quadrature modulation, single-tone generation, or interpolating DAC mode. The hardware that was designed is capable of operating the AD9857 in any of these modes. However, this paper will focus on operations in the quadrature modulator mode. To reduce the design risk and complexity associated with designing a complete AD9857 board, we chose to utilize the evaluation board supplied by Analog Devices. [One important note for anyone attempting to reproduce this work is that the AD9857 evaluation board will not operate correctly from its signal headers unless a pull-up resistor is attached to U2 pin 5 on the development board.]

The AD9857 requires a data source that provides 14-bit interleaved in-phase and quadrature (I/Q) data. Direct connection to the DSK external memory interface is not practical given the data rates desired, so an adapter board based on the Altera Cyclone FPGA was developed. In order to make the FPGA daughtercard design usable for other projects, it was designed with a generic interface exposing as many available FPGA input/output pins as possible. This interface is not directly compatible with the connectors on the AD9857 evaluation board. A simple adapter board was designed to provide the necessary signals and connectors to interface to the AD9857 evaluation board. The block diagram of the complete system is shown in Figure 6.

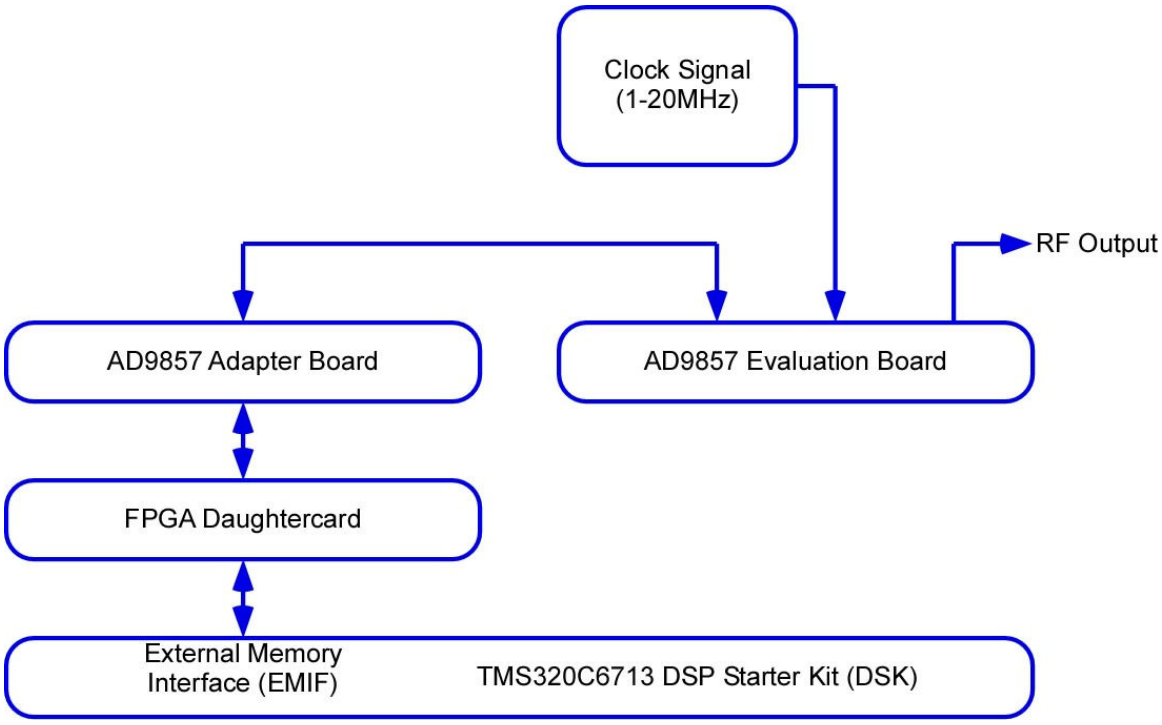

Figure 6. Complete system block diagram.

The FPGA daughtercard provides the direct control of the AD9857. Three modulation data sources are supported; baseband pulse shaped data from the DSP, ramps on the I or Q data channels, or pseudorandom (PN) data.

The functional block diagram of the FPGA logic is shown in Figure 7. If the ramp or PN data source is selected, the board operates autonomously without DSP data. If baseband data from the DSP is used, a 64 word FIFO is used to reduce the interrupt overhead incurred in sending the data. Depending on the baseband modulation scheme and pulse shaping used, baseband sample rates in excessive 500kS/s can be achieved. The AD9857 device has an SPI-compatible serial interface for configuration and programming. The FPGA implements an SPI transceiver to send and read configuration data stored in the AD9857 registers.

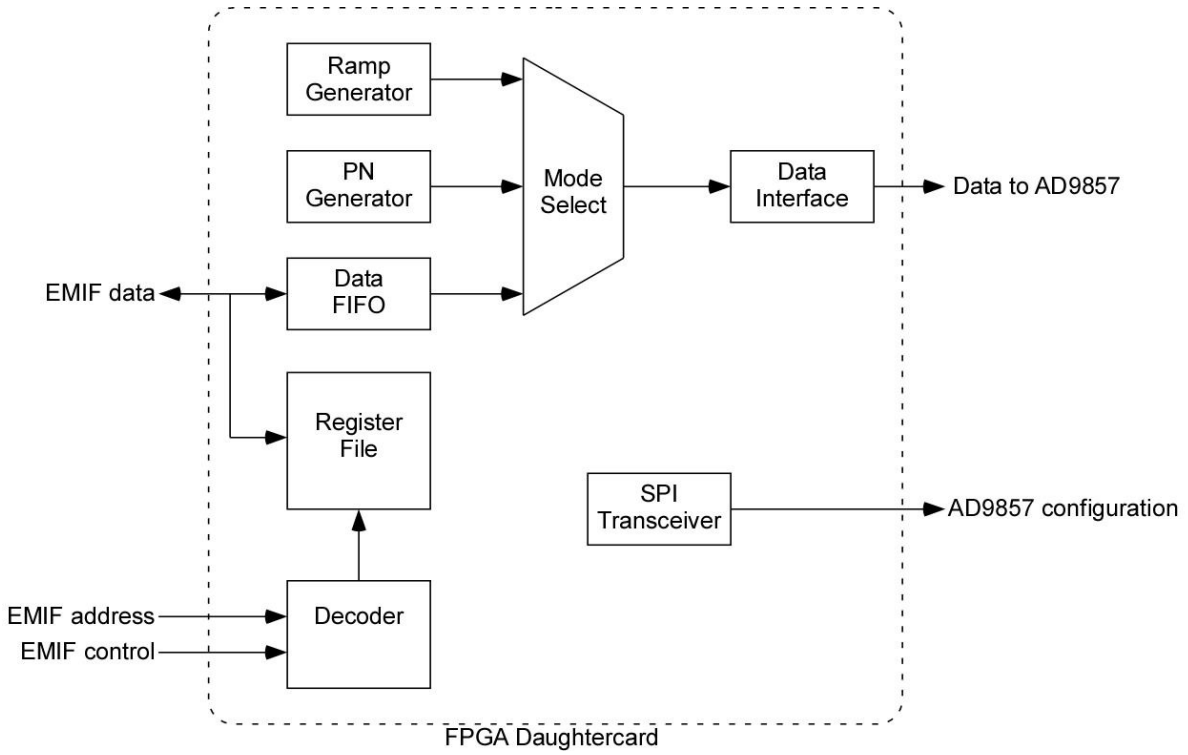

Figure 7. The functional block diagram of the FPGA logic.

The software application that was developed provides complete control over the AD9857 data path. This application is in fact an extension of our previous work that provided a complete quadrature modulator at carrier frequencies in the audio band.[1-12] With digital up-conversion, the carrier frequency may now be as high as 80MHz. The DSP supplies baseband data in a number of modulation schemes with variable pulse shaping features. That data is then sent to the AD9857. The AD9857 provides additional interpolation, and then modulates the signal onto the desired carrier frequency.

5 System Performance

With the complete system shown in Figure 1 connected to a host PC running winDSK6 (upgraded for commDSK_RF functionality) and an external clock attached to the AD9857 EVM, proper operation can be assured by measuring the output of the system. A typical system output as displayed on a spectrum analyzer (SA) or vector signal analyzer (VSA) is shown in Figure 8. In Figure 8, a slight amount of carrier leakage is clearly present. The central portion of the signal

is the desired signal's spectral content, with the remaining skirting effect due to the rate conversion process. The rapid roll-off of the signal's power near the edges of the display is due to on board analog filtering of the signal. Finally, the horizontal portions of the spectral display indicate the system's noise floor. The constellation diagram associated with this signal is shown in Figure 9.

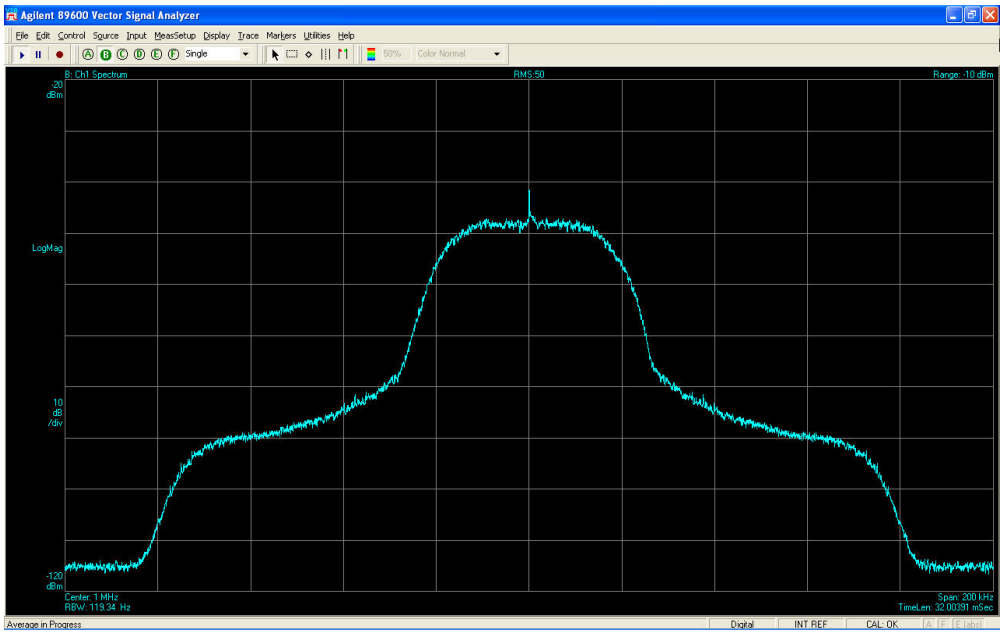

Figure 8. Typical spectral display. Carrier frequency - 1 MHz, modulation scheme - 16-QAM, raised-cosine pulse shaping (roll-off factor = 0.5), and a baseband data rate of 150 kbps.

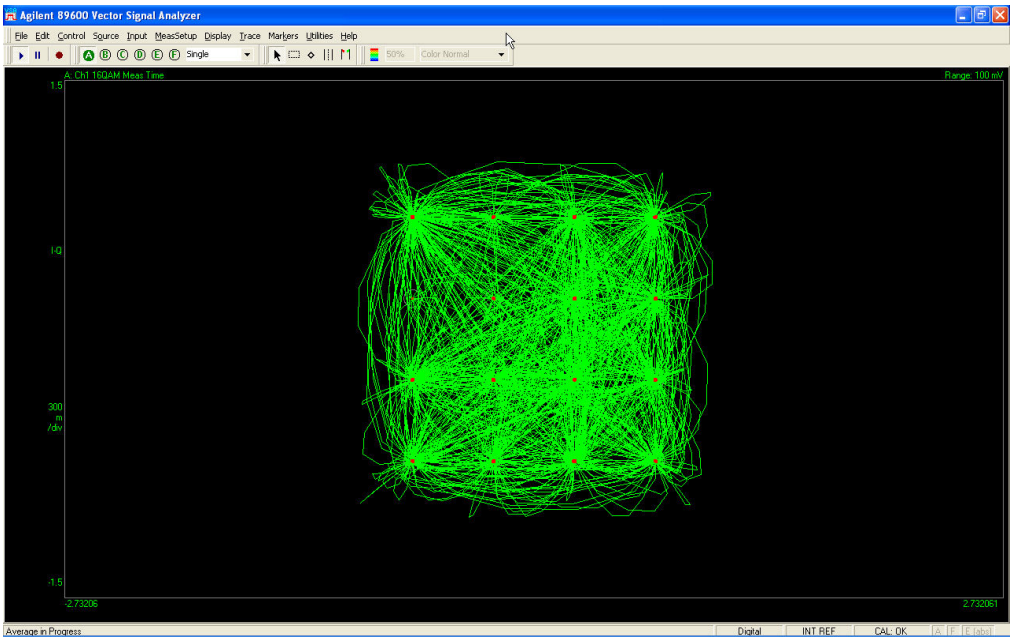

Figure 9. Constellation diagram associated with the example signal.

6 Classroom Use

Previous offerings of our DSP course have discussed rate conversion but have reinforced the student knowledge gained with the ubiquitous homework problem set and its associated MATLAB exercise. The extension to a real-time rate conversion system is by no means a trivial step. If student involvement in parameter selection and signal monitoring (for proper operation) is desired, significant time must be devoted to both the theory of the rate conversion process (as implemented in Figure 2) and the inherent limitations associated with this, and any, real-time system. This transition from a theoretical result to an actual signal output can be very frustrating if not handled properly. We prefer to handle these issues with additional classroom time being devoted to the rate conversion topic.

7 Conclusions

If you are interested in educating your students about the implementation of communication systems using both high performance digital signal processors (DSPs) and field programmable gate arrays (FPGAs) without spending tens of thousands of dollars for an individual board, consider this type of approach to solving the problem. This approach was very well received by our students and has the additional effect of reinforcing RF and communication system test and measurement skills.

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