An Interactive Web-Based Analog Grade Computer as an Electrical Circuits Capstone Lab Project

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Abstract

This paper describes the use of an interactive web-based circuit demonstration system to provide a mid-semester superposition capstone experience for electrical circuit fundamentals lab students. The particular circuit to be interactively demonstrated is a simple electronic artificial neural network which is used to compute individual and class average grades in our Electrical and Computer Engineering 100 Fundamentals of Circuits course. This provides a simple example of analog computing using a summing circuit. The analog grade computer is more fully described in a 1999 ASEE North Central Section Spring Conference paper by two of the authors of this paper entitled: "Neural Networks as a Source of Introductory Electrical Circuit Analysis Problems." The interactive system is based on a recently developed LabVIEW™ application for web-based circuit demonstrations which was subsequently enhanced to add distributed control of the circuit of interest. The resulting circuit demonstration emphasizes the key concepts of voltage division, superposition, circuit loading, and the principle of duality.

I. Introduction

We perennially update our fundamentals of electrical circuits course for non-majors (ECE 100). There are multiple dimensions of opportunities for updating what would otherwise could become rather prosaic – if not for the students then at least for the instructor. Regardless of whatever updates are selected we need to remain faithful to introducing electrical circuits in a manner such that the students gain competence in circuit analysis using fundamental circuit laws.

Our web-based Analog Grade Computer (AGC) provides the following updated electrical circuits learning experience in:

- Components:
  - The use of digital potentiometers rather than mechanical potentiometers. The students have already analyzed mechanical potentiometers in their first lab session.
- Instrumentation:
  - Virtual instrumentation.
  - Distributed display and control (action at a distance).
  - Multi-channel control and data acquisition.
- Application:
  - Weighted grade computation germane to their ECE 100 course.
- Relationship to scientific and engineering endeavors:
  - A degenerate artificial neural network, i.e. a single neuron.
  - A historical relationship of operational amplifiers to analog computing.
- Context:
  - Out of scope
    - The students are not expected to know the theory or application of op amps.
    - The students are not expected to know LabVIEW™.
    - An understanding of ANNs is not the purpose of our exposition nor are concerns involving digital simulations or implementations of ANNs.
  - In scope
    - The student is expected to analyze parts of the system using Ohm's law, voltage division, loading effect analysis, superposition and power concepts.

We chose a single artificial neuron with an identity activation function as the basis of our example application[2]. Specifically, the neuron is built using op-amps and is used to compute the student's grade in our ECE 100 course: Homework 10%; Lab 30%; EXAM I 15%; EXAM II 20%; and FINAL EXAM 25%. The neuron inputs are composite grades that are to be weighted in computing a final grade. Sample data is scaled to 0.0 to 1.0 with 1.0 considered a perfect score. Extra credit is facilitated in the components and the output by values greater than 1.0. Weights are represented as synaptic connection strengths. For example, a 0.85 course grade would arise from the following grade components respectively: 1.08, 0.93, 0.89, 0.83 and 0.67[1]. An extended exercise involves reprogramming what is basically a summing circuit to use unity weights and then to compute an average grade among up to five students.

II. Project Background

The project is scheduled to be completed in three weeks. It is initiated in lecture. The initial, display only, web access to the running client virtual instrument (vi) is completed as homework. The client vi access for distributed control and display is completed in lab. The analysis problems are completed as lab homework.

The following is a sample of potential exercises;

- In the web available photograph of the AGC delineate the summing node.
- Develop intermediate algebraic steps for expressing voltage division in terms of conductances rather than resistances.
- For one of the grade inputs identify the related circuit components and its IC pins representing the low, high and wiper terminals.
- In our digital potentiometer what terminals are used to simulate a manual "control" operation?
- Draw a circuit diagram from the viewpoint of +5V and ground representing the implementation of a grade component. Identify the uses of voltage division and compute the maximum voltage that can be used to represent a grade.
- How much under a digital potentiometer maximum power rating is the design?
- Assume 1G Ohms input resistance and compute the loading effect of a buffer.

The intricate aspects of superposition are covered in lecture. Duality is presented as well for purposes of awareness of an alternative representation and its connectedness to source transforms but not for the purpose of general competency in performing dual transforms.

At this time the students have not been educated in digital logic and computer architecture, nor for that matter neural networks, let alone cognitive science. Lest they might gain misconceptions about what we mean by a computer, we share the following succinct elucidation from Bell's *Mathematics, Queen and Servant of Science* originally published in 1951:

> "I shall not attempt to describe a digital computer, partly for the reasons already given and partly because as this is written new and improved types of machines are being invented and manufactured in rapid succession. Commercial competition has stimulated invention, as usual. The underlying mathematics is simple enough compared to the physical and engineering problems that must be solved for actual production. Electronics is (was?) one of the most effective sciences applied in design. I have already noted the connection with a two-valued logic, an open or closed circuit, a 'yes-no,' and hence a *binary* mechanism[3].

In contrast to Bell, we do hope to describe in a most rudimentary manner, using our analog grade computer, analog computing.

III. Alternatives Considered

Sometime we hope to move to sub-2V technology, surface mount integrated circuits and a PCB implementation of the AGC. There exist digital potentiometers with a more highly multiplexed control. We chose 3-wire control since it more directly relates to manual control.

IV. ANN Element

In Zurada[3] the basic artificial neuron is represented as the combination of a synaptic summing network activation function as characterized in Figure 1, where $f(net) = net$ where

$$net = \sum^{n} w_i x_i .$$

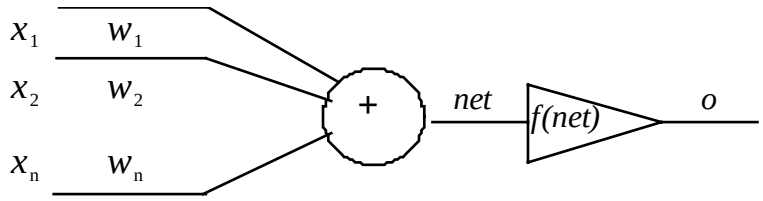

Figure 1. Weighted Dendritic Summing Network and Neuronal Processor

Here x_i are the inputs while w_i are the synaptic weights. These weights are the adjustable parameters of the neuron. The sum of all of the $x_i w_i$ ("*net*") represents the neuron activation potential. The neuron provides an output *o* via the activation function *f(net).* Note that the ability of a neuron to perform multiplication and addition, as required by the intended application.

V. Analysis

For those who routinely perform analysis using resistances and superposition of currents there is a need to supply a perspective of conductances and superposition of voltages in order to represent the application. Figure 2 shows the circuit topology whereby the voltage inputs represent grades, the conductances represent the component weights, and the voltage of the common node represents the output grade.

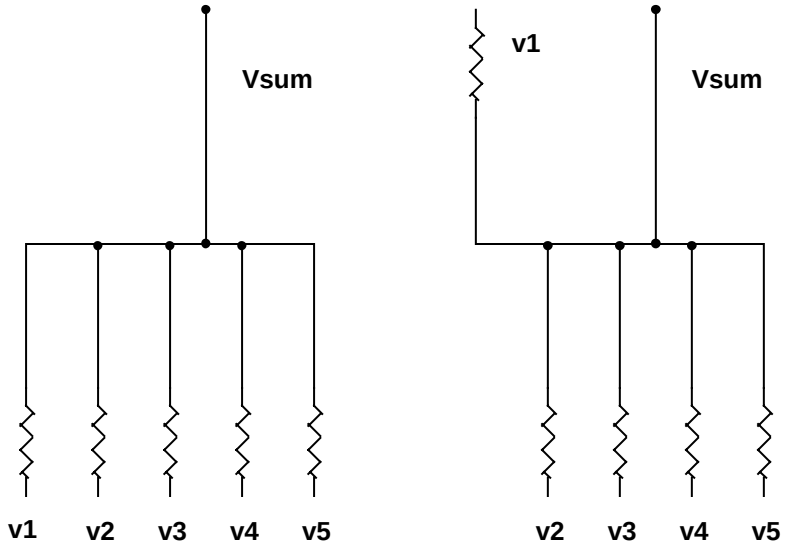

Figure 2 A redrawing (R) to exhibit voltage division from the perspective of v_1 (original, L).

In [1] we provide a detailed solution for the AGC. The critical formulas follow with intermediate results intentionally omitted:

$$V_2 = \frac{R_2}{R_1 + R_2} V \qquad (1.1)$$

Given source V and output V_2, voltage division in terms of resistances is expressed.

...

$$V_2 = V \Big/ \left(\frac{G_2}{G_1} + 1 \right) \qquad (1.9)$$

Voltage divider in terms of conductances.

Extend this to the network at hand using superposition of voltages yields:

$$v_k \; alone: v_i = 0|_{i=1}^{k-1}, v_j = 0|_{j=k+1}^{p} \qquad (2.1)$$

A way of stating that the other sources are to be shorted.

$$V_k = v_k \Big/ \left(\frac{Geq_{kothers}}{G_k} + 1 \right) \qquad (2.2)$$

Where V_k are the individual potentials at the summing node attributable to v_k alone.

$$V_k = v_k \Big/ \left(\frac{\sum_{i=1}^{k-1} G_i + \sum_{j=k+1}^{p} G_j}{G_k} + 1 \right) \qquad (2.3)$$

...

$$V_{sum} = \sum_{k=1}^{p} V_k \qquad (2.8)$$

Superpose the voltages for different v_k acting alone

$$V_{sum} = \sum_{k=1}^{p} \left(\frac{v_k G_k}{\sum_{i=1}^{p} G_i} \right) \qquad (2.9)$$

$$V_{sum} = \sum_{k=1}^{p} v_k G_k \Big/ \sum_{i=1}^{p} G_i \qquad (2.10)$$

Sum of voltage inputs * weights / sum of weights

VI. Implementation

Figure 3 depicts a practical implementation of equation (2.10). Details include 1/8 W 1% resistors and op-amps are programmed for unity gain to act as buffers. The input voltages represent composite grades * 100. The grade weights/1000 are represented as conductances. A resistance value corresponding to a conductance is easily implemented using at most two standard values.

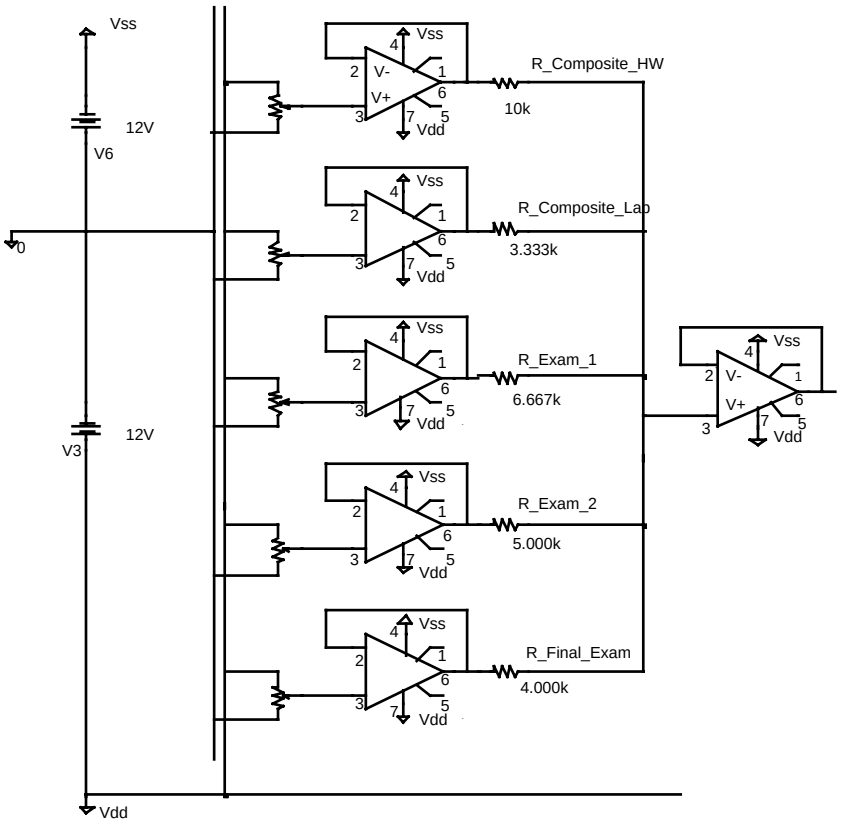

Figure 3. Weighted Grade Analog Computer Circuit

A succinct description that aids in the leap from mechanical to digital potentiometers is presented in Xicor's "A Primer on Digitally-Controlled Potentiometers":

> "There are two types of potentiometers; mechanical and electronic. The terminals of the mechanical potentiometer are called CW (clockwise), CCW (counter clockwise), and wiper. The corresponding names or designations for the terminals of the electronic version are V H or R H , V L or R L , and the wiper V W or R W . The mechanical pot is a three terminal device while the electronic pot is an integrate circuit with a minimum of eight terminals.
>
> "Xicor's digitally-controlled potentiometer (XDCP) is an electronic potentiometer whose wiper position is computer or digitally controlled. The electronic version of the potentiometer also has memory where wiper settings and/ or data can be stored. The digitally-controlled potentiometer (XDCP) is a system level control device performing a component level function. The control signals for the 3-wire bus are Up/Down, Increment, and Device Select. The Up/Down control input is a level sensitive signal which establishes the direction of the movement of the wiper. The wiper is moved on the falling edge of the Increment control input in the direction established by the Up/Down signal. The Device Select control input is like an address line and enables or disables the device."[5]

VII. Instrumentation

LabVIEW™ 6i was used for control and display.[6] Others have also embarked on undergraduate internet based instrumentation lab experiences (e.g. [4]). The overall virtual instrumentation architecture is depicted in Figure 4. The client and two servers are implemented as virtual instruments (vi). The transport services listen for connections. The server components run on a PC with a data acquistion board that is connected to the analog grade computer. The other components may run anywhere LabVIEW™ 6i is installed.

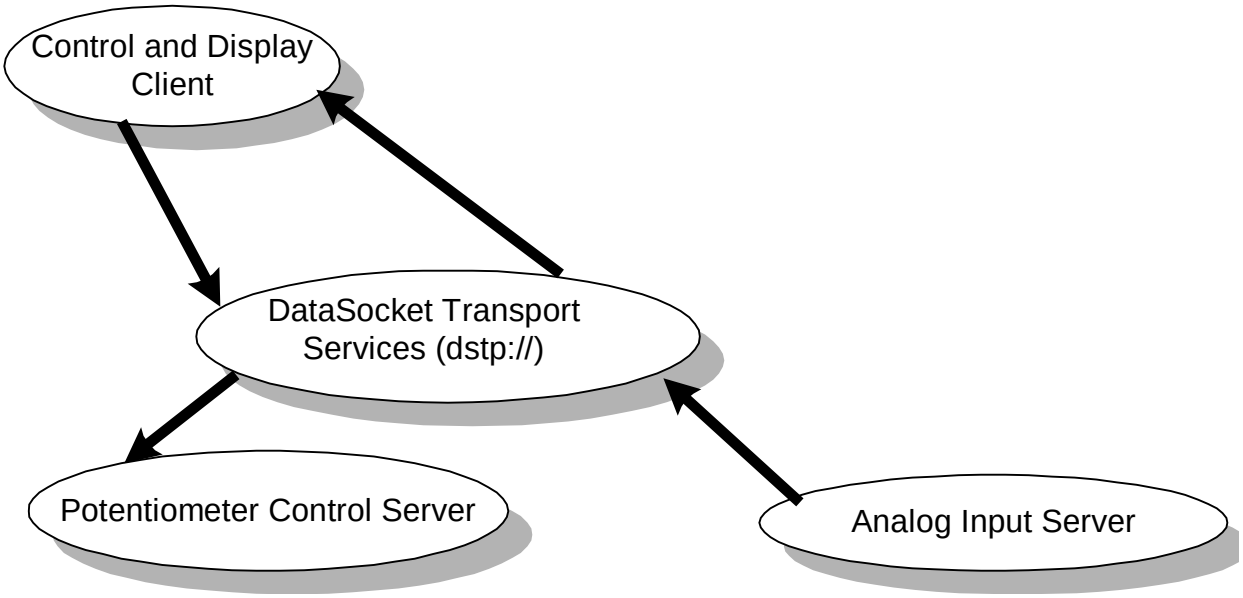

Figure 4. Distributed Virtual Instrumentation Architecture

The schedule of the sixteen LabVIEW™ DataSockets is depicted in Table 1.

Connected to the digital potentiometer server:
dstp:\\141.218.112.87\composite_homework_up_control
dstp:\\141.218.112.87\composite_homework_down_control
... and eight more for the respective components.
Connected to the analog input server:
dstp:\\141.218.112.87\composite_homework_display
... and four more for the respective components
dstp:\\141.218.112.87\grade_display

Table 1. DataSockets

Figures 5-7 depict some of the particulars of the LabVIEW™ vi-s. The DataSocket capability greatly ease the ability to "soft-wire" our system especially when compared to our prior experience in using LabVIEW™ 5 TCP/IP Sockets programming. Figure 8 depicts the users view of the system. The up/down controls require a single mouse click for each potentiometer wiper turn at a distance. Although laborious, this effort corresponds to their initial

potentiometer lab experience. Above the five controls and their corresponding displays is the display only "grade" display.

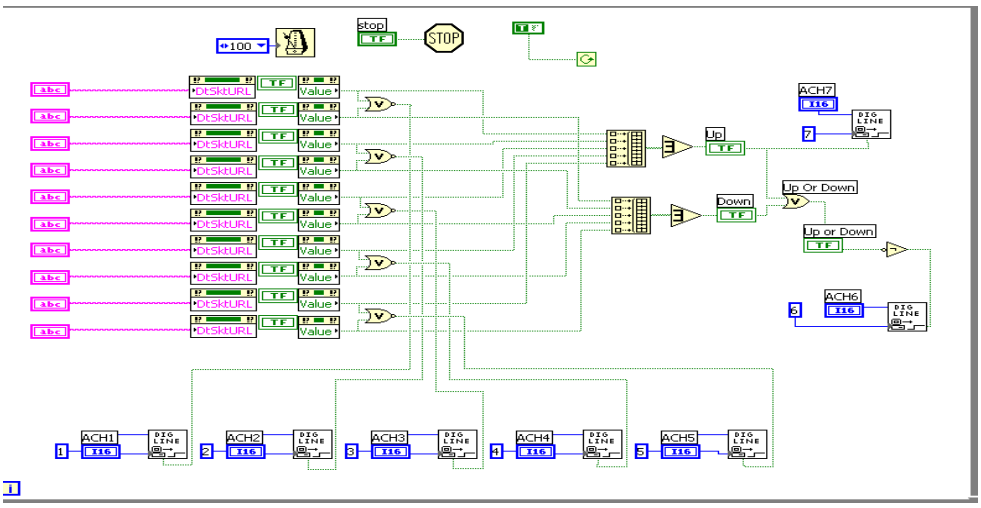

Figure 5. Digital Potentiometer Server Diagram

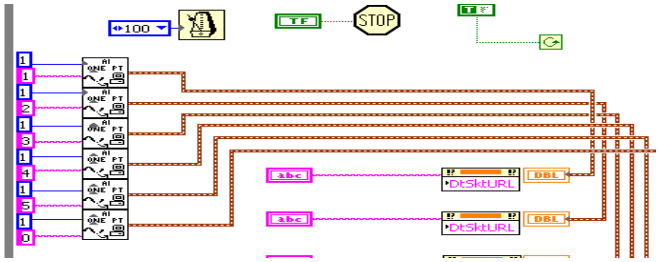

Figure 6. Portion of AGC Analog Input Server Diagram

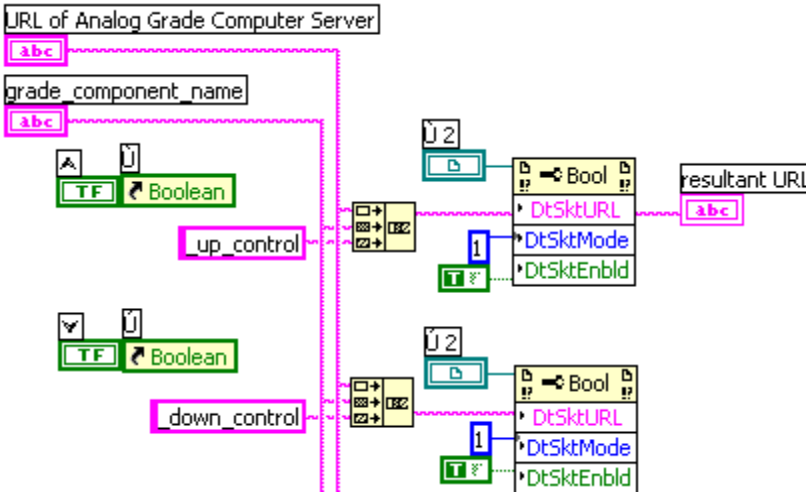

Figure 7. Portion of Sub-vi for single grade control and display unit

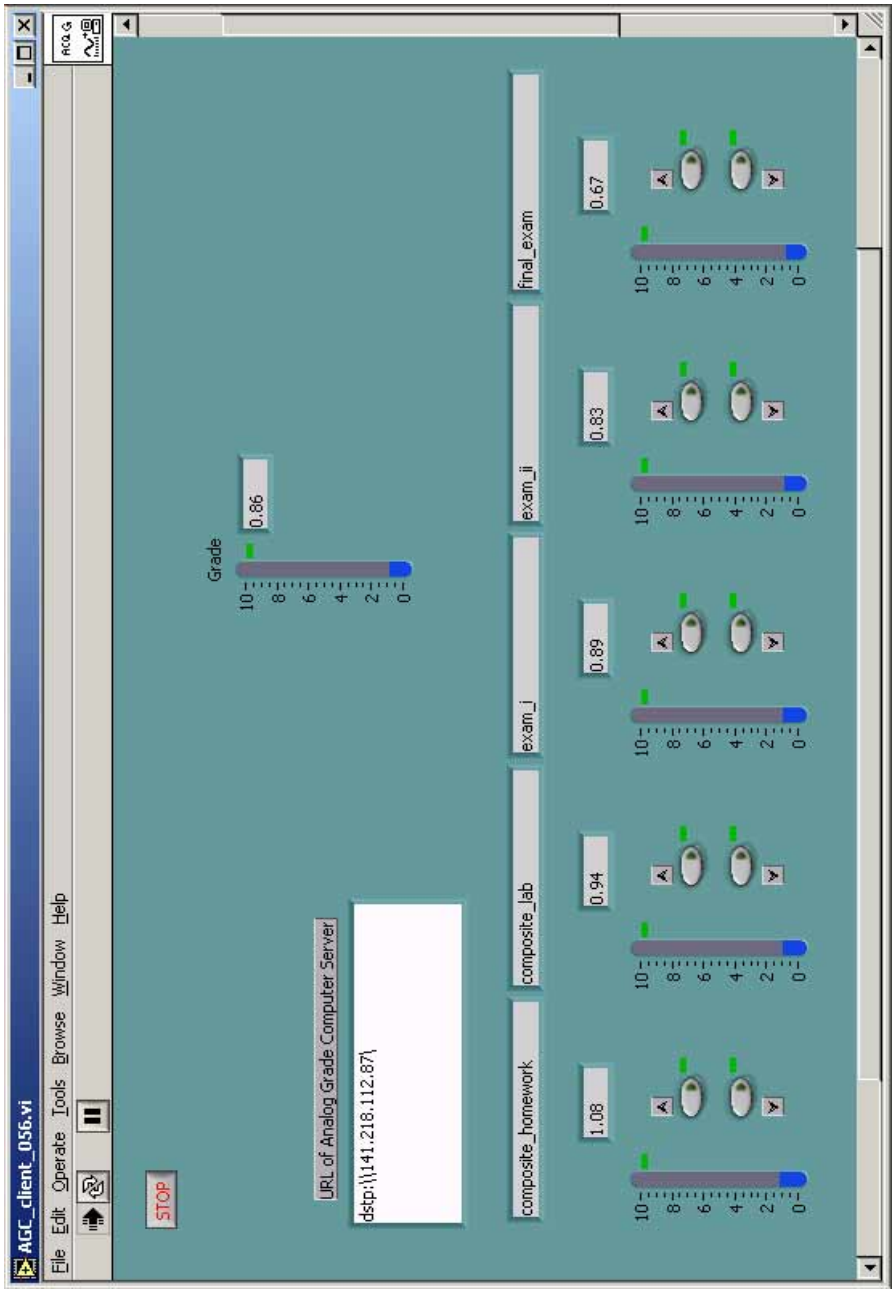

Figure 8. ACG Client Diagram

VIII. Deployment

The AGC distributed display and control using LabVIEW™ provides a recent evolutionary extension to our manual analog grade computer. Student involvement spans three, mid-semester, weeks. Unlike the focused topic laboratory experiments where we expect the student to gain competance with analysis, build, measurement and interpetation of unit concepts we treat the AGC as a supplement where the goal is awareness. The purpose of our demonstration system also serves to supplement the course text and laboratory workbook with an organically grown capability relevant to overall department efforts in web based instrumentation and instruction.

We provide a set of mandatory exercises involving the operational and grade component input portion of the AGC. Students are expected to study the physical implementation of the AGC in laboratory following their normal weekly unit. They are expected gain access to the following resources on the instructor's instructional web site using a browser from a location other than their lab:

- AGC theory
- AGC users manual
- Xicor™ digital potentiometer selection guide and product specifications
- Mandatory AGC exercises
- Extra credit AGC exercises

We proffer questions related to the superposition implementation of the grade computation for students who are seeking extra credit.

At this time we have rolled out this demonstration system to our technology oriented ECE 100 Fundamentals of Electric Circuits students. This demonstration system is their second LabVIEW™ experience. Their first LabVIEW™ experience is rudimentary and it involves the use of virtual DMM instrumentation in place of handheld or bench DMMs in voltage divider measurements.

Thus far we have discovered that the students in attempting to bring their unit experiences into this system context expose as much naiveté as perceptive insight in their responses. An example of naiveté includes the idea that the selection of a higher resistance digital pot would offer more resolution while failing to recognize such alternative component selection criterion such as a the number of wiper positions or its power consumption. An example of a successful insight is represented by some students who expressed a sense of a greater degree of control over an experiment when computer based instrumentation is used.

IX. Conclusions

We have evolved a web-deployed demonstration system that provides an early systems experience context for the application of a student's rudimentary electrical circuit knowledge. The higher level of abstraction provided by LabVIEW™ DataSockets as compared to low level sockets programming allows our distributed system to be implemented with acceptable effort. We have realized some of our multi-media, component and application modernization goals for one of our circuits course by this demonstration system. With this system development experience behind us we remain prepared to further adapt our efforts to probing our student's ability to apply unit knowledge in a system context.

Acknowledgements

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6. URL: http://www.ni.com/

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