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A Capstone Senior Design Course: Building a Simplified Computer Network

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Abstract
This paper discusses a capstone senior design course for electrical and computer engineering students. The course builds on the fundamentals of an ECE curriculum, and offers opportunities to learn new material, and to design, simulate, debug, build, and test a local area network. The six-node network that is realized uses either a Token Ring Protocol or an Ethernet protocol for sending short text messages on twisted-pair cable between network nodes. Students implement four of the Open Systems Interconnection layers: the application layer; the network layer; the data link layer; the physical layer. The node hardware consists of a Motorola 68HC11 microcontroller development board, plus additional hardware interfacing which students design and test. Working in groups of two, students appreciate the importance of exhaustive testing before connecting their node hardware to other nodes. The course includes various topics from previously taken courses: digital design (microcontroller programming, timing and interfacing); electronics (differential line drivers); electromagnetic fields (transmission lines, crosstalk, ground noise); control systems (phase-locked loop for clock recovery); electric circuits (power supply noise). The course also introduces students to new material for understanding network protocols. Once the network is functioning, students devise tests and take measurements to determine the network efficiency under various traffic conditions. This paper focuses on three questions: how is this capstone experience tied with the core courses of the curriculum; how is the course set up to meet the requirements of senior design and ABET's expectations; how other institutions can develop such a capstone experience, i.e. what should they expect from their students, and what hardware is actually needed to offer the course.

Introduction

A typical undergraduate course in computer networking focuses on the high-level behavior of networks, including their architectures, protocols and performance [1–5]. Laboratory work associated with such courses concentrates on software, using either available network cards as part of a physical network or simulating the behavior of a network [6–17]. The Electrical and Computer Engineering Department currently offers a networking course that emphasizes the lower-level operation of a network, including the physical medium, the packet format, and simplified protocols for Token Ring and Ethernet networks. In the laboratory component of the course, students realize each type of network using a microcontroller in conjunction with peripheral hardware. The

laboratory goal is the demonstration of a functioning network that can send short text messages between nodes. This course serves both as a capstone design experience and a means for introducing computer network hardware and protocols[18].

In 1997 Lafayette College redesigned its curriculum to focus on courses rather than credit hours. At that time, and in response to a growing interest in computer engineering by students applying to Lafayette, the Electrical Engineering Department decided to change its major, its degree and its name to Electrical and Computer Engineering [19, 20]. The proposal for the new program included a new course, ECE 491 Senior Project I, which was introduced to satisfy two distinct goals: provide a capstone design experience; introduce new material in the area of computer network hardware. The course is not intended to replace a typical course in computer networks, which covers material related to network architectures, protocols and performance.

The Course

Organized in a 14-week semester with two 50-minute lectures and one 3-hour laboratory period per week, ECE 491 has several goals: to learn about computer network protocols and hardware; to work on a design project that must interface properly with other groups; to evaluate the project from ethical and socially responsible points of view; to incorporate various topics from previous ECE courses. The objective towards meeting these goals is requiring students to design and realize a modest local area computer network with the application of sending short text messages between network nodes. Each group of two students must design a network node that meets the given specifications, and must demonstrate the operation of their node with all other nodes.

The project provides a team design environment by requiring students to work both within a group and to coordinate their results with other groups. Each group must test their own network node, and all groups must test the entire network together. Individual node tests are specified, but students must devise a methodology for troubleshooting the full network. Students are also responsible for devising tests for quantitatively assessing the performance of the network (i.e., measuring the network efficiency).

Throughout the design process relevant material from previous ECE courses is re-introduced to students and applied to various aspects of the design problem. The courses include: Analog Circuit Analysis; Digital Circuit Design; Computer Organization; Solid State Devices and Circuits; Signals and Systems; Control Systems. In their final reports, students must address societal and ethical implications of the project. To do this, students rely on material from their earlier course in Engineering Professionalism and Ethics.

The laboratory facility accommodates a maximum of seven groups, each group consisting of two students.

The Design Problem

ECE 491 focuses on a guided design project for realizing two types of local-area computer networks. One network uses a ring-architecture, similar to Token Ring; the other network uses a shared bus, similar to Ethernet. The project also includes the

realization of an application for sending short text messages from any node to any other node. The network protocols are specified and represent simplified versions of actual Token Ring and Ethernet behaviors. With reference to the Open Systems Interconnection model, students realize the application, network, data link and physical layers.

The course also includes a component emphasizing technical communication. Students present written results via technical memos, progress reports, and a technical report at the conclusion of the semester. A record of weekly laboratory work and results is kept in a laboratory notebook. Students give an informal oral report and demonstration to the ECE faculty when each network is successfully running. In addition to describing the technical details of the project, the technical report must also address issues relating to the manufacturability and sustainability of their network nodes, and the societal implications of a computer network

The Design Process

After discussing several approaches to the project, ranging from one with a strong emphasis on hardware (using a Field-Programmable Gate Array chip for the network node), to an approach that emphasizes software (using available network cards), students are guided to an approach that requires both hardware and software. Students use a Motorola 68HC11 microcontroller evaluation board and a peripheral USART chip (Universal Synchronous/Asynchronous Receiver, Transmitter) for serial data transmission and reception.

Hardware design includes an interface between the microcontroller buses and the USART, including miscellaneous glue logic realized using a programmable, generic-array logic chip (GAL). Students program the microcontroller for the USART interface, and for the entire network operation, using assembly language. In addition to introducing network protocols, the project also makes students aware of the practical aspects of digital system design, including the topics of power supply noise, cabling crosstalk and return path capacity, ground loops, and transmission line reflections and termination.

An important aspect of the project is the emphasis on the need for thorough testing. Before each node is permitted to connect to another node or nodes, a series of tests must be passed to guarantee proper node operation at a slow, user-controller speed. Provided in the laboratory are five test nodes that can monitor all activity on the network line, and can generate data packets. Successful completion of the node tests, however, does not always guarantee proper network operation at full speed, and students must develop a strategy for locating and fixing problems that arise in the full-speed network. The project provides an environment in which groups must coordinate their activities and cooperate with each other in order to realize a functioning network.

Because students design the network at the hardware level, the course can integrate material, which students have studied in previous courses. Analog circuit analysis is used for determining the nature of power supply spikes that result when a digital output switches between voltage levels. The use of capacitors to minimize such spikes is also studied using analog circuit analysis, as is the determination of a cable's return path

capacity. Topics from courses in solid-state electronics apply to the use of a differential line driver and receiver for access to the twisted-pair physical medium. Results from the course in signals and systems are used to determine the needed bandwidth of the physical medium for the networks[1–3]. Principles from electromagnetic field theory are used to qualitatively assess the sources of crosstalk in a system, and how to minimize its ill effects. Electromagnetic field theory also provides a basis for discussing ground loops in a system and how to minimize their effect. Topics from control systems are used to understand the operation of a phase-locked loop for recovering a clock signal from a data stream. And as befits the project, many topics from courses in digital circuit and system design are used: combinational logic design; counter design; microcontroller assembly language software; microcontroller on-chip hardware systems. At the beginning of the course students are required to complete a take-home entrance exam. This exam addresses various topics from previous courses that are used in ECE 491, and the exam provides the opportunity for students to review this material in preparation for its application to the computer network.

Although ECE 491 relies on much material from previously taken courses, it also introduces several new topics. Within our current curricular organization, the topic of microcontroller bus interfacing is not covered in the required course in digital system design. ECE 491 introduces this topic, which is essential for designing the USART-to-microcontroller interface. Also introduced in ECE 491 is the entire topic of transmission lines, including: a circuit model of a lossless line; derivation of the wave equation and its solution; a line's step and pulse responses; line reflections and termination. Reflections are analyzed through the use of both space-time diagrams and the Bergeron diagram. The Open System Interconnection model is also introduced, as well as the fundamentals of Token Ring and Ethernet protocols [21–23]. Thus ECE 491 is not entirely a capstone design experience; lectures presenting new material are an important part of the course.

ECE 491 has evolved somewhat during its four-year lifetime. The original goal was the demonstration of successful transmission and reception of text messages manually created from the computer keyboard. The original Ethernet protocol did not include collision detection and a back-off algorithm. During the second offering of the course, test nodes were made available to students to an environment for testing a node before connecting it to other nodes. During the third offering of the course, students took measurements to determine the efficiency of the Token Ring network under various traffic levels. All measured values were compared with theoretical values, and suggestions were solicited for improving the network performance. In addition, more test nodes were made available. During the fourth offering of the course, students were required to realize a second version of the Ethernet network, wherein collisions are detected and acted upon. Students were also charged with designing an environment for measuring the network efficiency [4, 5, 18].

The Development Tools

Students use a Motorola 68HC11 Evaluation Board with a processor version that includes a monitor program in ROM. The board has no memory beyond that on the processor chip; the on-chip memory includes read-write and electrical erasable read-only memory.

Students develop their code using assembly language and debug the code using the monitor program.

Students wire the USART chip, its interface logic, and the line driver chips on a breadboard, which connects to the 68HC11 buses of the development board. All the interface logic fits into one 16V8 GAL chip; students enter their logic expressions and generate a fuse map using the Universal Compiler for Programmable Logic (CUPL).

The test nodes provided consist of the same 68HC11 development boards with printed circuit boards containing the USART, interface logic and line drivers. Recycled laptop computers, which run Windows 3.1(!), are used to communicate with the test node hardware, which is jumper reconfigurable for use with either a Token Ring or Ethernet architecture.

Each bench in the laboratory is equipped with a mixed-signal oscilloscope, a signal generator, a power supply, and a desktop computer. The computers are locally networked and share a laser printer. An eighth bench houses a non-networked computer and a peripheral device for configuring programmable logic chips. The 68HC11 boards used in ECE 491 are the same as those used during the second half of the Digital Circuits II course, but the two courses are currently offered in different semesters thereby reducing demand for the boards.

Conclusion

From its inception, the course has been successful in terms of student enthusiasm, student understanding of network operation on the packet level, student appreciation of the need for thorough testing, student initiative in cooperatively troubleshooting the network, and student success in demonstrating functioning networks. The course has also successfully integrated many technical topics that students have previously studied. The project goal of realizing the networks is realistic for a semester-long course, and the project is modest in terms of necessary equipment and cost.

In the near future we plan to move the project to the Motorola 68HC12 processor, which provides more on-chip memory and faster speed. At that time students will program in a combination of C and assembly, thereby introducing students to a mixed programming language environment. Additional emphasis will be placed on an experimental determination of the Ethernet efficiency, and simulation software will be introduced to model the network performance.

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Biographical Sketch

John Greco is a professor in the Department of Electrical and Computer Engineering at Lafayette College in Easton, PA where he teaches courses and develops and teaches laboratories in the areas of digital circuits, digital systems, microcontrollers, and computer network hardware.