AC 2012-3260: A COST-EFFECTIVE AND USER-FRIENDLY SPECTRUM ANALYZER FOR EDUCATIONAL ENVIRONMENT

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A Cost Effective and User Friendly Spectrum Analyzer for Educational Environment

Abstract

This paper presents the design of an inexpensive and user friendly spectrum analyzer. This is accomplished by utilizing a variable switched capacitive filtering system in conjunction with some commonly used integrated circuits. The resulting system exhibits twelve spectral bands with constant gain and constant quality factor through the entire spectrum. Although the design considers only twelve spectral bands, with simple modifications the proposed technique can be expanded to any desired bands. The primary intention of this paper is to provide a simple method to build and utilize such an instrument in educational laboratories. Commercially available spectrum analyzers are very expensive and not feasible for underdeveloped courtiers with limited resources to obtain such expensive instruments.

I. Introduction

The Spectrum analyzers are real-time analyzers, which mean that they simultaneously display the amplitude of all signals in the frequency range of the analyzer. They provide information about the voltage or energy of a signal as a function of frequency\(^1\).

Spectrum analyzers play major roles in design of many applications in electrical signal analysis, mechanical measurements, and communications. These instruments are especially used in low frequency applications such as biomedical electronics, oceanographic measurements, electrical filters, and analysis of air and water pollution. Due to this wide variety of applications, spectrum analyzers are heavily integrated into engineering education. This integration is generally reinforced via laboratories experiments. Therefore, creating a burden on educational institutions to purchase these moderately expensive instruments. In addition, as technology grows these instruments become more complex and at times offer functionalities beyond the normal laboratories usage, thus, not fully utilized and often impractical in undergraduate laboratories. Furthermore, these complexities require more additional effort by instructors to utilize them effectively and efficiently. These problems can be resolved by designing low-cost and user friendly spectrum analyzer. One such device is available\(^2\) which is a plug-in board device that requires a personal computer. It is not uncommon for a laboratory course to require ten spectrum analyzers for each laboratories session. This requires a large number of personal computers, since the wide applications of spectrum analyzer persuade institutions to offer laboratories in several engineering disciplines simultaneously. Consequently, this approach is not cost effective for an educational environment. The alternative technique is to propose a low-cost stand-alone spectrum analyzer, this is the primary intention of this paper. This technique offers two significant advantages to educators; first, it provides a low-cost instrument that can be used in undergraduate laboratories where more expensive commercial spectrum analyzers are not available; secondly, it is suitable for use as a student project.
II. Design Approach

A common method to design spectrum analyzers consists of implementing a bank of band-pass filters followed by bank of detectors that are fed into an electronic sweep switching device. The switching device output is displayed on a CRT to provide spectral of the input signal. The block diagram of such scheme is provided in Figure-1. Such implementation, as described is very difficult due to the great number of filters that would be necessary for the desired resolution and bandwidth. To eliminate this difficulty we use a single-chip approach to filter and detector design as presented in the following sections.

![Figure-1. Block diagram of a spectrum analyzer](image)

**Single-chip Approach to Spectrum Analyzer**

In the context of the block diagram shown in Figure-1, a single-chip approach spectrum analyzer design is proposed in Figure -2. In particular, a single chip which is a variable switched capacitor filter manufactured by National Semiconductor is used to replaced the entire filtering bank of Figure-1. This filtering device is known as MF10. MF10 uses general purpose CMOS active filter building blocks that can be configured as two independent filters, configuration 1 can either be set as an all-pass, a high-pass, or a notch filter, configuration 2 can be set as a low-pass or a band-pass filter. In this approach only the band-pass feature is utilized, this is known as mode 1 of MF10 usage. The center frequency of this band-pass filter can be either directly dependent on the clock frequency or it can dependent on both the clock frequency or external resistor ratios. As it will be shown later the proposed method uses the latter approach. In addition, an analog demultiplexer is used to replace the detector bank of Figure-1. The proposed method considers the design of a twelve-band spectrum analyzer. This is achieved by controlling the clock of the MF10 via a frequency multiplexer. The inputs of this multiplexer are provided by twelve outputs from twelve outputs of two ripple counters. The input to this ripple counter is generated through a 1MHz frequency oscillator. The control signal for both frequency multiplexer and the analog demultiplexer are provided through a binary counter. The outputs of
the analog demultiplexer are the spectrum of the input signal. These outputs can be displayed on any LCD or a similar device using proper drivers. It should be noted that to further reduce the cost, a common signal generator can be used to replace the oscillator.

The proposed spectrum analyzer is designed to provide twelve band of frequencies, ranging from 10Hz to 20kHz with center frequencies of 9Hz, 19 Hz, 39 Hz, 78Hz, 156 Hz, 312Hz, 625 Hz, 1.25kHz, 2.5kHz, 5kHz, 10kHz, and 20kHz. Since the MF10 divides its clock frequency by 50, the oscillator must generate 1MHz clock in order for the ripple counter to produce this range of frequencies. In what follows the details of each sub-block of Figure 2 will be explored.

![Figure-2. Block diagram of proposed spectrum analyzer](image)

**Filtering**

As cited earlier the filtering portion of the design is accomplished using the MF10 Universal Monolithic Dual Switched Capacitor Filter, as shown in Figure-3. This filter is configured in mode 1 to provide the band-pass characteristic. The input signal is fed into pin 4 to produce an output at pin 2. The biasing circuit consists of three resistors that controls the gain and the quality factor of the filter. The main advantage of Figure-3 implementation is that its output dependents on the values of these three resistors only with low sensitivity and the precision of the input clock. Hence, the fine tuning of the gain and the quality factor are solely depend on the precision of the clock. Since, the available technology allows precise clock implementation with ease, the proposed scheme further simplifies the difficulties associated with filtering design \(^3,4\).
Since the input clock of the MF10 is provided by one of the outputs of ripple counters, a multiplexing scheme is needed to generate the proper clocks. The control circuit to generate the proper clock sequencing is the binary counter circuit shown in Figure-5.
Multiplexing

The outputs of the ripple counter must ultimately be presented as clocks to the MF10 sequentially. This necessitates the use of multiplexing scheme similar to one shown in Figure-6. This configuration utilizes two digital multiplexers, 74LS151. These multiplexers are cascaded via enable/disable pins. This is done by enabling one chip at the time with the binary address D. As it was mentioned previously, a binary counter is used to select the appropriate input clocks to be transmitted to the output of the multiplexers.
**Demultiplexing**

Next, the band-pass output of the MF10 is needed to be captured. Since this output consists of twelve different frequencies, the demultiplexing scheme is required to be implemented. This is achieved by utilizing two cascaded analog demultiplexers, CD4051, as shown in Figure-7. Similar to the multiplexing scheme, the binary counter controls the transmission of the analog signal from the MF10 to the output of demultiplexers. Furthermore, the address D will be used to control the enable/disable pins of the chips. In addition, to ensure a positive input voltage a diode is connected to the input of the demultiplexers.

![Figure 7. Analog Demultiplexer](image)

**Detector**

This section presents a method to ensure the stability of the outputs of the demultiplexer as well as to prevent misrepresentation of the input signal spectrum. Such undesirable condition may occur while the MF10 switches between the twelve bands. Figure-8 presents a scheme to accomplish this task. This system which consists of a peak detector and a delay circuit is placed between the output of the MF10 and the input of the demultiplexer. The time constant of the delay circuit needs to be long enough to sustain the voltage signal for the binary counter, however, short enough to show a decrease in the voltage when the signal is no longer presented. For this application a 1μF and a 2MΩ resistor are selected to allow a long time constant that is needed for the MF10 signal to get through (MF10 makes a complete sweep once every 0.9 seconds). The final output can be measured or displayed using any common device.
III. Conclusion

A cost effective 12-band spectrum analyzer was presented. This analyzer is designed to produce spectrum of low frequency signals ranging from 10 Hz to 20 kHz. This instrument is low-cost, easily implemented, offers a robust gain and high quality factor, and user friendly in comparison to the existing spectrum analyzers. Additionally, it is suitable to be used as a student project. The design lends itself nicely to increasing the number of bands in the spectrum, although for illustration purposes only 12-band was considered in this paper.

References