A DATA ACQUISITION SYSTEMS ENGINEERING COURSE

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Abstract

Teaching of data acquisition devices and systems belongs to a relatively standard program in electrical and computer engineering. The course is usually linked with data communications. There exist various textbooks covering some of the necessary topics on the theory and design of data acquisition systems. The advent of microprocessors has increased the need for more data acquisition designers. This need cannot be satisfied by the standard university program alone. Continuing education programs must be devised to address the needs of practising engineers and technologists who require newer or better skills in their design of digital systems. This paper describes a course on the architectures and design of data acquisition systems. The course is organized specifically for practising engineers and technologists. It can also be modified for undergraduate teaching. The paper discusses the topics covered, tutorials, projects and laboratory, as well as the student evaluation scheme.

OUTLINE

1. WHY INDUSTRIAL TRAINING?
2. INDUSTRIAL TRAINING AT IAMC.
3. THE IDP STRUCTURE.
4. VERTICAL & HORIZONTAL IDP COURSE OFFERING.
5. DATA ACQUISITION SYSTEMS ENGINEERING (DASE).
   - A. COURSE STRATEGY.
   - B. COURSE STRUCTURE.
   - C. DASE SYLLABUS.
   - D. COURSE UPDATING.

1. WHY INDUSTRIAL TRAINING?

PROBLEM

- TREND
  1960's - THE DECADE OF ELECTRONICS
  1970's - THE DECADE OF (MICRO)COMPUTERS
  1980's - THE DECADE OF VLSI?
  ROBOTS?

- TOO FEW DESIGNERS
  1979 - 17 K COMPUTER ENGINEERS (CEs) PRODUCED
  1990 - 1 M CEs REQUIRED

- IF ALL UNIVERSITIES PRODUCED CEs ONLY, THE NUMBER WOULD BE < 1M

SOLUTION

- UNDERGRADUATE & GRADUATE PROGRAMS (UNIVERSITIES & COLLEGES)
- CONTINUING EDUCATION (UNIVERSITIES)
- INDUSTRIAL TRAINING (INSTITUTES, CENTRES)

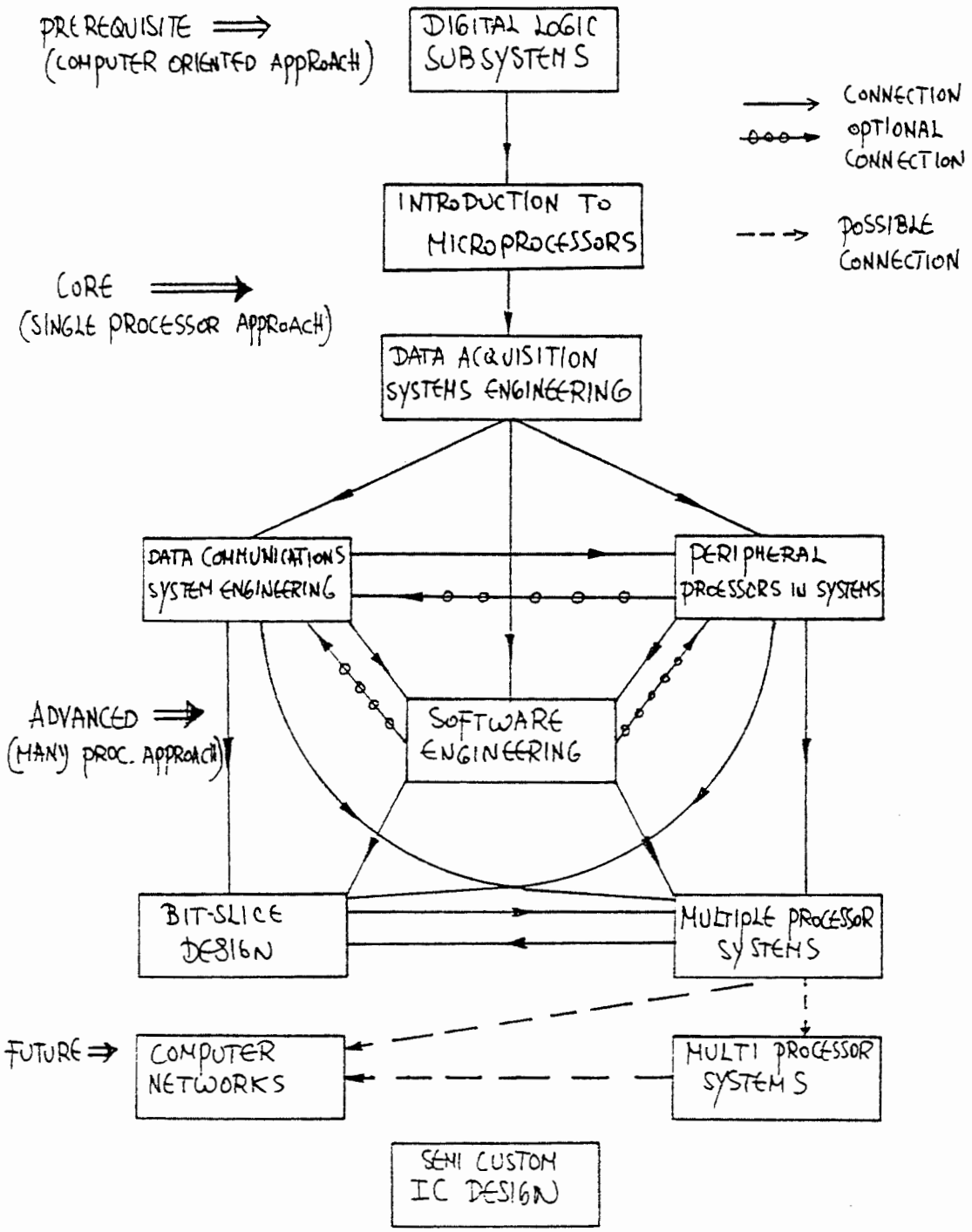
2. INDUSTRIAL TRAINING AT IAMC

1. In-Depth Program (IDP)
2. Technical Awareness Program (TAP)
3. Management Awareness Program (GAP)
4. General Awareness Program (GAP)

3. THE IDP STRUCTURE

- 8 courses
- Each course 12 weeks
- One evening session per week
- Three hours of lecture per session
- Two hours of lab/tutorial per session
- One assignment per session
- One individual project per course
- < 25 participants per course
- Lecture notes
- Textbooks, manuals, data books
- Fess $300 to $700

VERTICAL & HORIZONTAL
IDP COURSE OFFERING



5. DATA ACQUISITION SYSTEMS ENGINEERING (DASE)

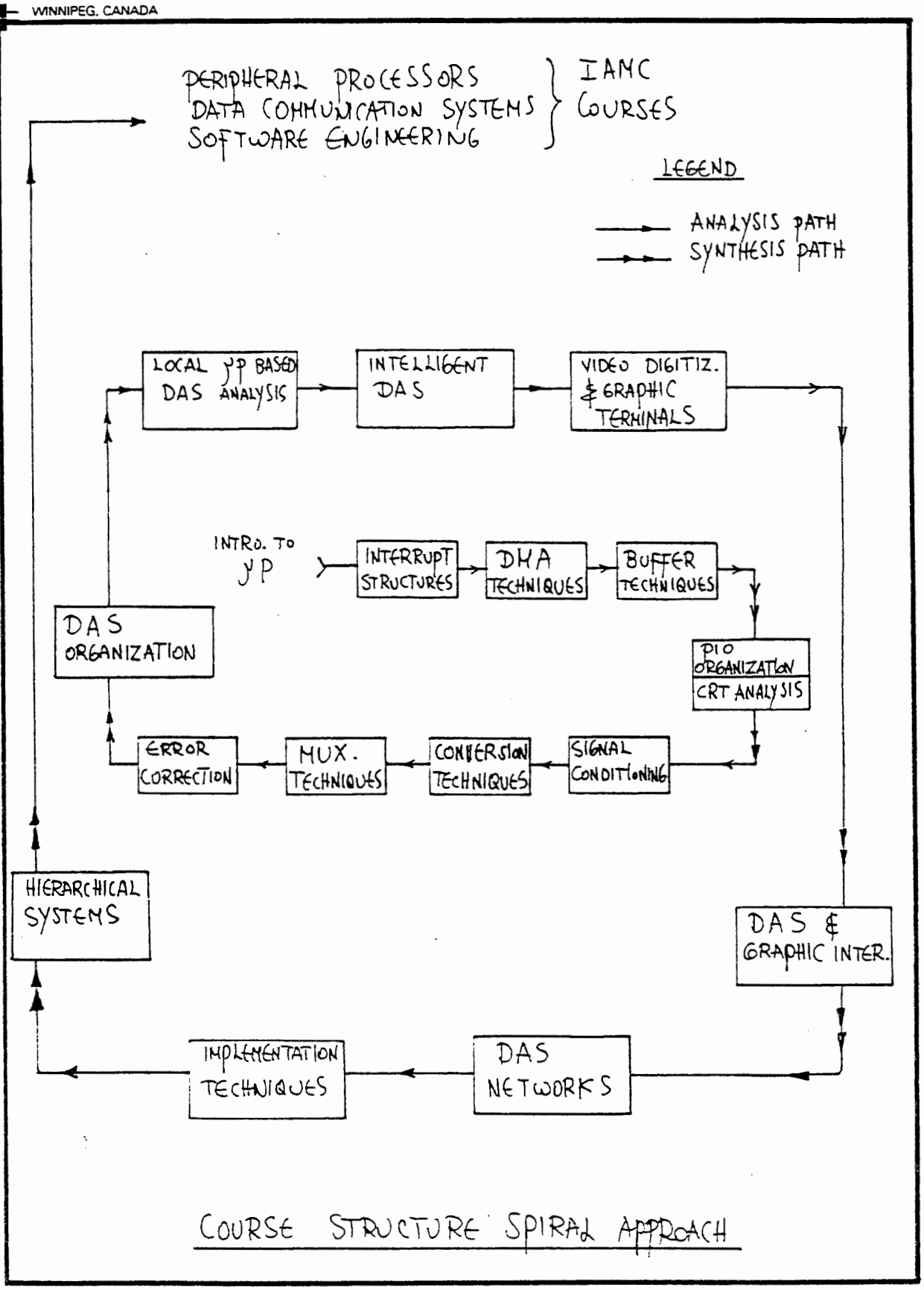
A. COURSE STRATEGY
B. COURSE STRUCTURE
C. COURSE SYLLABUS
D. COURSE UPDATING
(FIELD TRIPS → LECTURE/ASSIGNMENT/LAB/PROJECT)

A. COURSE STRATEGY

1. How to cope with technology changes in a μP-based data acquisition course?
   - Conceptual, hardware-independent approach
   - Hardware approaches:
     - Chip
     - Board/Subsystem
     - System
   - Essential support of vendor's literature
   - Individual projects
   - Dynamic tutorials

2. The analysis - synthesis approach
   - Analysis of architecture
     - components
     - subsystems
     - systems
   - Design of systems
     - dedicated
     - general

3. Structure
   - Lecture
   - Tutorial
   - Take-home lab
   - Demo lab
   - Project
   - Assignment



COURSE STRUCTURE SPIRAL APPROACH

C. DASE SYLLABUS

1. INTERRUPT STRUCTURES
   - 1.1 Single Level Priority Structure
     - .1 Skip Chain
     - .2 Daisy Chained, Automatic Polling
   - 1.2 Multilevel Priority System
   - 1.3 Two Dimensional Priority Structures
   - 1.4 Rotating Priority Structures
   - 1.5 Multilevel + Rotating Priority Structures
   - 1.6 Interrupt Triggering/Timing

2. INTERRUPT PROCESSING
   - 2.1 Direct Vectored Interrupt
   - 2.2 Indirect Vectored Interrupt
   - 2.3 Context Switching

3. INTERRUPT STRUCTURES IMPLEMENTATION
   - 3.1 Two Dimensional
   - 3.2 Multilevel
   - 3.3 Rotating Priority
   - 3.4 Combination
   - 3.5 Dynamic Reconfiguration of a Priority System

4. DMA TECHNIQUES
   - 4.1 DMA Organization
   - 4.2 DMA Modes
     - .1 Single Transfer
     - .2 Block Transfer
     - .3 Demand Transfer

C. DASE SYLLABUS (CONT'D)

- 4.3 DMA TRANSFER TYPES
  - .1 READ TRANSFER
  - .2 WRITE TRANSFER
  - .3 MEMORY TO MEMORY TRANFER
  - .4 VERIFY TRANSFER
  - .5 NON-CONTIGUOUS TRANSFER
  - .6 AUTO INITIALIZATION
- 4.4 DMA PRIORITY STRUCTURES
  - .1 FIXED PRIORITY
  - .2 ROTATING PRIORITY
  - .3 INTERRUPT AND DMA

5. BUFFER TECHNIQUES
   - 5.1 DOUBLE BUFFER
   - 5.2 SWINGING BUFFER
   - 5.3 FIFOs
   - 5.4 CIRCULAR BUFFER
   - 5.5 DUAL-PORT MEMORY
   - 5.6 INTERPROCESSOR BUFFER (WINDOW)
   - 5.7 DISK/MAG BUFFERS

6. PIO ORGANIZATION
   - 6.1 MODULAR REGISTER BASED ORGANIZATION OF A PIO
   - 6.2 PIO REGISTERS
   - 6.3 INT
   - 6.4 DMA

C. DASE SYLLABUS (CONT'D)

6.5 BUFF
6.6 PIU CONT
6.7 INTELLING PIU
6.8 CO-PROCESSOR, PERIPHERAL CONTROLLER

7. SIGNAL CONDITIONING
   7.1 INSTRUMENTATION AMP
   7.2 ISOLATION AMP
   7.3 CMRR & IMRR
   7.4 PGA; MUL D/A
   7.5 NON-LINEAR D/A
   7.6 S & H, PEAK DETECTORS

8. CONVERSION TECHNIQUES
   8.1 SUCCESSIVE APPROXIMATION
   8.2 DUAL AND QUAD SLOPE
   8.3 VOLTAGE TO FREQUENCY CONVERSION
   8.4 VIDEO A/D. ULTRA FAST CONVERSION TECHNIQUES
   8.5 NON-LINEAR CONVERSION TECHNIQUES

9. FLOATING MEASUREMENTS
   9.1 GUARDED A/D
   9.2 NOISE REDUCTION
   9.3 FLYING CAP ALTERNATIVES

C. DASE SYLLABUS (CONT'D)

10. MULTIPLEXING TECHNIQUES
    - 10.1 SINGLE ENDED MUX
    - 10.2 DIFF. MUX
    - 10.3 QUASI DIFF. MUX
    - 10.4 DIFF. WITH DRIVEN GUARD
    - 10.5 FLOATING DIFF. GUARDED MUX
    - 10.6 FLYING CAP
    - 10.7 SCANNING METHODS
        - .1 SERIAL
        - .2 RANDOM ACCESS
    - 10.8 HIGH SPEED CORRECTION OF ERRORS
    - 10.9 AUTOMATIC CORRECTION OF ERRORS

11. SIMULTANEOUS CONVERSION TECHNIQUES
    - 11.1 TIMING OF A DATA ACQUISITION CHAIN
    - 11.2 STANDARD THROUGHPUT ENHANCEMENT TECHNIQUES
    - 11.3 SIMULTANEOUS CONVERSION (VECOTR, S & H)
    - 11.4 SIMULTANEOUS CONVERSION USING MONOLITHIC SA A/D
    - 11.5 SIMULTANEOUS CONVERSION DUAL-SLPE A/D
    - 11.6 ISOLATION AND SIMULTANEOUS CONVERSION
        - .1 V→F
        - .2 SIMUL. FLYING CAP
        - .3 ISOLATION AMP.

12. ANALOG DATA DISTRIBUTION
    - 12.1 NON-SIMULTANEOUS
    - 12.2 NON-SIMULTANEOUS (DOUBLE BUFFERED D/A)
    - 12.3 ISOLATION, CURRENT DRIVE, LIVE ZERO

C. DASE SYLLABUS (CONT'D)

13. DIGITAL INPUT/OUTPUT
    - 13.1 ISOLATION TECHNIQUES
    - 13.2 SCANNING METHODS
    - 13.3 INTRODUCTION TO PLC (PROGRAMMABLE LOGIC CONTROLLER)

14. ORGANIZATION OF A DATA ACQUISTION SYSTEM (DAS)
    - 14.1 PIO ORGANIZATION
    - 14.2 LOCAL µP BASED DAS
    - 14.3 DAS

15. VIDEO DIGITIZATION AND SYNTHESIS
    - 15.1 VIDEO DIGITIZATION TECHNIQUES
    - 15.2 VIDEO RAM DESIGN
    - 15.3 INTRODUCTION TO SEMI-GRAPHIC COLOR RASTER-SCAN
    - 15.4 INTRODUCTION TO FULL-GRAPHIC COLOR RASTER-SCAN
    - 15.5 NOISE IMUNITY

16. DAS NETWORKS
    - 16.1 NETWORK CONFIGURATION
    - 16.2 IMPLEMENTATION TECHNIQUES
    - 16.3 HIERARCHICAL SYSTEMS

D. COURSE UPDATING

1. Field Trips to Pertinent Companies
   - NEC
   - OCTEC
   - Elscint
   - Matrox

2. Seminars (=0.5 IAMC + 0.5 Manufacturer's Designers)
   - Intel
   - Motorola
   - National Semiconductor
   - Texas Instruments
   - Mostek
   - Analog Devices
   - Intensil

3. Workshops
   - Hewlett-Packard
   - Tektronix

COURSE AUTOMATON