A Junior Level FPGA Course in Digital Design Using Verilog HDL and Altera DE-2 Board For Engineering Technology Students

by

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Abstract

This FPGA course is designed for junior level students who are pursuing a baccalaureate degree in electronics and computer engineering technology. Exercises were adapted for use of the Altera DE-2[6] development board, which were donated by Altera cooperation. Software used was Quartus II, which is freely available from Altera website. The board was found to be useful and student-friendly for majority of the laboratory exercises and for simple design projects.

Introduction

Use of a hardware description language, such as VHDL or Verilog to program a programmable logic device, has become very common basis for digital design laboratories. The programmable logic devices themselves have become capable of handling greatly increased amounts of logic, allowing more and more complex design to be programmed into more and more affordable logic devices. These programmable devices are capable of handling many inputs and can produce several outputs. The course, which was taught, was based on both combinational and sequential logic design.

Software Installation on PC[1, 6]

The Quartus II software is freely available from Altea website, for the laboratory use a license was acquired through Altera university education division. Following are the steps to download software from Altera website:

- Go to Altera website and click on software download
- Click on Quartus II Web Edition[1] Software
- In order to successfully download, fill out the form submit the request for downloading
- Once the form is filled out, it should lead to the download manager page. From there determine where you want to save the installation file.
- Once the download is complete, launch the Quartus software and follow the steps provided from the wizard
- After the software has been is installed successfully, a license file is required to run. This license file could be obtained from Altera website[1]. To install this file follow these steps:

1. Go to start ⇒ Run
2. Type *cmd* or *command*
3. Type *ipconfig/all*
4. Write MAC address of the Ethernet adapter
5. Go to Altera site and click on licensing and follow the steps
6. A license file will be e-mailed to you
7. Save that file in Quartus folder
8. Now you are ready to use Quartus software

Designing Combinational and Sequential Circuits

The Quartus II software provides three options for designing circuits;

- Schematic capture
- Using VHDL
- Using Verilog HDL

For this course, Verilog HDL was used to design logic circuits. Detailed instructions were provided to students about creating source files, using Altera DE-2[6] board, compiling source file, making pin assignments for *Cyclone II EPC35F672C6* device, and downloading compiled file to the Altera DE-2 board.

FPGA Structure

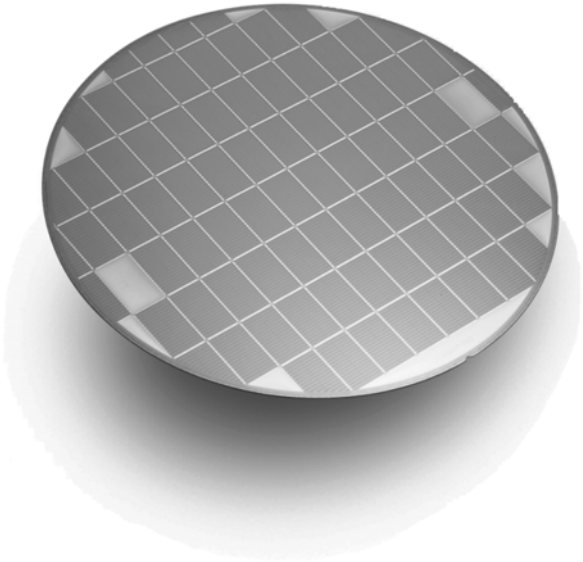


Fig 1: Silicon Wafer [2]

	Year					
	2006	2007	2008	2009	2010	2012
Technology feature size	78 nm	68 nm	59 nm	52 nm	45 nm	36 nm
Transistors per cm^2	283 M	357 M	449 M	566 M	714 M	1,133 M
Transistors per chip	2,430 M	3,061 M	3,857 M	4,859 M	6,122 M	9,718 M

Fig 2: Silicon Technology Evolution [3]

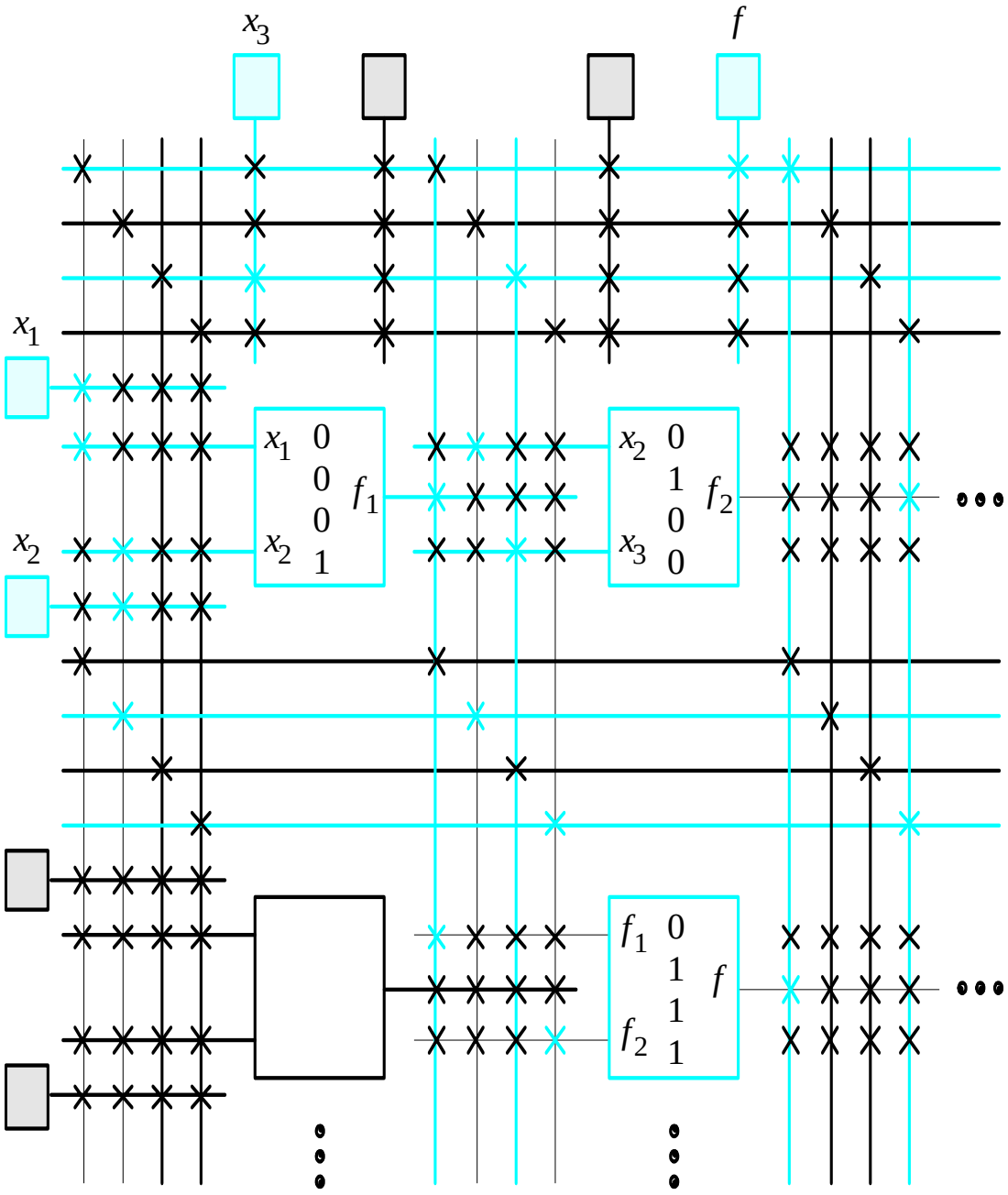


Fig 3: Internal Structure of a Programmed FPGA [4]

Fig 4: A Generic Design Flowchart [5]

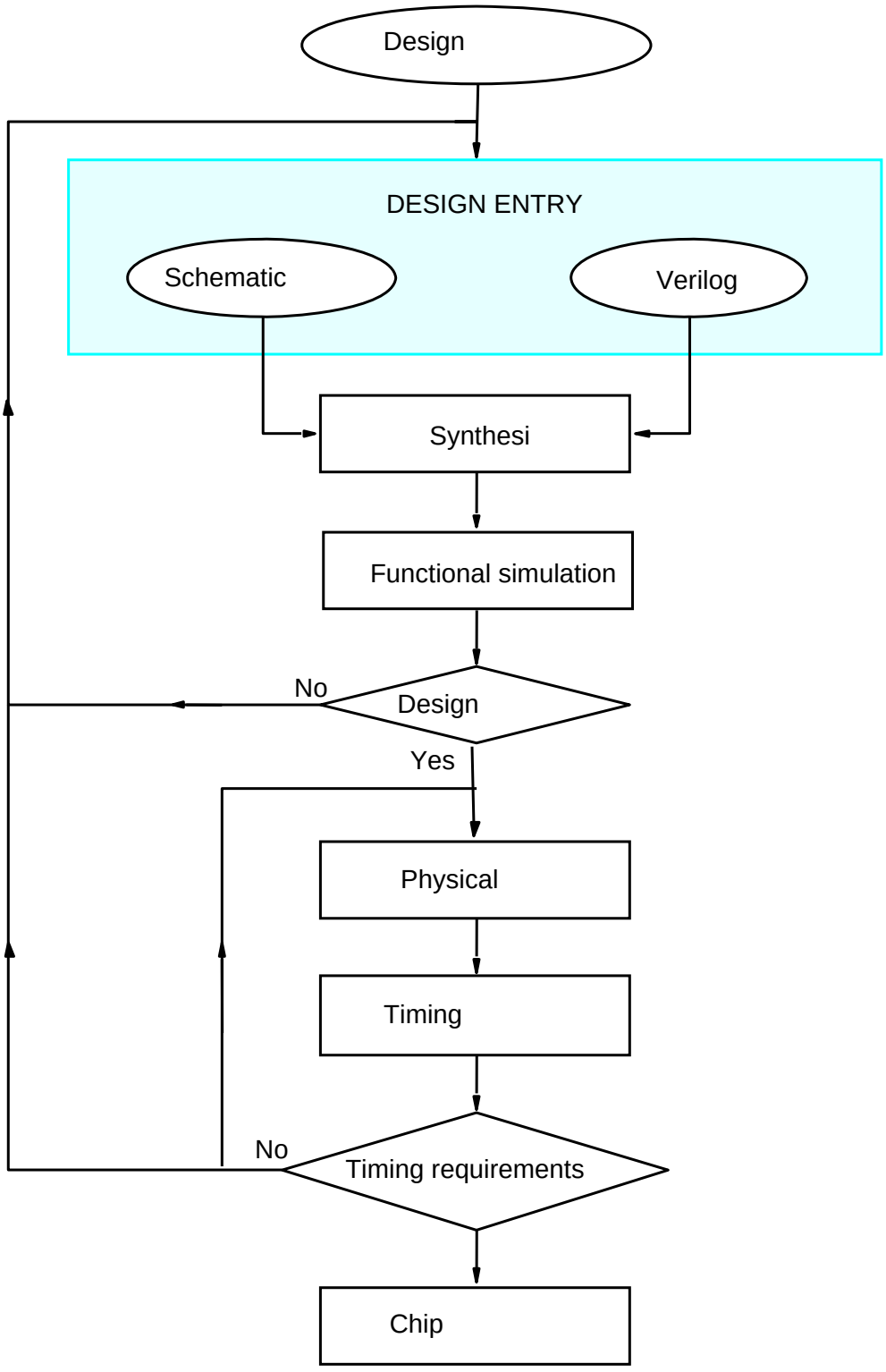
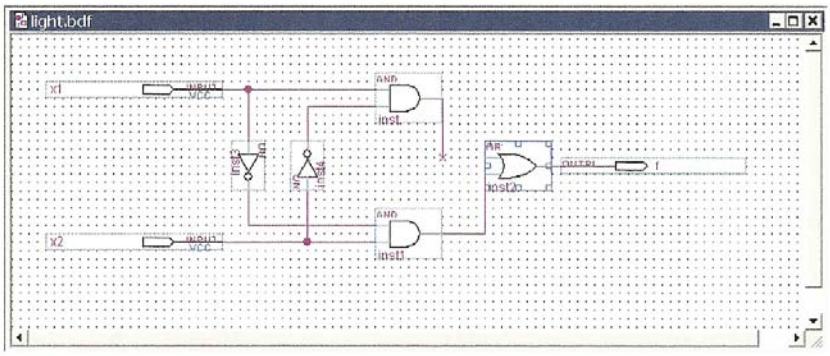
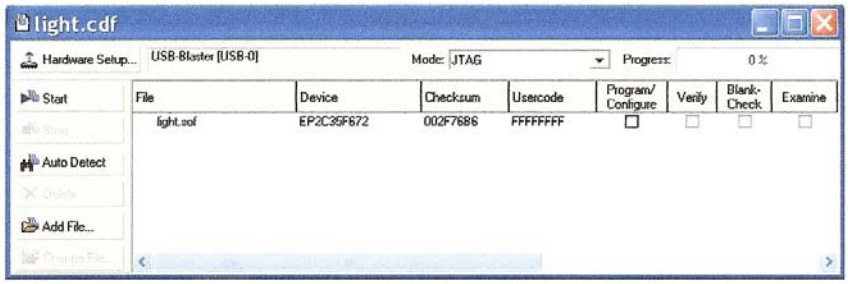
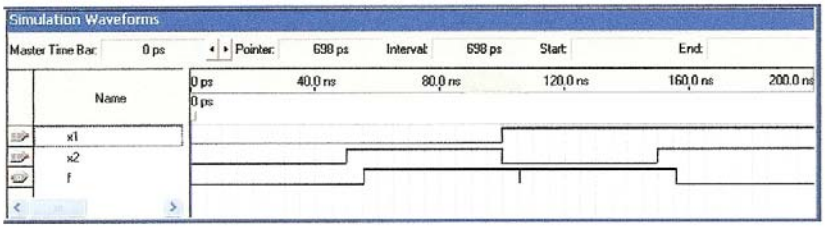


Fig 5: A Simple Simulation Test Using Schematic Capture[6]







Simple Combinational Design Verilog Code for k-bit 2x1 Mux and k-bit Adder

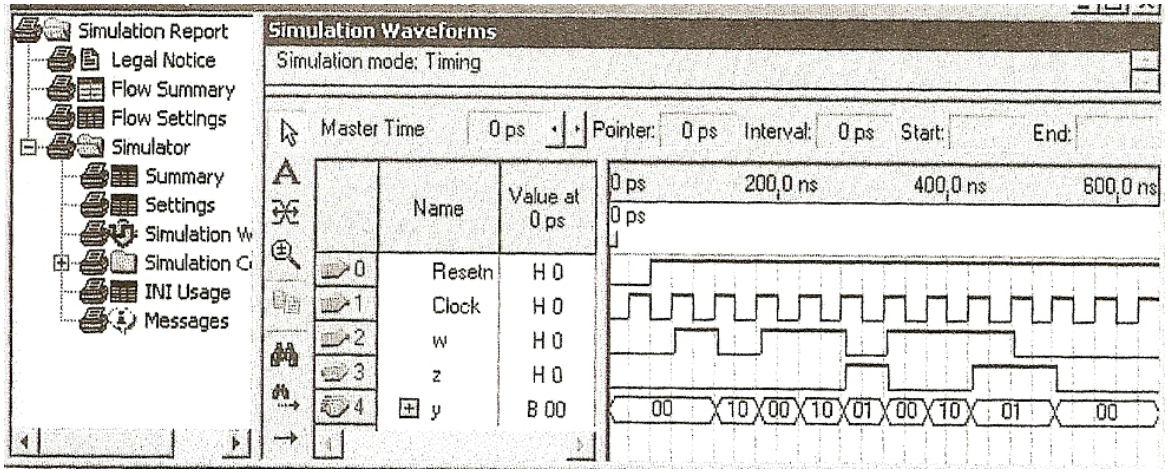
```
// k-bit 2-to-1 multiplexer
module  mux2to1 (V, W, Selm, F);
    parameter k = 8;
    input  [k−1:0] V, W;
    input  Selm;
    output  [k−1:0] F;
    reg  [k−1:0] F;

    always @(V or W or Selm)
        if (Selm == 0)  F = V;
        else  F = W;
endmodule

// k-bit adder
module   adderk (carryin, X, Y, S, carryout);
    parameter k = 8;
    input  [k−1:0] X, Y;
    input  carryin;
    output  [k−1:0] S;
    output  carryout;
    reg  [k−1:0] S;
    reg  carryout;

    always @(X or Y or carryin)
        {carryout, S} = X + Y + carryin;
endmodule
```

Fig 6: A Typical Simulation Result of Test Run Using Verilog[5]



Sequential Circuit Code For 2-bit BCD Counter

Verilog Code

```
module BCDcount (Clock, Clear, E, BCD1, BCD0);
    input Clock, Clear, E;
    output reg [3:0] BCD1, BCD0;

    always @(posedge Clock)
    begin
      if (Clear)
      begin
        BCD1 <= 0;
        BCD0 <= 0;
      end
      else if (E)
        if (BCD0 == 4'b1001)
        begin
                BCD0 <= 0;
                if (BCD1 == 4'b1001)
                        BCD1 <= 0;
                else
                   BCD1 <= BCD1 + 1;
        end
        else
          BCD0 <= BCD0 + 1;
    end

endmodule
```

Laboratory Experiments

1. Introduction to Quartus II[6] software
2. Introduction to combinational logic and Verilog
3. Multiplexes and Decoders
4. Introduction to Flip-Flops
5. Counters
6. State Machine Design[2]
7. Projects

Conclusions

The FPGA course was successfully taught and provided students with good basic knowledge of Verilog HDL. The Altea DE-2[6] board is user friendly and students had no problems using it. In the future more complex projects will be assigned to students using faster clocks and LCD display, which are on board features. This course will be made a required core course in the future, which will follow combinational logic and sequential logic courses. I had inquires from several companies who are looking for students with FPGA design experience. I think this course fits very well in Electronics and Computer Engineering Technology curriculum.

References

1. Altera Cooperation, Quartus II Web Edition Software, March, 2007
2. Mano, Morris M., Digital Design, 3rd Edition, Prentice-Hall, Inc., 2006
3. McGrath, Dylan, "FPGA Market to Pass $2.7 Billion by '10", May 24, 2008
4. Chang, K.C., Digital System Design with VHDL and Synthesis, IEEE CS, 2006
5. Sandige, Richard S., Digital Design Essentials, Prentice-Hall Inc., 2002
6. Altera Cooperation, FPGA University Program Tutorial Using Verilog HDL, 2008

Biography

Tariq Qayyum graduated from University of Engineering and Technology Lahore, Pakistan with BSEE degree in 1978 and with MSEE degree from Rochester Institute of Technology, Rochester New York in 1982. He has been teaching at Cal Poly Pomona since 1986. His interest includes digital design, microprocessors, and programming languages.