2006-131: A PRINTED CIRCUIT BOARD DESIGN PROJECT FOR A SWITCHING POWER CONVERTER

Biswajit Ray, Bloomsburg University

Christopher Root, Bloomsburg University

2006-131: A Printed Circuit Board Design Project for a Switching Power Converter

Biswajit Ray

Dr. Ray is an Associate Professor of Electronics Engineering Technology (EET) at the Bloomsburg University of Pennsylvania. He also serves as the Coordinator of the EET program.

Christopher D. Root

Chris is an undergraduate student at the Bloomsburg University of Pennsylvania. He looks forward to completing his B.S.E.T. degree in Electronics Engineering Technology in May 2006. Chris will continue his studies to obtain a Master of Engineering degree in Electrical Engineering.

A Printed Circuit Board Design Project for a Switching Power Converter

Abstract
A printed circuit board design project is presented through the development and testing of a dc-to-dc switching power converter for pulse load applications. Electrical design of power converter integrates the knowledge students have gained in previous courses such as circuit analysis, electronics, electrical machines, control systems, semiconductor devices, and thermal analysis. Use of industry-standard electronic design automation tools was emphasized in the prototype development process including schematic entry and printed circuit board layout. In order to achieve a high density design, use of surface mount components was emphasized over through-hole components. Populating the printed circuit board with surface mount components was carried out through an in-house solder reflow process using a standard toaster oven. The concepts of testing methodologies for high power circuit boards and optimizing the feedback control loop were introduced as part of this project experience.

Introduction
The design, printed circuit board (PCB) layout, circuit card assembly, and testing of a transformer-based 360 W dc-to-dc switching power converter based on pulse-width modulation technique and voltage/current feedback is presented in this paper. The input to the power converter varies between 24 and 32 V while the output is regulated at 30 V for operation from no-load (0 W) to full-load (360 W). The project required custom magnetics design and stability analysis for the feedback control loop.

The schematic entry and board layout were carried out using *Multisim* and *Ultiboard* software, respectively. A four-layer board was designed with two layers primarily dedicated to ground plane. The *Gerber* files were uploaded to a board manufacturers' server in order to get the PCB manufactured. The board was populated with surface mount parts using an in-house solder reflow process before hand-soldering the through-hole parts. The populated board was then tested thoroughly including optimization of the control-loop to meet the load transient specifications. The loop gain and phase plots were obtained using a frequency response analyzer. Changes incorporated to the power converter design to improve its overall performance are also discussed herein.

This design project provided an opportunity to a senior-level undergraduate student to incorporate and integrate knowledge gained in various EET courses by designing a power converter utilizing modern electronic design automation (EDA) and testing tools via a semester-long credit-bearing independent research course.

Power converter specifications
Input voltage: 22 – 32 VDC
Output voltage: 30 VDC ± 5%
Output voltage ripple: 1% (peak-to-peak)
Output load: 0 A (no-load) to 12 A (full load)
Isolation: Not required
Undervoltage lockout: ON @ 21 V and OFF @ 19 V
Switching frequency: 200 kHz
Full-load efficiency: ≥ 85%
Protection scheme: Cycle-by-cycle current limit

Power converter topology
Based on the input and output voltage and full-load power (360 W) specifications, a transformer isolated forward converter[1] topology was selected for the design. To protect the converter from excessive current draw due to under voltage conditions, an undervoltage lockout (UVLO) circuit was implemented that turns on the converter when input voltage exceeds 21 V and turns it off when it is under 19 V. Figure 1 shows the startup regulator and the associated UVLO circuit employing op-amp based hysteresis circuit. The startup regulator charges the bias supply capacitors with a maximum current of about 100 mA with a set maximum voltage of 14 VDC. The timeout period for the startup circuit is programmed through R12 and C4.

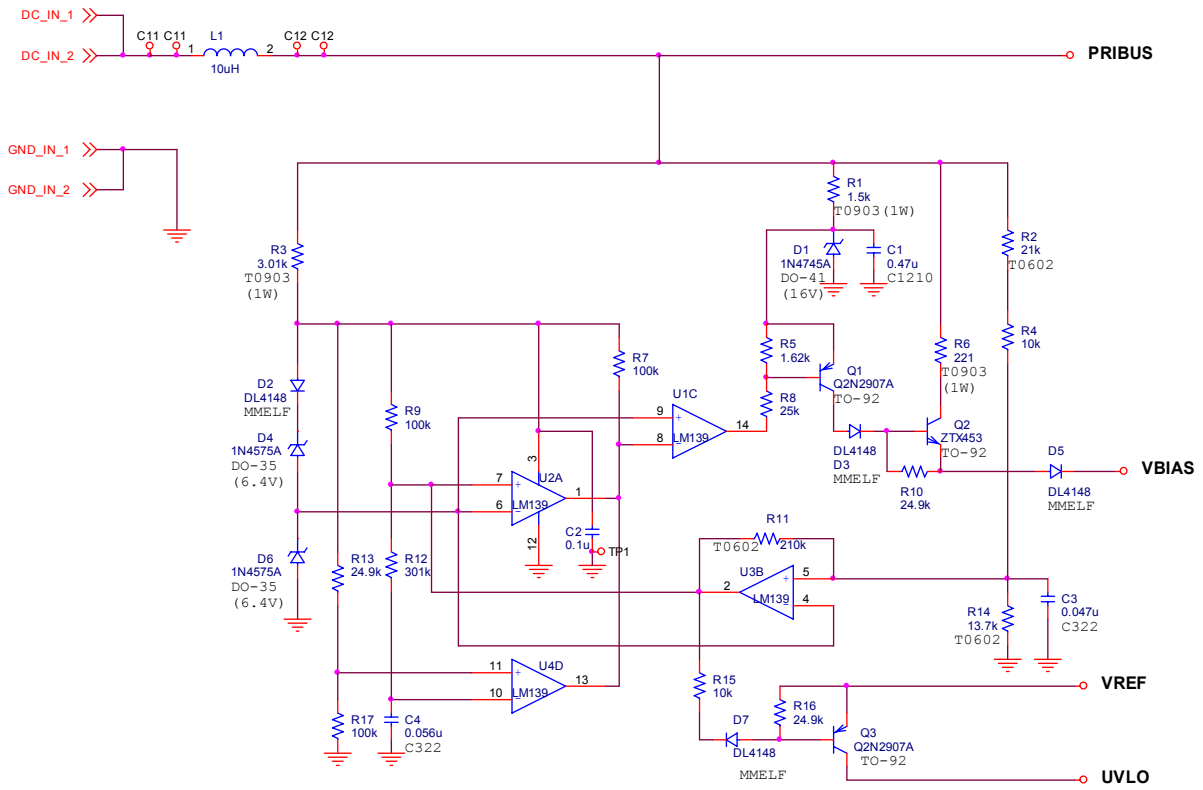


Figure 1 Startup and UVLO circuit for the power converter.

The forward topology based power stage for the converter is shown in Figure 2. In addition to the input and main output windings, the transformer includes core-reset winding and bias power winding. The primary current is sensed using a current-sense transformer and the voltage equivalent of the sensed current is fed back to the pulse-width modulation (PWM) controller IC. As shown in Figure 2, two MOSFETs (M1 and M2) are used in parallel as the primary switch to reduce the conduction loss at the expense of increased switching loss. Switching times, however, are minimized by using a dedicated high current driver IC (TC4420).

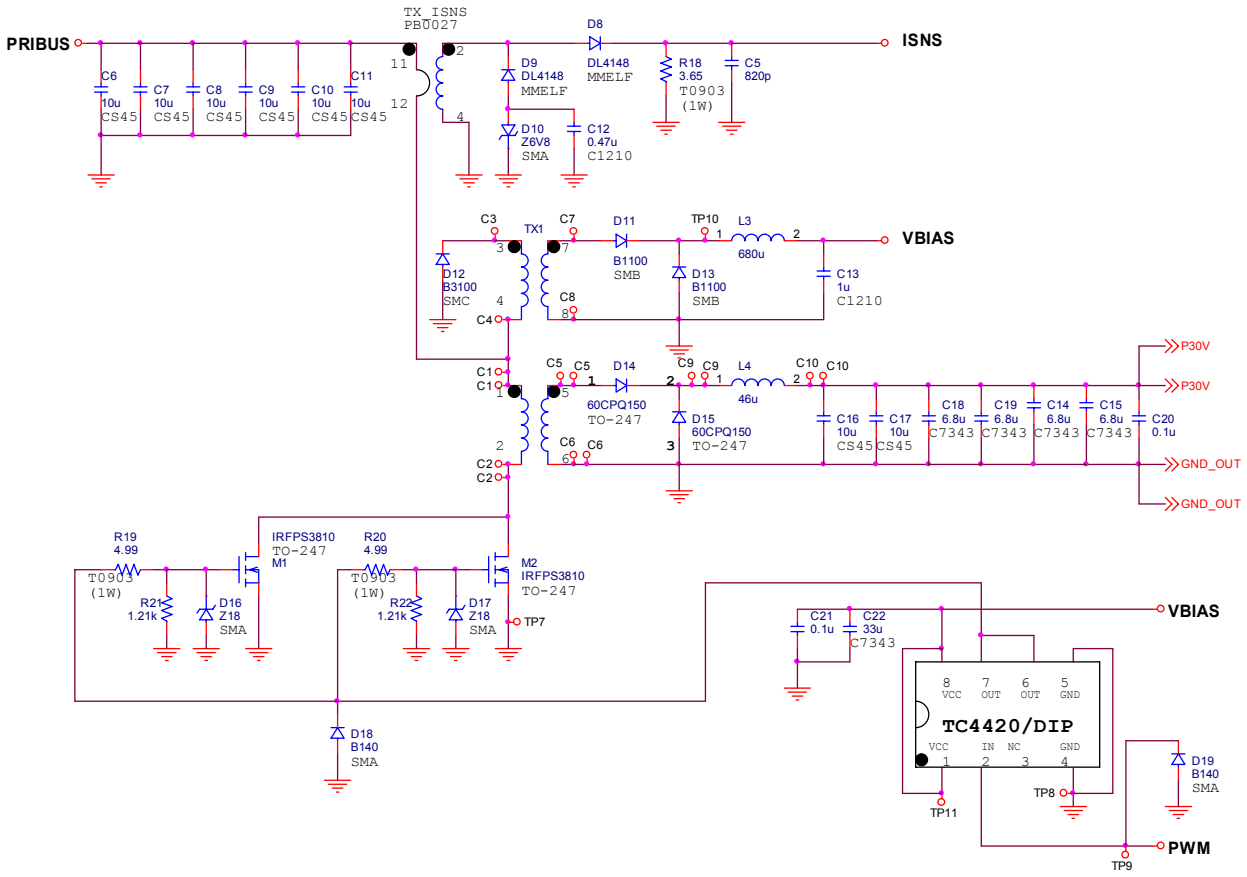


Figure 2 Main power stage of the power converter.

The PWM controller configuration for the power converter is shown in Figure 3. A current-mode control[2] scheme is implemented using output voltage as well as primary current feedback signals providing a built-in cycle-by-cycle current limit feature. A controller with an integrator, two zeroes, and two poles was implemented using R28, R31, R30, C29, R26, C28 and C26 to optimize the feedback control loop. A discrete soft-start feature was implemented using R29, C30, and Q5. Required slope compensation[2] for the current feedback loop was implemented using R25 and Q4.

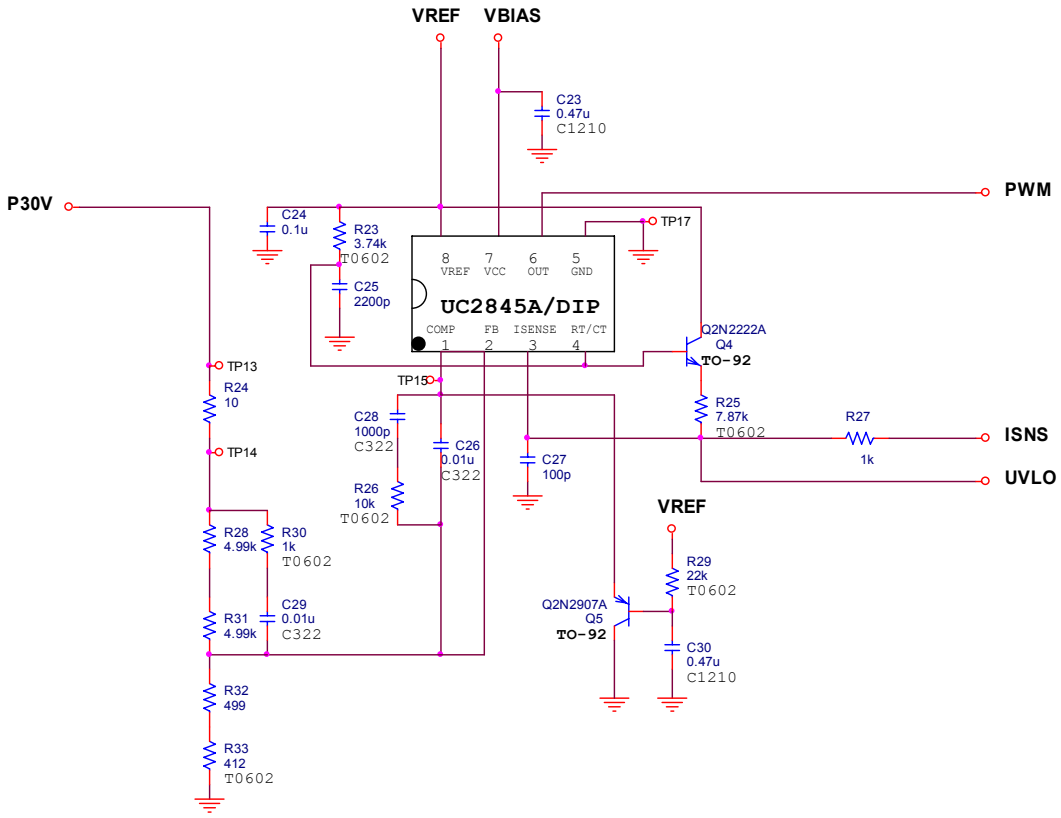


Figure 3 PWM control circuit for the power converter.

Forward converter design

Based on the input and output design specifications, the range of duty ratio was calculated to be from 0.26 to 0.45 assuming a transformer turns ratio of 11:3. The transformer was designed using an ungapped P42/29-3F3 soft ferrite pot core from Ferroxcube[3]. The primary and main output windings consisted of 9 and 3 strands of AWG #20 Litz wire[4,5] of 3/36/40 design, respectively. The reset and bias windings consisted of 30 gauge magnet wires of 2 and 1 strands, respectively. Next, the required values of filter components were calculated using the following design equations[1].

$$L_{filter} = \frac{V_{out}(1-D_{\min})}{2 f_{sw} I_{out\_\min}} \tag{1}$$

$$C_{filter} = \frac{V_{out}(1-D_{\min})}{8 V_{riple,p-p} L_{filter} f_{sw}^2} \tag{2}$$

Where, L_{filter} is the required inductance value to maintain continuous current conduction from full-load down to the minimum load (I_{out_min}), V_{out} is the output voltage, D_{min} is the minimum duty ratio, f_{sw} is the switching frequency, and $V_{ripple,p-p}$ is the allowable peak-to-peak ripple voltage in the output.

Using the above equations for the 30 V output, the required filter inductance is 46 μH and the filter capacitance is 10 μF. However, the filter capacitance used in the design is a parallel combination of two high current/low ESR 10 μF multilayer polymer capacitors[6] in parallel with four 6.8 μF low ESR tantalum surface mount capacitors to achieve low ESR and to limit voltage droop during load transients. The filter inductor was designed using a gapped soft ferrite pot core (P36/22-3F3-E250 from Ferroxcube[3]) with an air gap of 1100 μm and a winding consisting of nine strands of AWG #24 magnet wire.

EDA software usage

The schematic entry and the associated parts list creation for this design were carried out using *Multisim*[7] software. A complete parts list created using *Multisim* is shown in Table I. Surface mount components include resistors, capacitors, current sense transformers, diodes, and signal transistors. Through-hole components include resistors, energy storage capacitors, power semiconductor devices, power inductors, and power transformer.

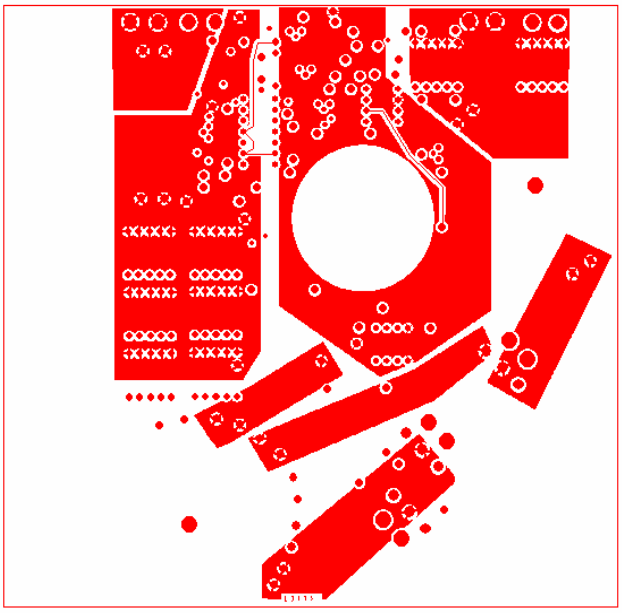
The printed circuit board layout was completed using *Ultiboard*[7] software after importing the netlist and ratsnest from *Multisim*. Custom footprints for power magnetics and power semiconductor devices with heat sink were defined within *Ultiboard*. A four-layer board was designed with through-hole components placed on the top layer and surface mount components placed on the bottom layer. The second layer from the top and the bottom layer were used primarily as ground plane in order to provide a low impedance ground path for the power converter board. The top layer and third layer from the top were used primarily for high current power planes to support high *di/dt* and high *dv/dt* paths. Figure 4 shows the copper layers for the power converter board. In addition to these copper layers, top and bottom silk screens, top and bottom solder mask, and solder paste for the bottom (surface mount) layer were created in *Ultiboard* for completing the printed circuit board artwork. Altogether, nine *Gerber* files were created and uploaded to a board manufacturer's server. The blank boards were received within a week of placing the order with PCBexpress[8].

Populating the power converter board

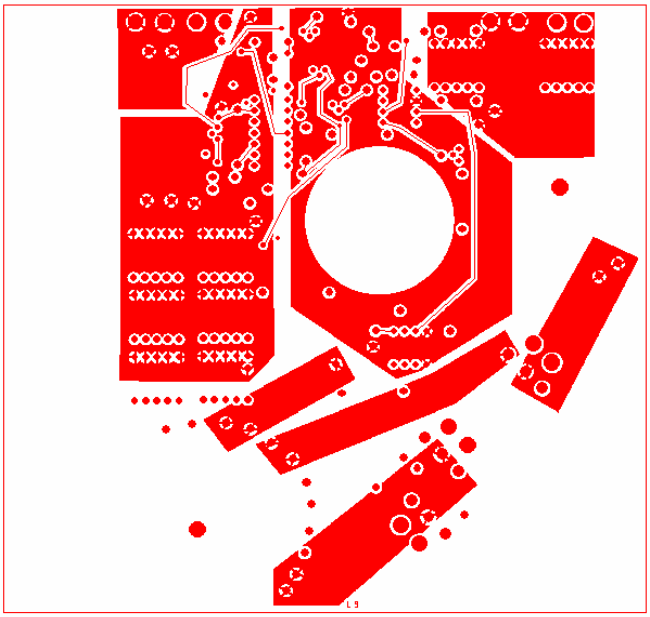
Surface mount components were placed on the board before hand-soldering through-hole parts. A stencil for the surface mount side of the board was ordered from PCBexpress[8] using the solder paste file created in *Ultiboard*. An in-house solder reflow process was used to place surface mount parts on the board. First, solder paste was applied on the surface mount side of the board using the stencil as shown in Figure 5. Next, the surface mount parts were placed on the board by hand. Finally, the board with surface mount parts was placed inside a toaster oven as shown in Figure 6. With the oven set in broil mode and the temperature set to maximum (475^{o}F), the solder reflow process was visually monitored through the glass door. The oven was turned off after observing proper solder reflow at the pads of the parts. The board was then removed form the oven and immediately inspected for adequate reflow at all of the surface mount pads. The total reflow time required for the board was just under ten minutes. Upon completion of the solder reflow process for surface mount parts, through-hole parts were placed on the top side of the board and hand soldered. Pictorial views of the through-hole and surface-mount sides of the board are shown in Figures 7 and 8, respectively.

Table I Complete Parts List

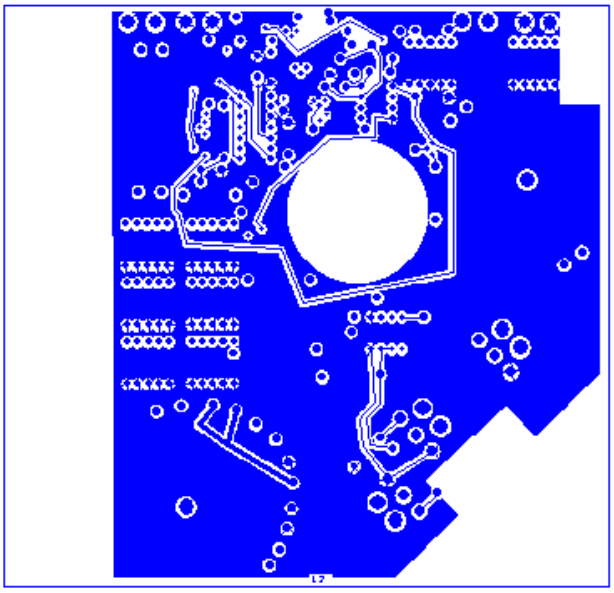
Item	Qty.	Ref. Designator	Value	Package	SM/TH	Polarized ?
1	4	C1,C12,C23,C30	0.47u	C1210	**SM**	
2	4	C2,C20,C21,C24	0.1u	C1206	**SM**	
3	1	C3	0.047u	C322	TH	
4	1	C4	0.068u	C322	TH	
5	1	C5	820p	C1206	**SM**	
6	8	C6,C7,C8,C9,C10,C11,C16,C17	10u	CS45	TH	Yes
7	1	C13	1u	C1210	**SM**	
8	4	C14,C15,C18,C19	6.8u	C7343	**SM**	**Yes (Band: +)**
9	1	C22	33u	C7343	**SM**	**Yes (Band: +)**
10	1	C25	2200p	C1206	**SM**	
11	2	C26,C29	0.01u	C322	TH	
12	1	C27	100p	C1206	**SM**	
13	1	C28	1000p	C322	TH	
14	1	D1	1N4745A	DO-41	TH	Yes
15	6	D2,D3,D5,D7,D8,D9	DL4148	MMELF	**SM**	**Yes (Band: K)**
16	2	D6,D4	1N4575A	DO-35	TH	Yes
17	1	D10	Z6V8	SMA	**SM**	**Yes (Band/Notch: K)**
18	2	D13,D11	B1100	SMB	**SM**	**Yes (Band/Notch: K)**
19	1	D12	B3100	SMC	**SM**	**Yes (Band/Notch: K)**
20	2	D14,D15	60CPQ150	TO-247	TH	Yes
21	2	D16,D17	Z18	SMA	**SM**	**Yes (Band/Notch: K)**
22	2	D19,D18	B140	SMA	**SM**	**Yes (Band/Notch: K)**
23	1	L1	10uH		TH	
24	1	L3	680u		**SM**	
25	1	L4	46u		TH	
26	2	M1,M2	IRFPS3810	TO-247	TH	Yes
27	3	Q1,Q3,Q5	Q2N2907A	TO-92	TH	Yes
28	1	Q2	ZTX453	TO-92	TH	Yes
29	1	Q4	Q2N2222A	TO-92	TH	Yes
30	1	R1	1.5k	T0903	TH	
31	1	R2	21k	T0602	TH	
32	1	R3	3.0k	T0903	TH	
33	2	R4,R15	10k	R1206	**SM**	
34	1	R26	10k	T0602	TH	
35	1	R5	1.62k	R1206	**SM**	
36	1	R6	220	T0903	TH	
37	3	R7,R9,R17	102k	R1206	**SM**	
38	4	R8,R10,R13,R16	24.9k	R1206	**SM**	
39	1	R11	210k	T0602	TH	
40	1	R12	301k	R1206	**SM**	
41	1	R14	14k	T0602	TH	
42	1	R18	3.6	T0903	TH	
43	2	R19,R20	4.7	T0903	TH	
44	2	R21,R22	1.21k	R1206	**SM**	
45	1	R23	3.74k	T0602	TH	
46	1	R24	10	R1206	**SM**	
47	1	R25	7.87k	T0602	TH	
48	1	R27	1k	R1206	**SM**	
49	1	R30	1k	T0602	TH	
50	2	R28,R31	4.99k	R1206	**SM**	
51	1	R29	22k	T0602	TH	
52	1	R32	499	R1206	**SM**	
53	1	R33	412	T0602	TH	
54	1	U1	LM139	DIP-14	TH	Yes
55	1	U2	4420	DIP-8	TH	Yes
56	1	U3	UC2845A	DIP-8	TH	Yes
57	1	XFMR_Isense			**SM**	**Yes (Dot: Pin 1)**
58	1	XFMR_Power			TH	Yes



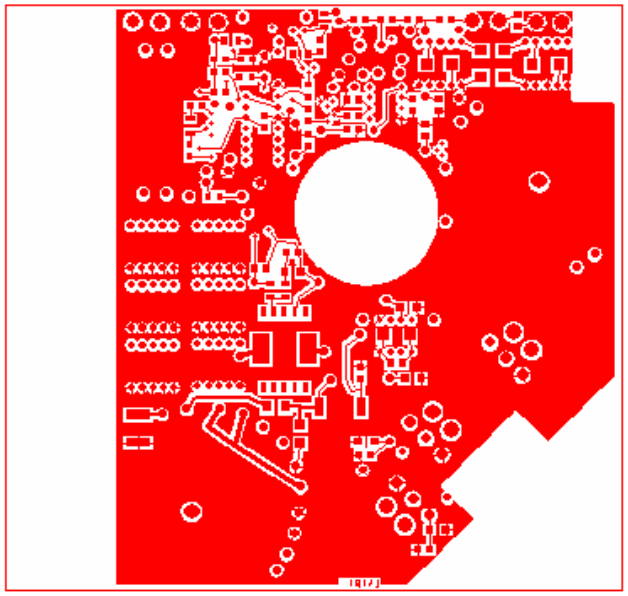
(a) Top (component) layer



(c) Third layer



(b) Second layer



(d) Bottom (surface mount) layer

Figure 4 Copper layers for the forward converter board.

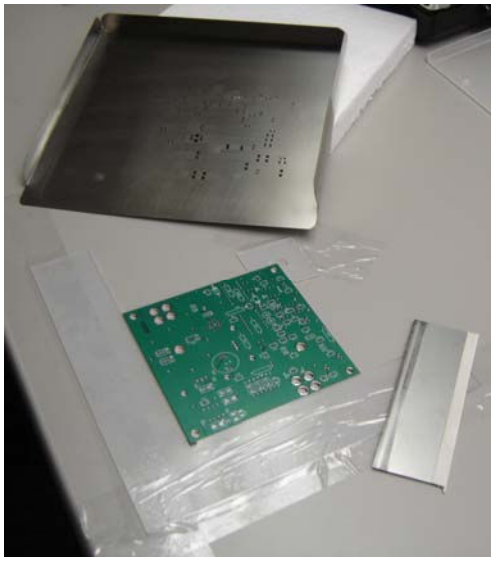


Figure 5 Stencil for the surface mount components and the blank board.

Figure 6 In-house solder-reflow process using a toaster oven.

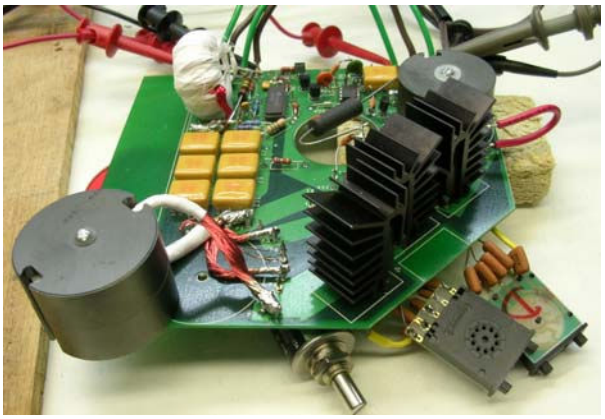


Figure 7 Pictorial view of the through-hole side of the board.

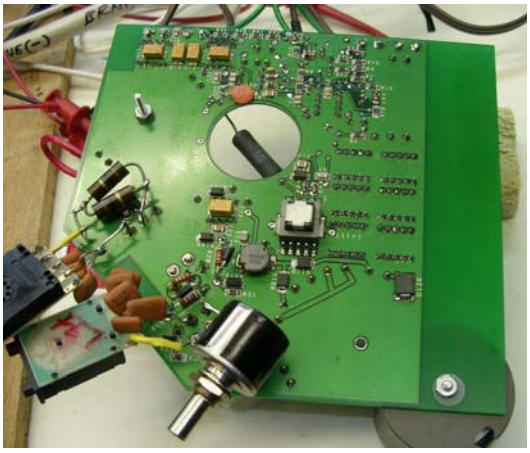


Figure 8 Pictorial view of the surface mount side of the board.

Testing the power converter board

Once the board assembly was completed, the first test carried out was to make sure that there are no shorts between the input rails, output rails, and between the high sides of input and output. The subsequent major testing steps included UVLO limits, minimum load current limit, converter operation under increased load, voltage regulation against load and input voltage variations, converter efficiency as a function of load, switching noise and waveforms, startup transients, load transients, and converter control loop optimization.

Output regulation was achieved after the converter was powered up for functional testing under light load conditions. However, the efficiency was only about 60%, indicating an excessive power loss in the unit. A closer look at the unit revealed that the power transformer was getting very hot, identifying the source of the problem. Further study of the converter waveforms showed that the transfer of current between the main output diodes (D14 and D15) was too slow,

indicating high leakage inductance[5,9] in the transformer. Also, the transformer core was getting extremely hot due to one of the winding terminations inadvertently making electrical contact with the core. This caused an unwanted current flow in the soft ferrite core whose resistance was estimated to be 38 Ω. Excessive loss in the core was justified based on its resistance and the operating voltage level. This finding led to the redesign of the transformer with a bigger core in order to reduce leakage inductance by accommodating a higher number of turns. Additionally, special care was taken in terminating the windings onto the circuit board.

Various primary and secondary side waveforms were studied to verify proper operation of the power converter. Figure 9 below shows the transformer secondary voltage across the main (30 VDC) output winding along with the gate-to-source voltage of the primary side MOSFET. These waveforms clearly show the quick transfer of current between D14 and D15, complete demagnetization of the transformer core within a switching cycle, and peak voltage stress for D14 and D15.

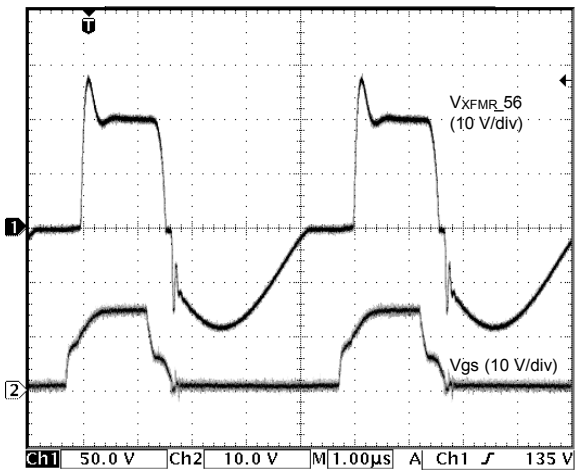


Figure 9 Transformer secondary (top) and MOSFET gate-to-source (bottom) voltages.

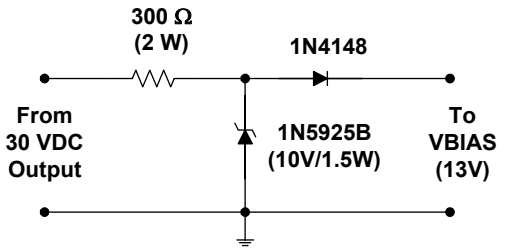


Figure 10 Second bias voltage implementation for no-load operation of the converter.

Next, the light load operation of the converter was investigated. The original design allowed the converter to regulate its output voltage at 30 V down to 0.25 A of load current with the converter entering discontinuous mode of operation below 1 A of load current. The converter shut down occurred below 0.25 A of load current. The bias voltage started to go down from the nominal value of 13 V as the load decreased below 0.5 A; and around the load current of 0.25 A the bias voltage was only about 8.0 V. Further decrease in load current caused the PWM IC (UC2845A) to turn-off due to its UVLO off limit of 7.9 V. This dependence of bias voltage on load is due to increased effect of leakage inductance under light load conditions, resulting in poor effective coupling between the bias and main output windings of the transformer. The way the converter was operated down to the no-load condition is by generating a second bias voltage of about 10 V off the 30 V output diode or-ed with the bias voltage of 13 V. Thus, the 10 V bias voltage will be used only when the 13 V bias voltage goes under 10 V during light load conditions; and it will maintain power to the PWM IC and keep the converter running down to the no-load condition. Figure 10 shows the implementation of the second bias voltage generation in order to achieve the converter operation down to no-load at the expense of an additional 2 W of power loss.

Upon inclusion of snubber circuits[2,5] to reduce switching noise, second bias circuit to implement no-load operation, and gate drive optimization, efficiency and voltage regulation data were recorded under steady state operation from no-load (0 W) to full load (360 W). Figure 11 shows efficiency of the converter with an input voltage of 24 V as a function of load, indicating a maximum efficiency of 86.5% at half-load (180 W) and a full-load efficiency of 83.5%. The static output voltage regulation data for the same conditions is shown in Figure 12, representing a full-load regulation of 0.37%. Output voltage regulation against input voltage variation under full-load operation is shown in Figure 13. The recorded data show only a 0.1% change in output voltage as the input voltage varies from 24 V to 34 V.

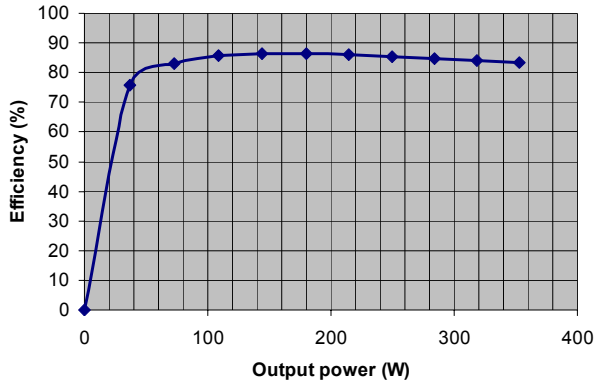


Figure 11 Efficiency of the converter.

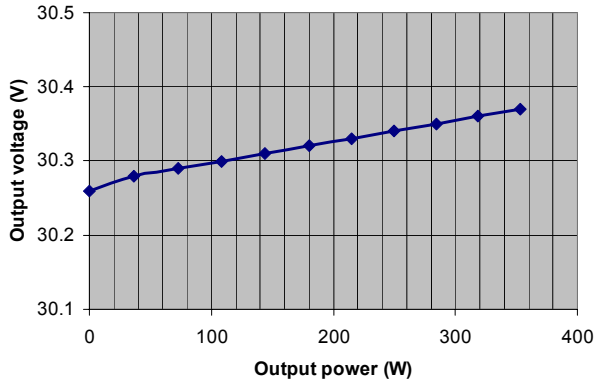


Figure 12 Output voltage regulation against load variation.

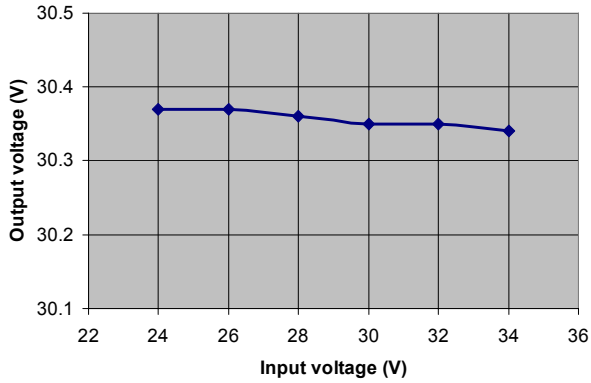


Figure 13 Output voltage regulation against input voltage variation.

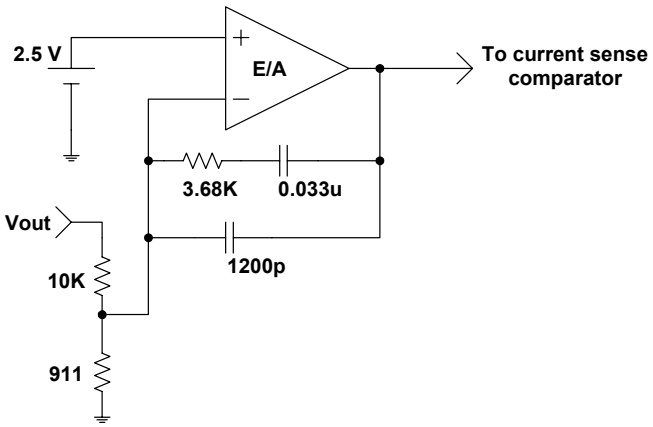


Figure 14 Modified controller configuration.

Feedback loop design

The analytical transfer function of a current-mode controlled forward converter[1,2] has a pole at a frequency determined by load resistance and output capacitor value, a zero at a frequency determined by ESR of the output capacitor and output capacitor value, and a sub-harmonic pole at half the switching frequency (100 kHz). Based on this information, during initial testing of the converter a simple first order compensator[9] (controller) in the form of an integrator was

implemented. This original compensator consisted of 0.136 μF (=2*0.068 μF) capacitor for C26. The following components were not used originally: R30, C29, R26, and C28. The implemented integrator was expected to provide a high dc gain, low crossover frequency, and a less-than-optimal phase margin. The gain and phase plots of the power stage, the compensator, and the loop were obtained with the original integrator compensator in the circuit and converter running under full load at a dc input of 24 V using a frequency response analyzer (Model 200 from AP Instruments[10]). The loop plot showed a crossover frequency of 1 kHz, a phase margin of 58°, and a gain margin of 50 dB; a good enough loop for steady state operation and testing.

In order to achieve a good audio-susceptibility and output impedance characteristics in support of a better transient response of the power converter, the crossover frequency needed to be improved while keeping a phase margin in excess of 50° and a gain margin in excess of 20 dB. Using the *Power 4-5-6*[11] power supply design software, a second order compensator[9] with an integrator, a pole and a zero was designed and implemented as shown in Figure 14. This compensator was designed using the measured power stage frequency response and analytical frequency response of the new compensator to achieve a loop crossover frequency of 5 kHz and a phase margin in excess of 60°. Upon implementation of the above compensator, frequency response of the new loop was measured and the recorded plots are shown in Figure 15. The new loop plot shows a crossover frequency of 5 kHz, a phase margin of about 75°, and a gain margin of about 23 dB; meeting or exceeding the set design values.

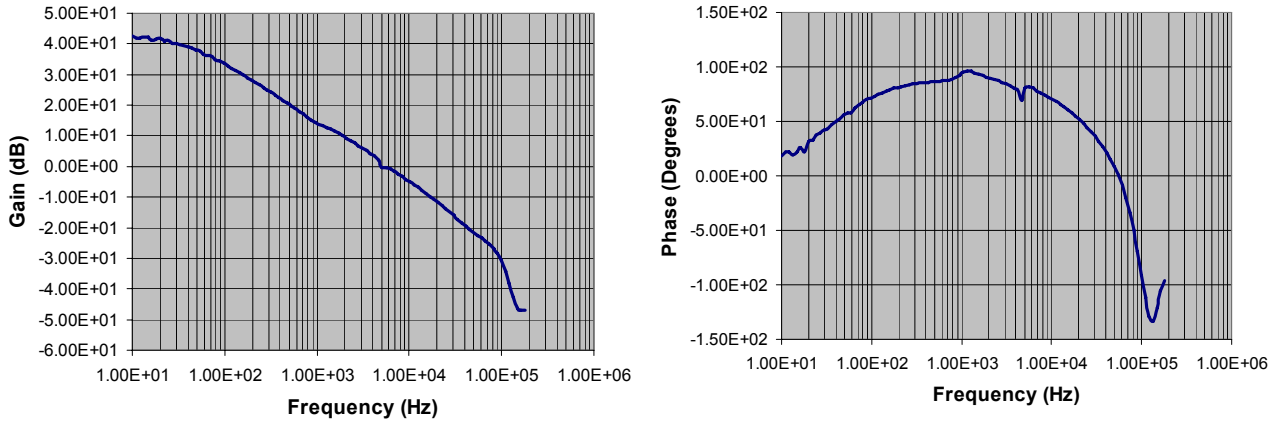


Figure 15 Measured gain and phase of the control (voltage and current feedback) loop.

Load transient performance

Once the loop design was optimized, it was time to test the converter under transient load conditions. Figure 16 shows the output voltage of the converter as the load is switched from 0 A to 12 A. As expected, output voltage dips and then recovers with practically no overshoot. The recovery time of about 200 μs is acceptable for this application; however, the voltage droop of about 6 V may not be acceptable. If the application requires a lesser droop in voltage, an improvement in converter's ability to handle step load change can be made.

First option is to increase the gain crossover frequency by designing a new compensator; this will help more with the recovery time and to a lesser extent the voltage droop. The second

option is to increase the output filter capacitance by adding a few more of 4.7 μF/50 V low-ESR tantalum capacitors. This will definitely help to reduce the amount of voltage droop, and is implementable since the power converter board can easily accommodate a few more of the surface mount tantalum capacitors. However, additional output capacitance would require modification to the present loop design to ensure proper gain crossover frequency, phase margin, and gain margin under the new power stage conditions.

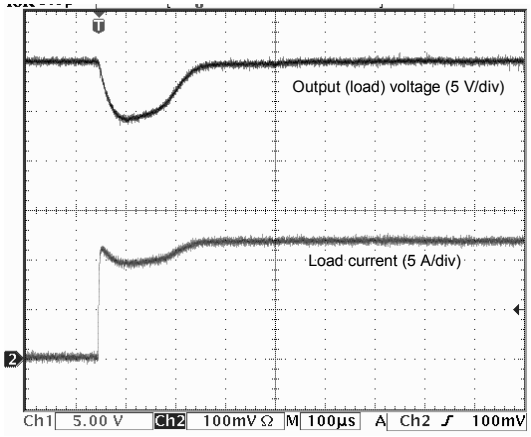


Figure 16 Converter output voltage for a step load change from 0 A to 12 A.

Summary

A switching power converter design project incorporating knowledge of power electronic circuit design, magnetics design, power semiconductor devices, feedback control theory, thermal design, schematic entry, circuit simulation, PCB layout for power applications, circuit card assembly using surface mount and through-hole components, and testing of circuit card assembly using modern instrumentation technologies is a great experience for EET graduates. This project was carried out by a senior level EET student as a credit-bearing semester-long independent research project. The overall experience was rated as excellent and marketable by the student.

References

1. N. Mohan, T. M. Undeland, and W. P. Robbins, "Power Electronics: Converters, Applications, and Design," (book), 3rd edition, John Wiley, 2002 (ISBN: 0-471-22693-9).
2. R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," (book), 2nd edition, Springer, 2001 (ISBN: 0-7923-7270-0).
3. "Soft Ferrite and Accessories," 2005 Data Handbook, Ferroxcube (http://www.ferroxcube.com/).
4. Litz Wire, New England Wire Technologies (http://www.newenglandwire.com/litz.asp).
5. M. Brown, "Practical Switching Power Supply Design," (book), Academic Press, 1990 (ISBN: 0-12-137030-5).
6. CS4/CS6 Capstick capacitors, ITW-Paktron (http://www.paktron.com/).
7. Multisim and Ultiboard, Electronics Workbench (http://www.electronicsworkbench.com/edu/eduprod.html).
8. PCBexpress (http://www.pcbexpress.com/).
9. G. Chryssis, "High-Frequency Switching Power Supplies: Theory and Design," (book), McGraw-Hill, 1989 (ISBN: 0-07-010951-6).
10. Frequency Response Analyzer, Model 200, AP Instruments (http://www.apinstruments.com/products.htm).
11. Power 4-5-6 Design Software, Ridley Engineering (http://www.ridleyengineering.com/software.htm).