

ADC Automated Testing Using LabView Software

Ben E. Franklin, Cajetan M. Akujuobi, Warsame Ali

Center of Excellence for Communication Systems Technology Research
(CECSTR)

Dept. of Electrical Engineering
Prairie View A&M University, Texas 77446

Abstract

The focus of this project is to implement automated test algorithms for testing analog-to-digital converters using LabView software. With the increase in bandwidth hungry applications the need for high speed and high resolution ADCs are needed on the front ends of the new systems that are being implemented today. As the designs become more complex, the ability to test these fast and high resolution ADCs becomes even more important. LabView allows the test engineer to interact with the device under test (DUT) through means of data acquisition and instrument control. Developing custom tests in LabView can result in reduced test time, which in turn will help reduce costs in testing. A linearity test will be presented for testing ADC static parameters in LabView, which include Differential Non-Linearity (DNL) and Integral Non-Linearity (INL).

1. Introduction

There are various methods of finding the code edges of an ADC such as binary search methods that are good for production testing of circuits that are essentially one-bit ADCs like comparators [1]. The use of binary search for ADCs with more resolution will result in at least 100 samples per iteration needed per code edge measurement, thus this will not benefit in the test time realm of production testing. The servo method is another method that utilizes a servo circuit that does the function of a step search, but is a fast hardware version. This method is good for production testing but it is not as fast as the histogram tests like the linear ramp and sinusoidal methods [1]. In ADC testing, a histogram shows how many times each output code appears in the response vector, regardless of the location [2], [3]. Linear ramp simplifies computation due to the proportionality of the step width to the number of hits of each code [2], [4]. The speed of the ramp cannot be too fast or the code will not be hit as many times as needed in order to get the most resolution and repeatability. The sinusoidal histogram method is the method of choice for this paper due to the relative ease of producing a pure sinusoidal waveform than a perfectly linear ramp for improved characterization of dynamic performance of the ADC

[1]. The typical input is a sinusoidal wave and it makes sense to test the ADC using the inputs that will be used in real world applications. We will explore the use of the sinusoidal histogram to essentially convert the many-to-one mapping of the ADC to one-to-one mapping for the calculation of Differential Nonlinearity (DNL) and Integral Nonlinearity (INL). We will present the results of the custom test developed in LabView to test the ADS5410 EVM (Evaluation Module) which utilizes a 12-bit 80MSPS ADC. In Section 2, we will discuss the test setup. The Sinusoidal Histogram, DNL, and INL calculations are discussed in Section 3 while the results, discussion and conclusion are in Section 4 and 5 respectively. The Reference is in Section 6.

2. Test setup

In order to begin testing the ADS EVM you must know what types of equipment will be used in order to get the types of results you are seeking. In conjunction with these instruments the tester needs to know how the instruments interface with each other and in what manner they are connected for testing the Device Under Test (DUT). Figure 1 displays the ADS5410 EVM setup with LabView [5], [6] as the software of interest.

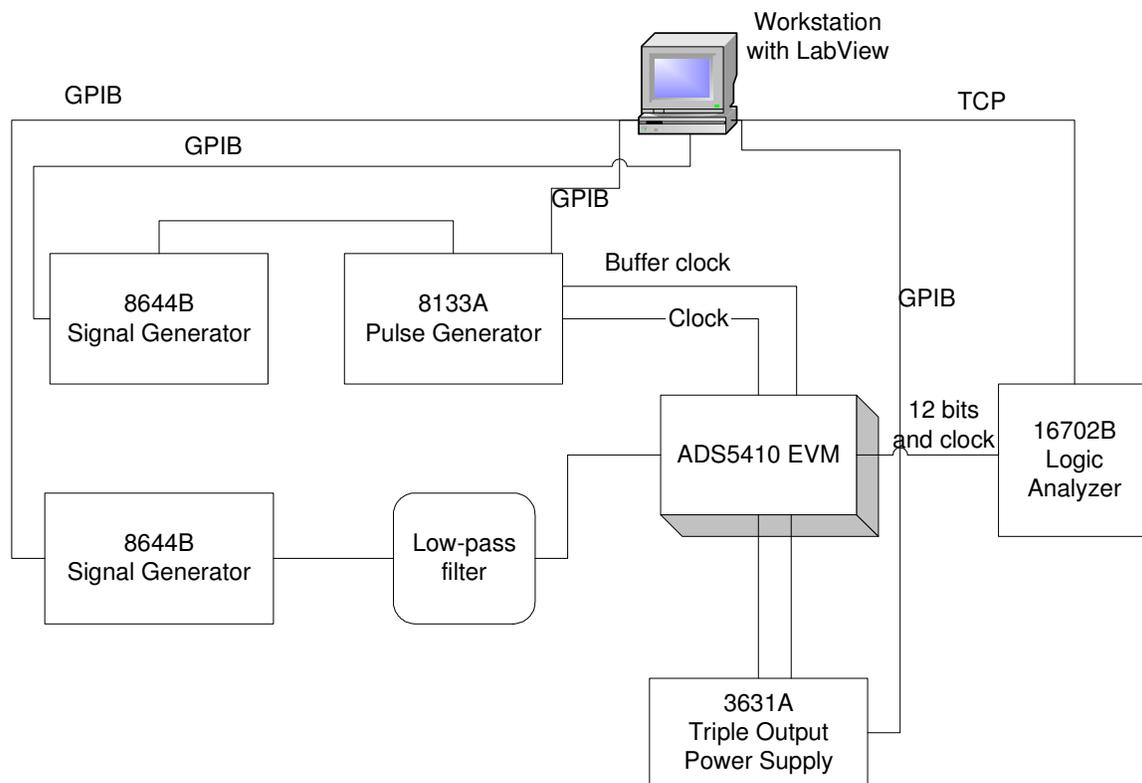


Figure 1: ADS5410 EVM test setup with LabView software.

The signal generator connected to the pulse generator is for a reference to the external input of the pulse generator. This signal generator is converted into a square wave for the ADS5410 clock and the buffer clock to represent the sampling frequency for the DUT. The sampling frequency should be at **least** three or four times the nyquist frequency for

adequate sampling [1]. The sampling frequency used in testing the ADS5410 is 80 MHz, which is 16 times that of the 2MHz carrier frequency used in this test. The signal generator connected directly to the low pass filter to the DUT is the actual carrier sine wave that will be sampled. The low pass filter is used to prevent aliasing during sampling in order to receive an accurate representation of the carrier signal [1]. The 8133A pulse generator is the central clocking reference for the overall test because it takes in the sampling frequency and converts it into a square wave to be outputted to the ADS5410 EVM. The pulse generator provides the ADC clock as well as the buffer clock to the board that connects to the logic analyzer. The offset and amplitude of the pulse generator is crucial in making sure that the clock circuit on the board is driven so that the logic analyzer can receive the signal for sampling, because a small offset voltage will not enable the clock output on the board. The 3631A triple output power supply provides a 3.3V supply to the analog input of the ADS5410 EVM and a 1.8V supply for the digital input of the board to drive the digital circuits. The 16702B Logic Analyzer captures the digital data output of the ADS5410 for analysis. From the workstation containing LabView all the necessary instruments can be controlled remotely for quick setup of parameters needed. All of these instruments use a GPIB connection for serial communication with the workstation, except for the logic analyzer, which uses a TCP/IP connection for data transfer and communication.

3. Sinusoidal Histogram, DNL, INL Calculations

This method is utilized by applying a sinusoidal waveform that is a little larger than the FSR of the ADC to ensure that all steps are hit from edge to edge [2]. The number of hits at the upper and lower codes will be used to calculate the input signal's offset and amplitude [1]. The calculation of the upper and lower codes as well as the offset and amplitude calculation are Mahoney's equations for this characterization and are as follows:

$$\text{Offset} = \left(\frac{C_2 - C_1}{C_2 + C_1} \right) (2^{N-1} - 1)$$

$$\text{Amplitude} = \frac{2^{N-1} - 1 - \text{offset}}{C_1}$$

$$C_1 = \cos \left(P \frac{A(2^N - 1)}{N_s} \right)$$

$$C_2 = \left(P \frac{A(0)}{N_s} \right)$$

$A(2^N - 1)$ is the number of times the upper code is hit, and $A(0)$ is the number of times the lower code is hit. To find the ideal sine wave distribution of hits expected from perfect ADC excited by a sine wave we utilize the offset and amplitude of the input sine wave. The formula for ideal distribution sine wave is:

$$A_{\sin wave}(i) = \frac{N_s}{P} \left[\sin^{-1} \left(\frac{i + 1 - 2^{N-1} - offset}{peak} \right) - \sin^{-1} \left(\frac{i - 2^{N-1} - offset}{peak} \right) \right],$$

$$i = 1, 2, \dots, 2^N - 2$$

From the ideal sine wave calculation we can get our code widths to enable us to obtain the DNL values for the ADC. To get the code widths we utilize this formula:

$$\text{LSB code width}(i) = \frac{A(i)}{A_{\sin wave}(i)}, i = 1, 2, \dots, 2^N - 2$$

After obtaining the code widths the test engineer can just subtract one from each width to get the endpoint DNL, but remember that the upper and lower codes are undefined so there will be one less value than the usual $2^N - 1$ codes. To get the INL you must do a running sum of the DNL values with a constant of integration of zero. The LabView code for the sinusoidal histogram method is shown in Figure 2 to show the graphical nature of programming in LabView.

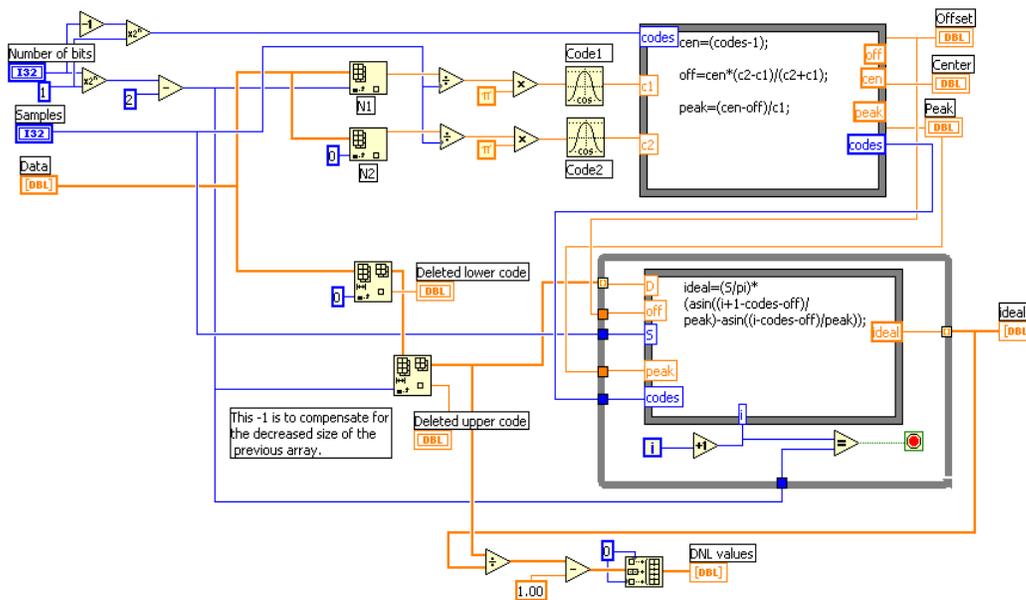


Figure 2: Sinusoidal histogram method with DNL calculation LabView code.

The INL calculation in LabView is displayed in Figure 2 in which the DNL values from the sinusoidal histogram are exercised.

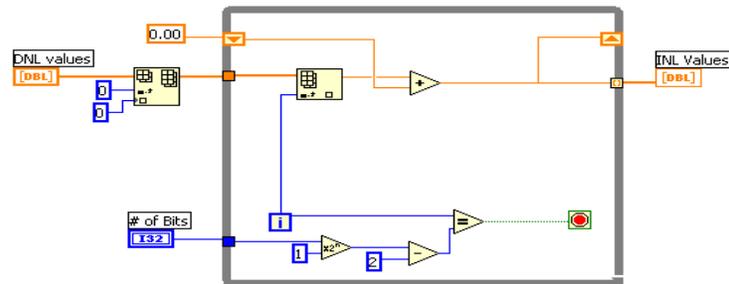


Figure 3: Running Sum calculation for INL in LabView.

The front panel user interface and LabView code of the Linearity test developed are displayed in Figures 3 and 4 to show the linkage between different calculations to act together as one total automated test.

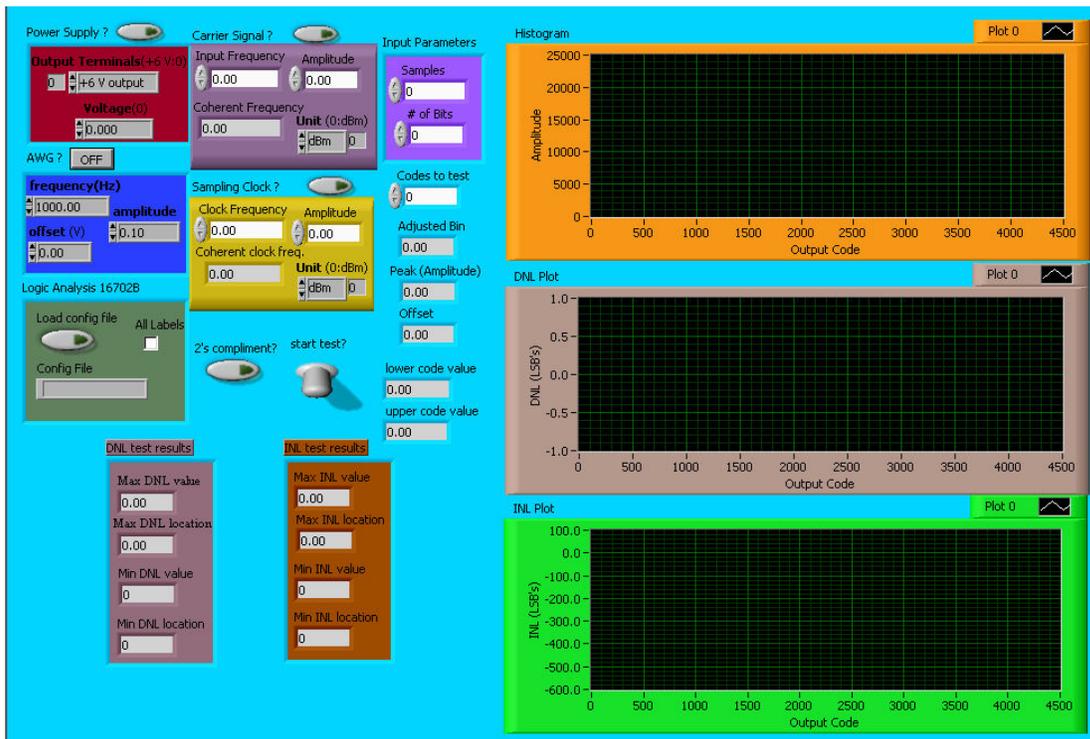


Figure 4: User interface of the Linearity test.

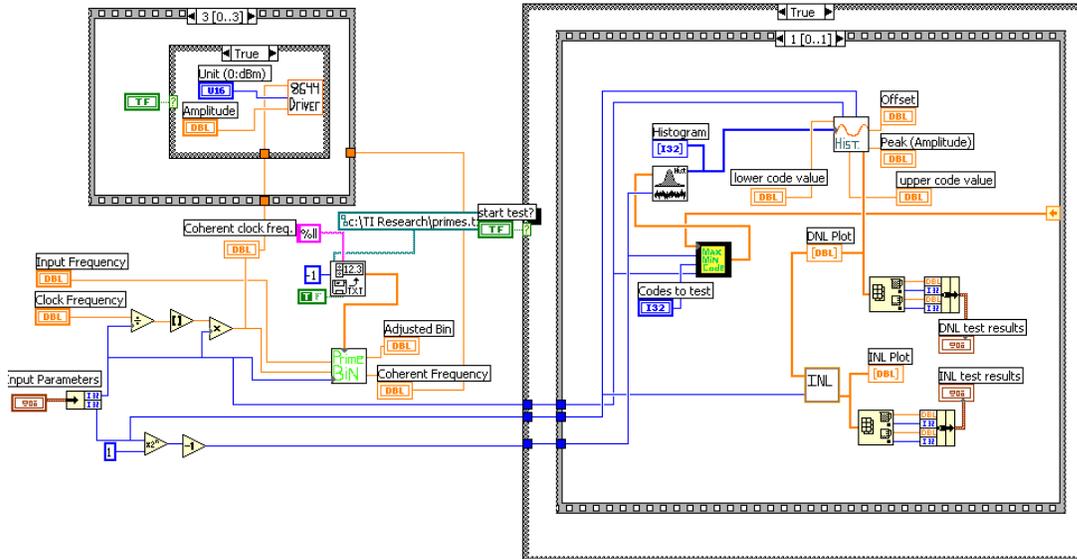


Figure 5: LabView code of the Linearity test developed.

4. Results

Figures 6, 7 and 8 are results of three runs of the Linearity test to get the dynamic characterization performance of the EVM with two different input frequencies and amplitudes. The frequency selection was based on the low pass filters that were available to us in the test lab. The filters have cutoff frequencies labeled on them, and to account for roll off of the filter, the input frequencies were set slightly below the cutoff frequency. For the 2MHz input frequency, the cutoff of the filter was 2.2MHz, and the 5MHz input frequency was obtained with a cutoff filter frequency of 5.5MHz.

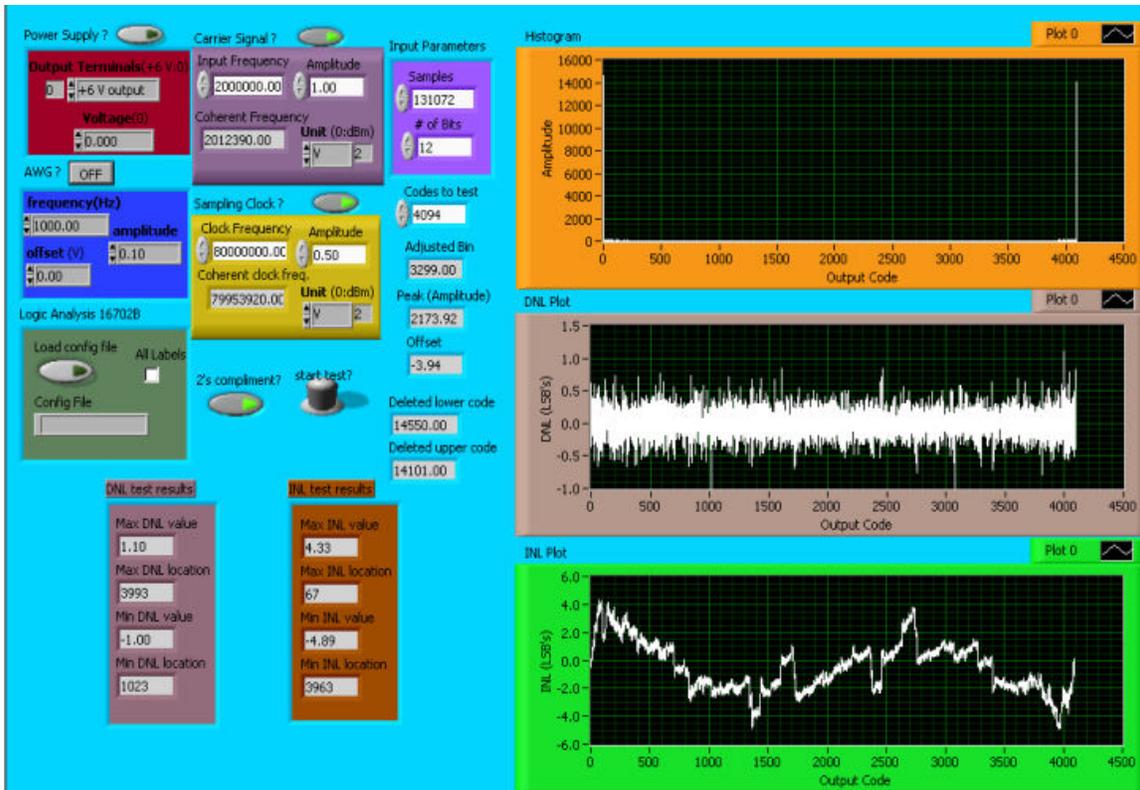


Figure 6: First run of test with a 2MHz input signal, 1V amplitude, and 32 times the sample size.

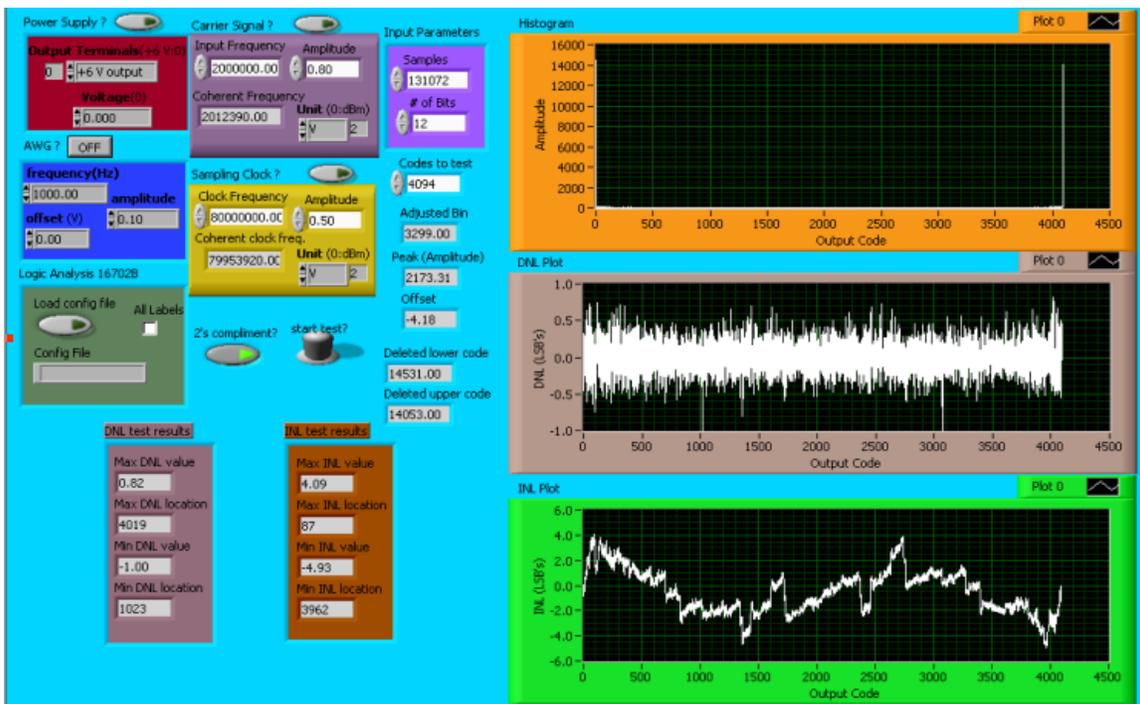


Figure 7: Second run of test with a 2MHz input signal, 800mv amplitude, and 32 times the sample size.

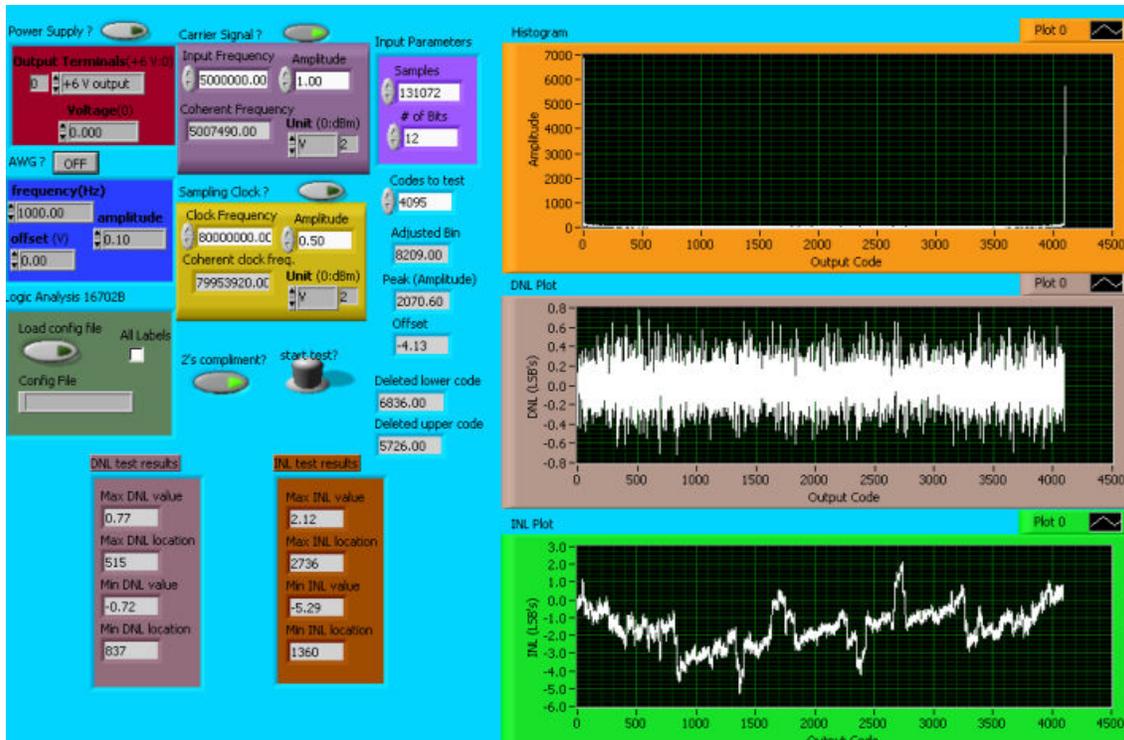


Figure 8: Third run of test with 5.2MHz input signal, 1V amplitude, and 32 times the sample size.

5. Discussion and Conclusion

The test results showed good DNL values and present correlation with the data sheet of the ADC. The INL results were on average 2 LSBs off the data sheet specifications. These INL values are due to the fact that there are a number of DNL values that are either negative or positive consecutively. Averaging the DNL can also help somewhat in the plot, but not too drastically. We will explore increasing the sample size and input amplitude to see if there is any change in results.

6. References

- [1] Burns and Roberts, "Introduction to Mixed-Signal Test IC Test and Measurement," Texas Instruments, Inc. McGill University, Texas A&M University and The University of Arkansas.
- [2] Matthew Mahoney, "DSP-Based Testing of Analog and Mixed-Signal Circuits," *IEEE Computer Society Press-1987*, Los Alamitos, California, pp. 135-152.
- [3] S. Bernard, F. Azaïs, Y. Bertrand and M. Renovell, "Linear Histogram Test of ADCs – A BIST Implementation," LIRMM - University of Montpellier 161, rue Ada, 34392 Montpellier, France.
- [4] Sasikumar Cherubal, Abhijit Chatterjee, "Optimal Linearity Testing of Analog- to-Digital Converters Using a Linear Model," *IEEE Transactions On Circuits And Systems—I: Fundamental Theory And Applications*, Vol. 50, No. 3, March 2003.
- [5] Robert H. Bishop, "Learning with LabView," University at Texas at Austin, 1999 Addison- Wesley Longman, Inc.
- [6] Mahesh L. Chugani, Abhay R. Samant, Michael Cerna, "LabView Signal Processing," National Instruments 1998 Prentice Hall PTR, Prentice-Hall Inc.

BEN E. FRANKLIN

Ben Franklin is a graduate student of Electrical Engineering at Prairie View A&M University. He is working as a Research Assistant at the Center of Excellence for Communication Systems Technology Research (CECSTR) in the area of Mixed Signals since 2003. He completed his BS from Prairie View A&M University. His research interests are in the field of Mixed Signal testing and Signal Processing.

CAJETAN M. AKUJUOBI

Dr. Akujuobi is the founding Director of the Broadband Access Technologies Program and Laboratory at Prairie View A&M University. He is also the founding Director of the Center of Excellence for Communication Systems Technology Research (CECSTR). One area of his research interests is in Mixed Signal Systems Design and Testing. He is also the founding Director of the Mixed Signal Systems Research Program at Prairie View A&M University.

WARSAME ALI

Warsame Ali is one of the researchers working at the Center of Excellence for Communication Systems Technology Research (CECSTR). He is a member of the Electrical Engineering faculty. His research interests are in Mixed Signal Systems and Control Systems.