Adopting the Cādence® Design System for an Engineering Technology Program

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Abstract

The University of New Hampshire (UNH) Manchester campus offers a four year program in Electrical Engineering Technology (EET). This work describes a multi-year collaboration between the UNH-EET program and an industry partner to develop a digital and analog curriculum to address the staffing needs of the regional microelectronics industry. The UNH-EET program consist of a three course sequence in digital and a two course sequence in analog. The introduction course topics are consistent with traditional analog and digital EET curriculum with the advanced courses now covering integrated microelectronics concepts. The advanced digital course covers Metal Oxide Semiconductor (MOS) transistor theory, Complimentary MOS (CMOS) processing, transistor level gate delay analysis, power estimates, interconnects impact assessment, reliability design considerations, CMOS scaling calculations, and system simulation approaches. The advanced analog course includes transistor amplifiers theory, design of transistor level differential amplifiers, multistage amplifiers applications, implementation of bias circuitry, and output stage architecture. Through a partnership and financial support of a major international semiconductor company the industry standard Electronic Design Automation (EDA) Cādence® Design system has been adopted for the associated laboratory exercises on schematic capture, simulation and physical design for both the digital and analog curriculum. Over a four year period enrollments in the course sequence have increased and steady placement of students in the microelectronic industry in the region has been demonstrated. This curriculum approach makes the UNH-EET program one of only 250 American academic institutions to provide access to the Cadence Systems through the Cādence® University Program.

Introduction

The traditional method for delivering Electrical Engineering Technology curriculum is to start with several courses in digital and analog electronics along with the appropriate Alternating and Direct Current (AC/DC) circuit analysis classes. For the digital class the introduction material is covered in the first class such as basic logic gates, number systems, Boolean algebra, Karnaugh mapping, flip-flops, latches, counters and programmable logic devices. A second semester digital course would cover the internal structure of logic families, complex digital circuits, synchronous logic, A/D and D/A conversion, timing diagrams, computer bus systems, programmable logic devices (PLD), and complex circuit debugging, digital interfacing various logic families to each other as well as digital Input Output (I/O) structures.

The analog electronics curriculum usually starts off with the basic physical behavior of electronic devices. Emphasis in this introduction course can be on analysis and application of

electronic circuits utilizing semiconductor diodes, operational amplifiers, and transistors. Once the basic device applications are understood topics such as rectification, clipping circuits, clamping circuits, regulated power supplies, basic op-amps, biasing of transistors, and simplified AC modeling of transistor circuits is covered. The second course off Analog design covers more advanced topics with and broader system level applications. The non-ideal characteristics of op-amps and other electronic devices is typically included emphasizing offset, gain and linearity. Other topics may include but are not limited to: sensors, pulse width modulations, Bode plots, Silicon Controlled Rectifiers (SCR), Triode for Alternating Current (TRIAC) and some basic optoelectronic devices. Engineering Design Automation (EDA) tools can be used to reinforce the theory through analysis and simulations. The two most common eductational EDA tools are National Instruments Multisim and Linear Technology LTSpice.

Both the Analog and Digital curriculum will be the basis to understand the system level approach of specifying, breakdown, hardware/software development, and integration of an embedded systems course. In such a course students typically explore microprocessor architecture, instruction sets, interfacing, and real-time programming techniques in assembly language. Laboratory exercises usually consist of system level development in serial and parallel data transfer, data acquisition, and analog input and output signal processing. The most common chips used in microprocessor courses are the Motorola HC11/12 or the Intel 8051.
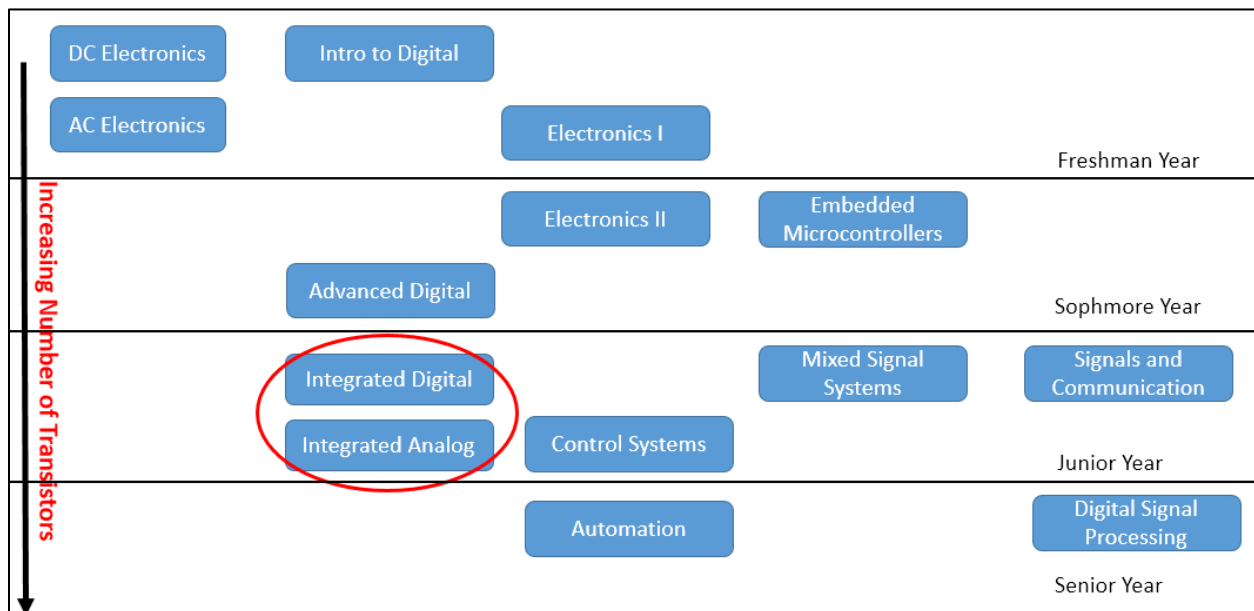

Figure 1

Figure 1 shows how a four year EET curriculum would map out introducing the integrated Analog and Digital curriculum. Also include in the figure is the year, semester/term on the left hand side with the relative number of transistors the student will be working with. The diagram maps out the curriculum flow and stacks the prerequisites as the material covered builds of previous classes. The two courses that are circled in red are the integrated digital and analog courses under discussion.

Microelectronics Industry in New England

The east coast and New England in particular played a pivotal role in the history of the integrated circuits industries. It is commonly known that the first transistor was invented at Bell Laboratories in 1945 in New Jersey[1]. What is lesser known is the presence of several important semiconductor manufactures that invested billions of dollars in silicon fabrication facilities across New York and New England. Two of the largest facilities were built by International Business Machines (IBM) in Fishkill New York and Essex Junction Vermont. At the height of the microprocessor and memory wars in the late 1990's and early 2000's IBM employed tens of thousands of people in the microelectronics industry. Digital Equipment (DEC) had a large semiconductor processing facility in Hudson Massachusetts. Fairchild semiconductor had a facility in Portland Maine. IBM famously left the microelectronics industry in 2015 by giving both its manufacturing plants in New York and Vermont to Global Foundries[2]. DEC closed in 1998 and the fabrication facility was sold to Hewlett Packard which was eventually acquired by Compaq then to Intel. Fairchild was acquired by ON semiconductors in 2017.

It would seem having major players like IBM, DEC and Fairchild leave the industry would mean less demand for engineering technology graduates with integrated circuit design skills; such as testing and analysis however the exact opposite is currently the case in New England.

Fewer and fewer companies can support owning and operating a fabrication facility so in the absence of a manufacturing infrastructure many companies opted to a fabless model. These kind of companies focus on the design of integrated circuits using sophisticated EDA tools. With a large population of highly skilled engineers looking to stay in New England many new companies were started or branch offices of established companies opened up. Beyond the bigger companies like Global Foundries and Compaq smaller companies like Texas Instruments, Linear Technologies, Allegro Microelectronics, Analog Device International, Melixus Semiconductors, and Skyworks opened integrated circuit design shops in Southern New Hampshire, Maine and Massachusetts regions. In Vermont the integrated circuit talent that left IBM started smaller boutique design shops including AsicNorth, GreenMountain Memories, Nanya, and Mobile Semiconductors.

The current situation is the integrated circuit design, analysis and testing talent is aging and many students and colleges have steered away from integrated circuit curriculum. As the internet boom took hold there was a common perception that transistor level design would go away. The use of Field Programmable Gate Arrays (FPGA) and Programmable Logic Devices (PLD) along with the use of high level synthesis languages such as VHDL would render circuit level design skills worthless. Nothing could be further from the current reality. With all of these smaller design shops opening up there is a strong need for students who understand how a transistor is built, how to use EDA tools to do transistor level design and simulation in both the Analog and Digital domain. ET students are particularly well suited to take these jobs as a lot of the work is in physical design, verification and simulation.

The Curriculum

The key topics for the curriculum are shown in Table 1 and is separated out into two columns one for the Digital and one for the Analog. The textbook for the digital class is "CMOS VLSI design a circuits and system approach" by Neil H. S. Weste[3]. The book used for the Analog class is "Microelectronic Circuits" by Sedra and Smith[4].

Integrated Digital	**Integrated Analog**
• MOS Theory	• Signals and amplifiers
• CMOS Logic	• Ideal amplifiers
• CMOS process Technology	• FET, BJT operation
• Delay, Transient Response	• Transistor Amplifiers
• Dynamic and Static Power	• Voltage Transfer Characteristics
• Circuit Simulation	• Small Signal Models
• DC Transfer Characteristics	• Basic Configurations
• Combinatorial Circuit Design	• Building Blocks of Integrated Analog Amplifiers
• Sequential Circuit Design	• Differential Pairs
• Latches and Flip Flops	• A complete FET Op-AMP
	• Output Stages
	• Frequency Response/Stability

Table 1

The Sedra and Smith book does cover both Digital and Analog microelectronic circuit design but the way the material is handled it was desirable to use the Weste book for the Digital design concepts. The Weste book does a much more in depth explanation of how transistors are made and has much more advanced topics in digital systems design. The Weste book also has material relevant to hierarchal and system level design. The Sedra and Smith book is widely adopted for teaching analog circuits design. Interestingly both these text books are used at top traditional Engineering programs and are not particularly targeting ET students.
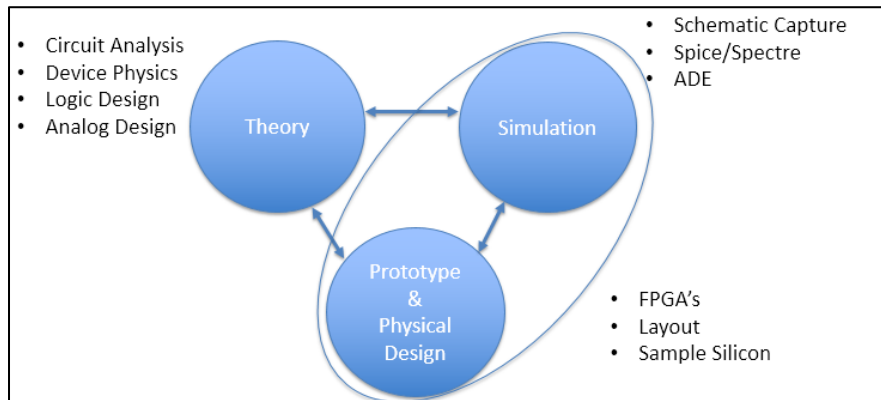
Figure 2

Throughout the course sequence three key areas of integrated circuit design are explored. First a sound understanding of theory, second using simulation as a tool for understanding, and finally the need to physically design or prototype a system. Theory is explored in lecture and through weekly homework assignments. Simulation, Prototype and Physical Design are explored during

weekly laboratory sessions. Figure 2 shows how these three areas interact with each other in the overall design ecosystem. In the laboratory Prototype and Simulation are jointly explored and are somewhat grouped together.

The Desired Educational Outcomes:
- Students will be familiar with the microelectronic industry
- Students will be familiar with microelectronic processing steps
- Students will be able to design logic circuit using CMOS gates
- Students will be able to design analog circuits using integrated MOS and BJT technology
- Students will be familiar with hierarchal design ranging from a few transistors to billions of transistors
- Students will be able to perform design and analysis with industry standard Electronic Design Automation EDA tools, in this sequence the **Cadence** design suite will be used for,
    - Schematic capture
    - Simulation
    - Physical design

Above is a list of the desired educational outcomes. The key outcome is to understand at a transistor level how to build analog and digital systems using CMOS and BJT technologies. The student also gains an in depth understanding the difference between doing discrete design compared to integrated design and the different approaches with EDA tools. In order to understand the complete process of designing integrated circuits the students need to understand how an integrated circuit is built. The intention is not to get bogged down with complex material science traditionally taught in VLSI courses, such as calculating oxide growth rates, or calculation diffusion profile depths but to understand the steps necessary to build a Field Effect Transistor (FET) so a student can do the physical design of a CMOS logic gate. It is also necessary to understand what Layout vs. Schematic (LVS), and Design Rule Checking (DRC) are for. Once the fundamentals are covered the concepts of modeling power, delay, circuit density and hierarchy are investigated. By the end of the two course sequence students are familiar with what EDA tools are used for, have some basic skills in using them, and to understand how a single transistor or logic gate is built and how billions of perfectly functioning transistors could be placed on a single chip.

The Cādence® University Program

To support the curriculum and to provide the hands on laboratory experience an appropriate EDA tool needed to be selected. As mentioned before NI-Multisim has been widely adopted in ET curriculum as it is intuitive to use, free to students and it can readily be downloaded to Window based systems. It is very common for ET programs using Multisim to have the students download the software to their laptops to do the necessary laboratory exercises on their own time in many cases at home. The drawback to using Multisim is it is very limited on transistor level simulation and there is no capability to do physical design (Layout) of the transistors. Student

versions also are limited in the number of devices that can be placed on a schematic. The device library has many more discrete devices such as 2Nxx bipolar transistors and 74xx series logic.

The two most common design systems that can handle transistor level design of integrated circuits are Cādence® and Synopsys. Both companies provide a suite of EDA solutions that can do full verification of silicon based integrated circuit designs. The features included simulation, schematic capture, physical design, layout vs. schematic (LVS), design rule checking (DRC), reliability evaluation, printed circuit design (PBC), chip level verification, logic synthesis, timing verification and many more. Cādence® has more market share than Synopsys with the larger companies like IBM, Global Foundries, Texas Instruments and Allegro are Cādence® design shops. Due to its presence in the larger employers Cādence® was chosen as the design system to be adopted. Another key factor in choosing one EDA tool over the other was the Cādence® University program[5]. This program offers the licenses to use the full suite of tools at a very reasonable price compared to the commercial price which can be many hundreds of thousands of dollars depending on the number of seats and features needed. The University program currently supports 250 institutions across the world including many tier one engineering research schools.

The first hurdle in using Cādence® in an ET laboratory is that the integrated circuit tools ONLY run on Linux based machines. This can be a road block for both faculty and students as Linux is not widely used in ET curriculum. When the students take this sequence of classes they typically are juniors and in most cases none of the students have ever used or seen a Linux line command prompt. The other common complaint is the students cannot download a version of the software onto their personal laptops and attempt to do the labs at home when it is convenient for them. In order for the software to be installed properly and consistently maintained the ET program contracted IT support from the main UNH IT department. The UNH IT support staff built a "virtual Linux server" on the university main computing system where the software was installed and the license handled. Students remotely logged onto the server by using Cygwin-x in windows opening up a Linux command prompt on the desktop. This logon approach would work if students had Cygwin-x on their personal laptops from home with two considerations; first they would need a secure VNC to get the appropriate license from the virtual server, and second the connection and ability to run the cadence software is very unreliable through a WiFi Cygwin-x connection.

The final consideration is the Cādence® system needs "Technology Files". These files have the BSIM/moratsp device models for SPICE like simulation (Spectre for Cadence), they have the files that describe the schematic symbols, the layer definitions for physical design, the design rules for physical design, and libraries of common devices. Cādence® supplies a generic design environment with limited functionality. Another option is the Metal Oxide Silicon Implementation Service (MOSIS) from the University of Southern Californiat[6] information services that provides industry developed technology files for free to research and instructional Universities. The files from MOSIS can be used to build actual production level integrated circuit designs and fabrication facilities will build prototype chips that will be packaged and tested for functionality.

Laboratory Exercises and Objectives

Below is a list of the laboratory curriculum, each semester about six lab exercises are assigned. Each student will complete the work and submit a lab report that at minimum consists of a schematic, layout, and a simulation waveform. When students are doing physical layout they need to upload Layout vs. Schematic (LVS) and Design Rule Checking (DRC) run logs showing a schematic equivalency and clean design rules.

Digital

- Intro to Linux and the Cādence® Design system
- CMOS Inverter Voltage Transfer Curves P/N Ratio optimization
- Simple NAND gate schematic and simulation
- Simple NAND Gate Physical Design LVS/DRC
- RC Delay Line Modeling
- 4-Input NAND, Schematic, Simulation, Physical Design LVS/DRC

Analog

- Ideal Amplifier Models/Amplifier Hierarchy
- FET/BJT device curves finding r_o, gm, V_t, V_A ,and β
- Single Transistor Amplifier, Common Source
- The current Mirror
- Differential Pair, Common Mode and Differential Gain, CMRR
- Complete FET operational amplifier with output stage

When the laboratory classes start it was necessary to review the use of Linux. Cādence® still runs on a Lixus line command and today's students seem to be very unfamiliar with using line commands. The basic idea of directory structures, trees, launching executable files, copying files and listing directory contents are covered. Once students are familiar with navigating in a Linux environment the students start to work with the **i**ntegrated **c**ircuit **f**ront end to **b**ack end (icfb) utilities and **c**ommand **i**nterface **w**indow (ciw) to navigate the library management tool and to get familiar with the schematic capture window and the physical design window.

The First gate to be examined is the common logic inverter. This device is simply two FET's one NFET and one PFET. Students learn to create the schematic generate the physical design (Layout) and to run the LVS and DRC tools. Once the student creates a "clean" inverter they learn how to use the Analog Design Environment (ADE). This tool links the schematic capture tool to a simulation environment for Cādence® the tool is Spectre, similar to a SPICE simulator. It is necessary to setup the ADE to point to the correct morastp device models, define any variables, and choose an appropriate simulation. In this case students will do DC analysis and Transient analysis. The ADE tool will create netlists from the schematics and launch the simulation to complete on the Linux server. It is necessary to choose the appropriate output signals to generate graphical outputs of the appropriate signals. Of particular interest is the Voltage Transfer Curve (VTC) where for a DC only analysis the input is plotted as a function of the output. Students will learn how to adjust the P/N ratio of the FET's to optimize the gate for

the best balance of rise time and fail time. Additionally students will identify the unity gain points and determine the logic HIGH and logic LOW margins. Once these lab activities are done the students have a fairly solid understanding of basic CMOS gate design and the whole process of schematic capture, physical design and simulation. One of the interesting pieces of antidotal data that was observed it seemed students who had previous Computer Aided Design (CAD) experience with tools such as Solid Works or Fusion360 seemed to struggle with the physical design tasks. The students claimed the concept of grids and snapping and the hot keys to do basic functions are very different from typical mechanical CAD system implementation that it was confusing to them.

The next gate to be examined is the NAND structure. It is very common in introduction to logic classes for the instructors to make the point that logic designs typically use NAND structures over AND structures and usually NAND gates will not commonly exceed four inputs. De Morgan's law can be used to go back and forth between a NAND and AND implementation for a given logic structure. The main point of proceeding to the NAND gate is to demonstrate the reason why NAND gates are the most effective gates in a traditional CMOS implementation. Through simulation the students again "balance" the gate by adjusting the P/N ratios. Once the student is asked to do the layout the concept of sharing diffusion is introduced and the various ways of physically building NAND gates is looked at. At this point the concept of a symbol is introduced and the basic idea of hierarchy is discussed.

The important part of approaching circuit design from an integrated circuit perspective is to recognize that the physical structures that are being designed are not "ideal". To a first order this means appreciating that interconnects and wire routing are not perfect conductors. This idea is talked about in introduction to Digital Design classes but not really emphasized or explored in a meaningful way in the laboratory exercises. To address this students are introduced to the concept of wire models including the lumped, pi, and T models. Each model type is simulated and evaluated to determine the most appropriate model to be used in integrated systems. It would be very interesting to use extraction tools to generate full parasitic models of the gates but by this point in the semester students are overloading with new platforms and tools it was decided to not use extraction methodologies.

Finally the idea of hierarchy in design is explored. This laboratory exercise designs a four input NAND gate using a NAND-INVERT-NOR structure. It is left up to the student to design and balance a two input NOR gate. By this point in the semester the instructions for the labs are intentionally getting less descriptive and students are required to use the concepts and methods outlined in prior laboratory exercises to complete the task. Once the student has the three components of the NAND-NOR-INVERT it is necessary to place them all in a physical design. At this point it is necessary to use multiple level of the metal stack to connect all the gates. This final exercise typically takes much more than the allotted two and a half laboratory sessions and they are given two week to complete the assignment.

In the second semester during the Analog course there is a different viewpoint and approach to the laboratory exercises. The analog material is more simulation based and the physical design of analog structures is held off until the end of the semester. The idea behind the Analog laboratory

assignments is to understand the building blocks of an Analog circuit, in this case a simple differential operational amplifier. First the student will use the dependent sources to create a generic amplifier, an operational amplifier is simply a voltage controlled voltage source. Schematically the generic amplifier will be a source resistor in series with the input resistance, the voltage created across the input resistance will be the control voltage for the voltage controlled voltage source (VCVS) finally an output resistance is put in series with the VCVS. This netlist give the basic structure of an OP-Amp the gain on the VCVS can be set high such as 125,000 which is similar to the open loop gain of a 741 OP-Amp. At this point the netlist is simulated and hopefully the student will appreciate the difference between open loop gain and closed loop gain. This circuit can be configured as an inverting or non-inverting amplifier (Note: an output saturation condition is note modeled). Additionally open loop comparator circuits can be implemented.

The next laboratory exercise looks at the transistor. Most introduction to electronics courses do look at FET and BJT devices. Students learn what the transfer characteristics of these devices are and will do some load line analysis. It seems most ET programs still disproportionately study BJT's even though most modern electronics are mostly designed with FET's. Even with looking at BJT's in depth and solving many examples using the square law relationship it seems students do not take away the most basic functions of FET's and BJT's; simply put they can be used as switches and amplifiers. With that understanding it is then necessary to look at the characteristics of these devices that make them good switches or amplifiers. This will inform designers why you would choose BJT over a FET and also help better understanding of the different approaches of doing integrated design as opposed to discrete design.

The students generate the transfer curves of both the FET and BJT. This is done by biasing a basic common emitter (BJT) and common source (FET) amplifier and running a DC sweep on the control variable, additionally parametric analysis is done on a step variable. For the BJT the sweep variable is the voltage from Collector to Emitter (VCE) and the step variable is the voltage from Base to Emitter (VBE) plotting Collector current IC. For the FET the sweep variable is the voltage from Drain to Source (VCS) and the step variable is the voltage from Gate to Source (VGS) plotting the drain current (IDS). From these curves several key characteristics can be interpreted. For both the early voltage can be extrapolated (VA) and the output resistance (ro). Another important parameter to understand transistor amplifiers is transconductance (gm). It is interesting to compare the influence of the step parameters between the BJT and FET, for BJT's the current is very sensitive to VBE as it is an exponential dependency, for the FET the effect of VGS is less profound. Additionally it is interesting to look at the transition regions going from the linear region to the active region, for the BJT the emitter must be forward biased and VCE must exceed a defined saturation voltage, for the FET VGS must be higher than a threshold voltage and VD must be larger than VDS-Vt.

Once the student is familiar with the transistor characteristics they start to work with the basic building blocks of analog circuits. The next laboratory exercise is looking at a single transistor amplifier in the common source and common emitter configurations respectively. This will result in both a DC and AC analysis that plotting the VTC curves and transient analysis. The next block

studied is the current mirror, several configurations of current mirrors are simulated looking at passive-resistive and active-transistor loads. Current mirrors are a major building block for any analog circuit and looking at the various implementations help understand the benefits in area and power consumption for the various configurations. The next laboratory exercises look at the differential pairs as amplifiers. In class the use of differential pairs is explored discussing the benefits over single ended amplification. This leads to a discussion of differential gain, frequency response, transistor mismatch, Common-Mode-Rejection-Ratio (CMRR) and Power-Supply-Rejection-Ratio and also the use of active of passive loads. Finally the discussion of output stages is presented. For the final lab the students will assemble an active load current mirror that supplies a tail device into an active loaded differential pair feeding a Class-B output stage a complete differential Operational Amplifier. The students will simulate the gain and frequency response of their Op-Amp along with setting up test benches for measuring CMRR and PSMRR.

Conclusion/What Will Be Next?

A fairly obvious criticism of this approach is how relevant will the study of integrated circuit design for ET students particularly CMOS be in the near future. Generally it is worth asking; "as Moore's law draws to its end would teaching transistor level circuit design in any style still be a relevant skill?" Looking objectively at most current ET curriculum it is still disproportionally weighted to discrete bipolar transistors, 74xx series TTL logic gates and operational amplifiers (Usually the 741 Op-Amp running on +/- 15V power supplies). Teaching Analog and Digital design with discrete component opens the options to build and simulate a broader family of circuits. Another valid question is how relevant is the 741 Op-Amp and 74xx series TTL logic. With the integrated circuit design approach the student gain a much more in depth appreciation for real world circuit design as a craft opposed to a process of tinkering with chip sets that they will never see when they are working in the field.

To make a stronger case; it is difficult, if not a complete waste of time, because of miss match, to build complex analog circuits with discrete components, such as a current source feeding a differential pair with an output stage. As most analog functions are now realized with standard product integrated circuits developed by companies like Texas Instruments and Analog Devices International. Today it is extremely rare that a practicing engineering would build any system with 74xx series logic gates or 741 OpAmps operating off of +/- 15 and 5 volt supplies. It would be very interesting to know how many 74xx logic and 741 Op-Amps are consumed by instructional institutions versus those used in commercial products. By teaching the curriculum using EDA tools much more complex systems with higher tolerances and accuracy can be achieved.

Once it is accepted that this curriculum approach is beneficial to ET students it is important to look at what will happen when Moore's law ends. It is commonly understood that something will need to replace CMOS and it is not entirely clear what that will be. From 1971 to 2014 the International Technology Roadmap for Semiconductors (ITRS)[7] had documented and projected a clear progression for the semiconductor industry. In 2015 the IEEE took over and now the trends

can be followed by referring to the International Roadmap for Devices and Systems (IRDS)[8]. It is clear that with the new devices being proposed such as, Silicon on Insulator (SOI), fully Depleted SOI, FinFet's, Lateral Gate-All-Around-Device (LGAA), Vertical Gate-All-Around-Device (VGAA), 2.5 and 3D Packaging, that IRDS is projecting scaling to 2030. Even with scaling older technologies are still the backbone of many cutting edge designs.

In summary; this work described the UNH Manchester EET program approach to including the concepts of integrated circuit technology into the existing EET curriculum. The Cādence® design system was used in a series of laboratory exercises to complement the curriculum. This approach has been used over a three year period and many of the students have found work in local companies of which there primary business is integrated circuit design. In order to offset the cost of the Cādence® UNHM entered the University program and partnered with a local international semiconductor company. The company wrote a three year grant to cover the cost of the software and course fees were added to maintain the license costs moving forward. The sponsor company and several other companies serve on the UNHM-ET Industrial Advisory Board and do help inform curriculum development.

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