An Electrical Engineering Graduate Course Sequence in Integrated Circuits Targeted to Real-World Problems in Industry, Defense, and Security

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Abstract

This paper describes a three-year study to introduce nine learner-centered instructional techniques into a two-course electrical engineering graduate course sequence in integrated circuits (ICs) targeted to real-world problems in industry, defense, and security. The study measures the student learning in this two-course sequence with the use of a pre-test/post-test teaching methodology and is carried out through a collaboration of Air Force Research Laboratory Sensors Directorate and Air Force Institute of Technology (AFIT), a government institution. The participants in the study were Air Force officers at AFIT.

Results presented in this paper demonstrate the effectiveness of a pre-test/post-test teaching methodology even when data is restricted to samples of small size. Results show that a statistically significant improvement was observed in the first course of the two-course sequence when the Diagnostic and Post-Diagnostic evaluation results were compared. Analysis of the final exam results for one course for Year 2 and Year 3 shows that there is statistically significant improvement in performance. This change is attributed to the improved teaching methodology presented in this paper.

The views expressed in this document are those of the authors and do not reflect the official policy or position of the United States Air Force, Department of Defense, or the U.S. Government.
Introduction

For the United States to maintain a globally competitive advantage in an increasingly advanced technology-based society, science and engineering curricula must produce technically competent leaders, researchers, scientists, and engineers, as discussed in Rising Above the Gathering Storm\(^1\) and Research Universities and the Future of America\(^2\). No field is more important in this regard than semiconductor design and fabrication of integrated circuits (ICs). The very-large scale integrated circuits (VLSI) revolution was launched with the publication of the seminal textbook by Mead and Conway\(^3\) as discussed in the special issue of the IEEE Solid-State Circuits Magazine on Lynn Conway,\(^4\) and the subsequent foundation of MOSIS Integrated Circuit Fabrication Service.\(^5\) A state-of-the-art course sequence in ICs that produces technically-competent circuit designers must include exposure to real-world design experience with industry-standard software and laboratories, and instruction that equips students to address future needs for reduced device size, weight, and power as well as the capacity to design increasingly complex integrated circuitry and modern computing systems of interest to the computing industry, aerospace, and defense, as discussed in Report on Technology Horizons, Layered Sensing, DOD STEM Education & Outreach Strategic Plan, A National Action Plan, Constable and Somerville, and Examination of the U.S. Air Force’s Science, Technology, Engineering, and Mathematics Workforce Needs.\(^6\)\(^ -\)\(^11\) Such a course sequence must cover the topics of complex multi-core microprocessors identified as a key technology by Moore and Simon,\(^12\) chip size and performance tradeoffs, and fundamental logic blocks in a manner accessible to students.

As a result, a need exists for students to become aware of the importance of integrated circuit designs for industry, defense, and security applications using semiconductor technologies that are optimized for commercial applications, as discussed in the document Defense Science Board Task Force\(^13\) and Maynard,\(^14\) and semiconductor technologies and circuits targeted specifically for DOD applications including radiation-hard chips, as discussed in Maynard\(^14,15\) and Beckhusen.\(^16\)

This three-year study examines the impact of the introduction of nine learner-centered teaching techniques on students’ knowledge of VLSI concepts in a two-course graduate course sequence in VLSI circuit design. The study also examines students’ attitudes toward their experience with the new course sequence. The participants in the study were officers at Air Force Institute of Technology (AFIT), Wright-Patterson Air Force Base (WPAFB), Ohio. The research methodology involved pre- and post-tests of knowledge and end-of-quarter student surveys administered on-line by the Office of Institutional Assessment. The rest of this paper describes the new approach and how it was evaluated; presents and interprets results, and summarizes and discusses the findings.

DOD Government Institution of Higher Education

Air Force Institute of Technology (AFIT) is a DOD government institution and engineering graduate school with 900 graduate students. The institution mission is to advance air, space, and cyberspace power for the Nation, its partners, and the U.S. armed forces by providing relevant
defense-focused technical graduate and continuing education, research, and consultation. In the Graduate School of Engineering and Management, there are approximately 130 faculty (50% civilian, 50% military). Over 200 students graduate each year with M.S. degrees.

DOD Government Research Laboratory

The Air Force Research Laboratory (AFRL) Sensors Directorate’s “mission is to ensure unequaled reconnaissance, surveillance, precision engagement, and electronic warfare capabilities for America’s Air and Space Forces by developing, demonstrating and transitioning advanced sensors and sensor technologies.” At AFRL RYDI, the Integrated Circuits & Microsystems Components Branch “conducts both in-house and contractual efforts focused on the development and validation of comprehensive design tools and integration techniques for RF and mixed signal devices and components,” as discussed at the branch website.

Need for a New Course Sequence

If a course sequence is to deal with modern computing systems of interest to the computing industry, aerospace, and defense, it must cover complex multi-core microprocessors, chip size and performance tradeoffs, and fundamental logic blocks in a manner accessible to students. Rigorous instruction is especially needed to teach U.S. Air Force members, both military and civilian, to design, specify, and procure the highest possible VLSI capabilities. Industry-standard state-of-the-art Cadence Design Systems software has been selected by the instructor because it is used widely by professional engineers and scientists in industry, government contractors, and government laboratories including the Mixed Signal Design Center at the Air Force Research Laboratory Sensors Directorate. The Mixed Signal Design Center is co-located with AFIT. Figure 1 shows the structure of the U.S. Air Force capabilities and relationship to the VLSI course sequence for engineers.

![Figure 1. Key nature of the VLSI course sequence to the U.S. Air Force. Adapted from [6].](image)

In response to the growing need for a secure on-shore high-performance supply chain, the Air Force Research Laboratory Mixed Signal Design Center sponsored AFIT to participate in the
Trusted Access Program Office multi-project wafer silicon runs. The Trusted Access Program Office provided a path for the Department of Defense to “have guaranteed trusted microelectronics technologies” through IBM facilities, including design, packaging, fabrication, and characterization.

Course Structure and Teaching Techniques

The students in the VLSI course sequence are enrolled in the MSEE program, an 18-month experiential program with a required research thesis, in the Department of Electrical and Computer Engineering at AFIT. They are Air Force officers and completed their bachelors’ degrees in electrical, chemical, or aerospace engineering. The sequence provides an introduction to VLSI and digital circuit design, including the inverter, design tradeoffs, logical effort, power, high performance microprocessors, design for manufacturing, adder architectures, circuit tuning, and more complex combinational logic. In the course offerings that are the subject of this paper, emphasis was placed on teaching students to perform design tradeoffs, such as obtaining delay estimates for a timing-critical path, tuning the circuits to reduce the delay, recalculating the new delay of the timing-critical path, and quantifying changes in delay.

During the period of three years (denoted as Y1, Y2, and Y3) a two-course electrical engineering sequence in very large scale integration (VLSI) named EENG653 and EENG695 was taught to students at AFIT at Wright-Patterson AFB, Ohio. The EENG653 class was taught in years Y2 and Y3; and EENG695 class was taught in years Y1, Y2, and Y3. The teaching methodology was modified during these years in order to improve students’ learning. Statistical significance of changes in students’ learning was measured by comparing the evaluation data for each class during the three-year period.

Each course had a separate lecture and laboratory. Lectures were held two days per week for two hours each day. The laboratory was available 24-7 for the students, and most students took 6-8 hours per week to complete the weekly laboratory assignments. Tables 1 and 2 outline the course content, textbook readings, assignments, worksheets, laboratories, in-class mid-term exams, in-class final exams, a week-long midterm laboratory exam, and a week-long laboratory final exam.

Prior to enrolling in the first course, students are expected to have a working knowledge of algebra, calculus, solid-state physics, Boolean algebra, and binary arithmetic. At the beginning of each course, students were given a pre-test with a combination of questions on the prerequisite knowledge and material to be covered in the course. Post-tests given at the end of each course consisted multiple-choice questions on key course concepts. Some questions on the post-tests paralleled questions on the pre-tests, and some were qualitative questions designed to test conceptual understanding. Class attendance is required, and all students took the pre-tests, mid-term exams, post-tests, and final exams.
Instructional Approach and Four Categories of the Learner-Centered Teaching Techniques (A) through (D)

Three principles guided the design of the instructional approach used in the course sequence: (1) “Constructive Alignment,” wherein lessons, activities, assignments, and assessments all address the same learning objectives; (2) “Practice and Feedback,” a necessary condition for knowledge attainment and retention and skill development; and (3) “Balance,” wherein the instructor balances the needs of students with different learning styles, provides training in both basics and high-level skills, blends lecturing and active learning, and assigns individual and group work. 

Nine learner-centered teaching techniques based on those principles were implemented. The techniques fell into four categories: (A) Course setup, (B) Course delivery, (C) Formative assessment, and (D) summative assessment. The nine techniques 1) through 9) are now discussed in order in the categories (A) through (D).

(A) Course setup

1) Graphic organizer targeted to authentic VLSI applications in industry and aerospace

Graphic organizers are described in [56] by Felder and Brent who provide an example on page vi of [56]. Graphic organizers “preview material to be covered in class and/or summarize what was covered and put it in a broader context.”

In the case of this two-course sequence, the VLSI Graphic Organizer gave students the big picture of the circuit design process in the context of authentic industrial and aerospace problems. The use of a graphic organizer is expected to be helpful because approximately 80% of engineering students are visual learners [27, Table 1].

2) Learning objectives

For each homework assignment, laboratory exercise, and exam, students are provided with a table mapping each problem to the appropriate course learning objective(s). This table is a cover sheet that lists each learning objective in order in one column and a list of the problem(s) that map to each learning objective in the second column.

3) VLSI-CAD Manual

Students are provided with a tutorial-style, step-by-step 336-page laboratory manual with screen-shots of each graphical user interface (GUI) to learn the Cadence Design software at their own pace. Since prior knowledge of Cadence, Linux, object-oriented databases, cshell, and Secure Shell (SSH) is not assumed, each step is accompanied by written instructions and a screenshot of the associated step. This laboratory manual, with a complete listing of steps, is posted online at http://cmosedu.com/cmos1/cadence/cadence.htm.

Figure 2 shows examples of pages with detailed steps and images excerpted from the laboratory manual. Figure 2(a) shows an inverter chain with a check and save step; Fig. 2(b) shows a discussion of a hierarchical design methodology with hierarchical schematic; Fig. 2(c) provides a detailed review of steps to create an inverter chain; and Fig. 2(d) shows an example of how to use the calculator in Cadence.
Steps shown in the Lab Manual include the command windows, GUIs with input, and instructions to carry out specific VLSI design tasks. These tasks were adapted with generous permissions to use materials by faculty at Columbia University, University of Pennsylvania, Tufts University, and University of Virginia as shown on page 1 of [56]. These steps include (1-10) general information about Linux and how to set up a Linux account, FireFox, SSH, capture of images with The GIMP, printing and plotting, getting started with Cadence, and sending email from Linux. After carrying out these setup steps, the manual steps the student through the process of (11) creating a library, (12) a schematic, (13) a symbol, (14) Spectre simulation, (15) layout, (16) Design Rule Check (DRC), (17) extraction, (18) Layout versus Schematic check (LVS), (19) extracted-layout simulation, and (20) simulation with NC-Verilog. Subsequent steps are (21) generating I-V curves for an nFET, (22) parametric simulation of I-V curves for an nFET, (23) generating a voltage transfer curve (VTC) of an inverter, (24) creating an inverter chain, (25) ring oscillator, (26, 28) using the calculator in Cadence, (27) generating a parameterized inverter chain and measuring the delay of the parameterized inverter chain, and (29) performing a parametric analysis of the delay of an inverter chain.

Figure 2 (a)

Department of Electrical and Computer Engineering

Integrated Circuit Design CAD Tool Information

b. Open the 'ringoscillator_test’ cell schematic and wire the 11 inverters into a ring as shown in the image below. You will need to delete the load capacitor. Note that the output node of the 11th inverter is connected to the input node of the first inverter as shown in the image.

Check & Save the schematic and make sure the Check & save completes successfully by inspecting the CIW. Make sure there are no errors or warnings. If you have errors and/or warnings, go back and fix your schematic. Then, rerun Check & Save your schematic to make sure it completes successfully.
c. When you are creating a hierarchical schematic that contains many
levels of hierarchy, you may find it helpful to make modifications on
different cells that are instantiated in the schematic without closing
and opening different schematics. You can edit or read different
cells through a process referred to as traversing the hierarchy of the
schematic. You can traverse the hierarchy upwards and you can
ealso traverse the hierarchy downwards. The image below shows
how to descend the hierarchy to read a cell at a lower level of the
hierarchy (change the radio button to "read" if you want to edit the
cell in the lower level of the hierarchy.)

For example, to make modifications to or to read the 'inv' schematic
contained in the 'yrics' library, select it, click on "Edit →
Hierarchy → Descend Edit" or "Edit → Hierarchy → Descend Read."
The 'Descend' window will appear as shown in the image below.
Click OK in the window. The Inverter should now appear. You can
now edit it if you want; be sure to Check & Save after editing. This
will change all instances of 'inv' schematic in your hierarchical
schematics.

---

w. Let's review the creation of this inverter chain.

So far, you have instantiated four inverters, the vpulse symbol, vdc
symbol, and the noConn symbol.

Now connect the vdc to vdd (a symbol from the 'basic' library) and
gnd (a symbol from the 'basic' library). Connect the terminals with
wires (blue).

Connect the vpulse to gnd and to the net "IN1." Use wires and wire
labels.

Connect the input port 'IN' to the input of invx1, and label the input
net "IN1." Use wires and the labeling tool.

Connect the output of invx1 to the input of invx4 with a wire.

Connect the output of the invx4 to the input of invx16 with a wire.

Connect the output of invx16 to the input of Load64 with a wire.

Label the wire between invx1 and invx4 as 'IN2'.

Label the wire between invx4 and invx16 as 'IN3'.

Label the wire between invx16 and Load64 as 'OUT'.

Connect the output of invx16 to the output pin labeled "OUT".

Connect the output of the Load64 inverter to the noConn.
k. Notice the change in the calculator window. The entry has now been expanded to show the delay calculation expression.
(B) Course delivery

4) Real-world mini-sessions targeting industry, defense, and security issues
The lectures were organized as two 2-hour class meetings each week as shown in Tables I and II. The tables show the week-to-week alignment of the each of the topics in the content, the assignments, worksheets, and integrated laboratory assignments. Two themes in the course sequence are to introduce a few key living engineers who led the transformation of the semiconductor industry as well as the steady progression of the increasingly small silicon technology nodes in the past two decades (starting from 250nm node). As background, first-person stories by the key engineers are featured in the IEEE Solid-State Circuits Magazine from 2008 through 2014, where the course instructor was Editor-in-Chief; this magazine is available for download on IEEE Xplore. 

In a 10–15 minute interval between the first and second hour, students learned about real-world VLSI problems related to industry, defense, and security discussed in Constable and Somerville, Moore and Simon, and DOD documents discussed previously. Topics included high-performance adder design; high-performance microprocessor design; system performance, size, weight, and power; high-k metal gate transistors; global clock distribution networks with technical animations on high-performance microprocessors; Grace Hopper’s nanosecond wire; inverter chains in across-chip wiring; development of the integrated circuit; use of the NOR3 gate in the Apollo program discussed by Hall in “Apollo Guidance and Navigation: E-1880, A Case History of the AGC Integrated Logic Circuits;” reliability in the Apollo program; on-chip interconnections in high-performance microprocessors in the literature including publications of the instructor; and the VLSI revolution of Mead and Conway known as the “Mead & Conway Revolution”.

Examples were cited from journals including Proceedings of the IEEE International Electron Devices Annual Meeting, IEEE International Solid-State Circuits Conference (ISSCC), Intel Technology Journal, IBM Journal of Research and Development, and International Technology Roadmap for Semiconductors (ITRS). These examples provided a modern chronology of the development of increasingly small transistor sizes as technology nodes decreased from 250nm to 180nm, 135nm, 90nm, 45nm, and 22nm nodes. Overall trends in the progression of the nodes were discussed to provide a sense of the ongoing progress of the semiconductor industry. Physical characteristics of the devices published in the literature along with the associated electrical characteristics, wire image cross sections obtained by transmission electron microscopy, and yield characteristics were discussed. For example, regarding high-performance adder design, examples published in the IBM Journal of Research and Development for the POWER4 and POWER6 high-performance microprocessors were discussed. As another example, examples of the system performance of the servers manufactured with these chips were discussed. Examples of circuit design published by one of the authors was discussed (as one of the authors of this paper was Instruction Fetch Unit Integrator of the POWER4 and co-author of the POWER6 introduction paper at IEEE International Solid-State Circuits Conference, ISSCC). The introduction of the high-k metal gate transistor by Intel in the 45nm technology node was discussed with examples published in the Intel Technology Journal. Global clock distribution networks published in the IBM Journal of Research and Development in the POWER4 microprocessor were discussed.
5) VLSI Olympic Games targeted to industry and defense issues
The VLSI Olympic Games gave students an opportunity to work together on teams and individually in VLSI Pictionary, Grand Challenge Problems, and VLSI Jeopardy. One “Grand Challenge Problem” was to design a global clock distribution network driving a capacitive load equivalent to the load on the first multi-core microprocessor. The project was to design, layout, and simulate a fabrication-ready functional digital circuit. Time trials were held to prepare students to work toward a deadline, and results for the delay of each extracted layout were posted as the deadline approached. Students used the Cadence Design System software, and layouts had to satisfy all design specifications, use redundant vias, and pass design rules, and layout-versus-schematic checks. The layouts were extracted, and the extracted layouts were simulated using Spectre™.

Table I. Course content and structure in the first course (EENG653).

<table>
<thead>
<tr>
<th>Week</th>
<th>Content</th>
<th>Assignments</th>
<th>Worksheets</th>
<th>Integrated Laboratory</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pre-test</td>
<td>Silicon Run I, Silicon Run II</td>
<td>Pre-test</td>
<td>Laboratory Tasks 1-23 [32], to bring all students with various backgrounds up to speed. These tasks are: Inverter – Library, Schematic, Symbol, Spectre™ Simulation, Layout, DRC, Extraction, LVS, NC-Verilog, I-V Curve; Voltage Transfer Curve</td>
</tr>
<tr>
<td>2</td>
<td>Introduction to VLSI and the Inverter; Delay and Performance; Design Tradeoffs; High Performance and Low Power</td>
<td>HW #1</td>
<td>Return Pre-test (ungraded)</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>-</td>
<td>In-class problems</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Mid-Term Exam</td>
<td>-</td>
<td>-</td>
<td>Mid-Term Lab Exam: I-V curves; Constant current method to extract values of threshold voltage and threshold current; Linear extrapolation of threshold voltage; Dependence of inverter delay on capacitive load</td>
</tr>
<tr>
<td>7</td>
<td>Logical Effort of Logic Gates; Delay</td>
<td>HW #2</td>
<td>Logical Effort Worksheet</td>
<td>Laboratory Tasks 24-29 [32]: Inverter Chain, Ring Oscillator, Delay of Parameterized Inverter Chain; Use of the Cadence Calculator</td>
</tr>
<tr>
<td>8</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Final Lab Project: Gate Capacitance, Parasitic Capacitance</td>
</tr>
<tr>
<td>9</td>
<td>Power, Energy and Yield of More Complex Logic; Low Power Concepts</td>
<td>HW #3</td>
<td>Power, Energy, Yield Worksheet</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>VLSI Olympics: Team, individual events; “Grand Challenge Problem”; Post-test</td>
<td>-</td>
<td>-</td>
<td>Final Lab Exam: Effective Resistance</td>
</tr>
<tr>
<td>11</td>
<td>Final Exam</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Week</td>
<td>Content</td>
<td>Assignments</td>
<td>Worksheets</td>
<td>Integrated Laboratory</td>
</tr>
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<td>-------------------------------------------------------------------------</td>
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<td>---------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>Pre-test</td>
<td>HW #1</td>
<td>Activity Factor Worksheet,</td>
<td>Lab 1: 4-bit Adder Architecture #1, Subthreshold Slope, Simulation of $I_{off}$, $I_{dsat}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Power Worksheet</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Power; More Complex Logic; Critical Paths; High Performance Concepts; High Performance Microprocessors</td>
<td></td>
<td>Power Worksheet</td>
<td>Lab 2: 4-bit Adder Architecture #2, Power measurements [79]</td>
</tr>
<tr>
<td>3</td>
<td>Power; More Complex Logic; Critical Paths; High Performance Concepts; High Performance Microprocessors</td>
<td>HW #2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Interconnect; Buffering; Critical Paths; High Performance Concepts; High Performance Microprocessors</td>
<td>HW #3</td>
<td>Interconnect Worksheet</td>
<td>Lab 3: Critical path simulation through circuit on EENG653 Final Exam: Delay, Energy, Area, Tuning</td>
</tr>
<tr>
<td>5</td>
<td>Interconnect; Buffering; Critical Paths; High Performance Concepts; High Performance Microprocessors</td>
<td>HW #4</td>
<td>Robustness Outline and Worksheet</td>
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<tr>
<td>6</td>
<td>Robustness; Yield; Redundant Vias; Single Event Upsets</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Mid-Term Exam</td>
<td>-</td>
<td>-</td>
<td>Mid-Term Lab Exam: Design, layout, extract, simulate a 1-bit ripple-carry adder with custom wiring methodology, redundant vias, and power and ground grids [Year 2 only due to expiration of software license]</td>
</tr>
<tr>
<td>8</td>
<td>Adder Architectures</td>
<td>HW #5</td>
<td>Adder Arch. Worksheet</td>
<td>Project, with Time Trials, to generate layout for fabrication. Yield issues (redundant vias) are taken into consideration in the layout. [Year 2 only due to expiration of software license]</td>
</tr>
<tr>
<td>9</td>
<td>Combinational Circuitry</td>
<td></td>
<td>Combinational Circuitry</td>
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<td></td>
<td></td>
<td></td>
<td>Worksheet</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>VLSI Olympics: Team, Ind. Events; Post-test</td>
<td>HW #6</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Final Exam</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>
Figure 3 shows three examples of student layouts for adder architectures that were ready for integration using ON Semi 0.5 micron technology. This figure shows layouts for (a) an 8-bit ripple-carry adder; (b) a 4-bit carry-select adder; and (c) a 4-bit carry-look ahead adder. Use of redundant vias for yield enhancement was discussed. Students were asked to prepare the layouts using redundant vias, minimum-width wiring on Metal 1, Metal 2, and Metal 3. Students were also asked to prepare layouts using 10-signal-track-wide bits containing triple-width power and ground buses.

6) Worksheets
Worksheets are provided with problems to serve as small-group active learning exercises in class or homework assignments as discussed in Felder and Brent\textsuperscript{30} and Johnson, Johnson and Smith.\textsuperscript{31} The worksheets were structured with 1-2 pages of introductory overview material, such as a review of adder architectures and a detailed outline of the robustness chapter of the textbook. The overview material was followed by a series of increasingly complex problems, with questions and gaps for students to fill in. In class, the groups were given a few minutes for each step of the worksheet, and randomly selected students were then called on to share their groups’ solutions. The instructor elaborated on the responses and made corrections when necessary, and correct solutions were put on the board. Problems not addressed in class were assigned to the students to complete on their own time along with the regular homework assignments.
Figure 3. Physical design layouts for three adder architectures in ON Semi 0.5 micron technology with redundant vias, minimum-width wiring on Metal 1, Metal 2, Metal 3, 10-signal-track-wide bits, triple-width power and ground buses. Devices are red and green vertical stripes; wires are purple and blue; vias are dark rectangles at intersections of horizontal and vertical wires. The figure shows (a) an 8-bit ripple-carry adder; (b) a 4-bit carry-select adder; and (c) a 4-bit carry-look ahead adder.
(C) Formative assessment

7) Electronic surveying
One or more times in each lecture, the instructor used Clicker Assessment and Feedback (CAF), also referred to in the literature as student response systems, classroom response systems, CRS, clickers, [49 - 53] to query students about the course. Clickers provide the capability for real-time feedback to answer multiple-choice questions during a lecture.

In the case of this course sequence, students used the clickers to answer multiple-choice questions about the course pace and difficulty of course topics. Answers provided to the instructor from the clickers were used to adjust the course pace and to change the amount of time covering topics with different levels of difficulty (and to provide additional examples and worked problems based on student feedback).

8) Minute papers
At the conclusion of each class, students answered the question: “What was most confusing about today’s class?” on a sheet of paper. The instructor emailed clarifications of the issues raised within 24 hours to all students.

In the case of this course sequence, this approach was taken so that all students received the same information and also so that the students could benefit from questions posed from other students.

(D) Summative assessment

9) Pre- and post-tests
In the first week of each course, students were given an ungraded open-book pre-test consisting of a combination of open-ended and multiple-choice questions about prerequisite material and VLSI concepts to be covered in the upcoming course. They spent an hour of class time on the pre-test and had until noon the following day to complete it. The post-tests consisted of questions on course content that paralleled the pre-test questions. (That is, on the post-tests, some of the questions were similar to the questions on the pre-tests, and some of the questions were variations on the pre-tests, so that the students could not just do well on the post-tests by memorizing the questions and answers on the pre-tests. The goal was to test the similar concepts on the pre-tests but to vary the question to check to see that the student understood the concepts being covered). The pre-tests were returned within a week with references provided for each question. Students with incorrect answers to prerequisite questions were encouraged to consult the references and make sure they understood what they got wrong.

One in-class mid-term exam and a final exam were administered in each course. Separate mid-term and final laboratory exams were administered outside of class. Grading was done through accumulation of points in each assignment: homework, mid-term exam, final exam, laboratory tasks, laboratory mid-term exam, laboratory final exam, project, and extra credit points in post-test, VLSI World Championships, VLSI Olympics, and VLSI Jeopardy. Each student could accumulate a maximum of 1,000 points, not including extra credit points. Total point thresholds were provided at the start of each course to map to a final letter grade.
Assessment Results

While the results presented and discussed below show clear patterns of improvement in both courses and both laboratories, too much should not be made of the quantitative outcomes in view of the very low values of $N$ and the absence of control data. Results also show that students in Year 1/Year 2/Year 3 reach the same level of learning in each year. That is, no matter which year the students take the course, there is no significant difference in learning from one year to the next. This result can be seen by observing that there is a significant overlap among all three Midterm grades, and there is similar overlap for all three Final tests.

Our observations can summarized as follows:

• Class EENG653:

As was observed above in the case of the EENG653 class, diagnostic evaluations performed in Year 2 and Year 3 indicate that students in both cases represent the same population. Specifically there is no statistically significant difference in their variations and means. This analysis demonstrates that there is statistically significant improvement in Year 2 from the Diagnostic evaluation to the Post-Diagnostic Evaluation. Year 3 data also shows improvement (from D3 to P3), although it is not statistically significant. Both Midterm and Final exam results improve from Year 2 to Year 3, but only the Final exam improvement is statistically significant. This observation can be attributed to the improvement in teaching methodology.

• Class EENG695:

In the case of the EENG695 class, it should be noted that there were unusually low diagnostic test results for Year 3. Therefore, we cannot assume that in each year (Year 2 and Year 3), students have the same level of preparedness for the class. Another surprising finding is that in Year 2, the post-diagnostic results were lower than the diagnostic results and that the difference was statistically significant.

We observe that there was statistically significant improvement during Year 3 (especially considering the diagnostic and post-diagnostic evaluations). This can be attributed to the teaching methodology.

Summative Assessment

We now demonstrate the effectiveness of the pretest/post-test teaching methodology even when data is restricted to samples of small size. In recent years considerable attention has been given to pretest-posttest knowledge gain assessment. In addition to being an objective measurement of knowledge gain, this approach provides a framework for accurately assessing the influence of other factors on student’s success.

In Year 2, eight students enrolled in the first course and laboratory, and five enrolled in the second course and laboratory. In Year 3, five students enrolled in the first course and laboratory, and four enrolled in the second course and laboratory. In both Year 2 and Year 3, the response rates for the pre-tests, post-tests, mid-term exams, and final exams were 100% for both courses since attendance was required and the pre-tests, post-tests, mid-term exams, and final exams
were given during class. The response rates for the projects, mid-term laboratory exams, and final laboratory exam (given in the first course) were 100%.

In Year 2, the averages and standard deviations of the pre-test marks were \(17\% \pm 7\%\) for the first course. Figure 4 shows the class scores for the pre-tests and post-tests for the first course. In Year 3, the averages and standard deviations of the pre-test marks were \(55 \pm 21\%\) for the first course. Figure 5 shows the class scores for the pre-tests and post-test for the first course. The scores shown are only for the questions on the course material on both the pre- and post-tests, leaving out the pre-requisite questions on the pre-test. Student knowledge of material covered in the first course increased substantially for all students except Student #5 in Year 3, as reflected in the post-tests in Year 2 and Year 3.

![Figure 4. Pre-test and post-test scores for the first course (N=8) in Year 2. The scores are only for the questions on the course material on both the pre- and post-tests.](image)

![Figure 5. Pre-test and post-test scores for the first course (N=5) in Year 3. The scores are only for the questions on the course material on both the pre- and post-tests.](image)
Tables V and VI show the mean, standard deviation, standard error for the first course in Year 2 and Year 3 and for the second course in Year 3, with the p-value for the one-tailed T-test using matched data pairs.

Table V. Mean of Pre-test and Post-test for the first course in Year 2 and Year 3. The p-value in both Year 2 and Year 3 are less than 0.02.

<table>
<thead>
<tr>
<th>First Course</th>
<th>Pre-test</th>
<th>Post-test</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>N Mean</td>
<td>Standard Deviation</td>
</tr>
<tr>
<td>Year 2</td>
<td>8 0.469</td>
<td>0.0198</td>
</tr>
<tr>
<td>Year 3</td>
<td>5 0.545</td>
<td>0.213</td>
</tr>
</tbody>
</table>

Table VI. Mean of Pre-test and Post-test for the second course in Year 3. The p-value is less than 0.03.

<table>
<thead>
<tr>
<th>Second Course</th>
<th>Pre-test</th>
<th>Post-test</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>N Mean</td>
<td>Standard Deviation</td>
</tr>
<tr>
<td>Year 3</td>
<td>4 0.333</td>
<td>0.272</td>
</tr>
</tbody>
</table>

For the first course, the mean of the Year 2 Pre-test is 0.47 with standard deviation 0.20 and standard error 0.07. The mean of the Year 2 Post-test is 0.85 with standard deviation 0.05 and standard error 0.02. The p-value for a 1-tailed t-test is p = 0.00132. The mean of the Year 3 Pre-test is 0.55 with standard deviation 0.21 and standard error 0.10. The mean of the Year 3 Post-test is 0.78 with standard deviation 0.062 and standard error 0.02. The p-value for a 1-tailed t-test is p=0.01644. For the second course, the mean of the Year 3 Pre-test is 0.33 with standard deviation 0.27 and standard error 0.14. The mean of the Year Post-test is 0.80 with standard deviation 0.027 and standard error 0.027. The p-value for a 1-tailed t-test is p=0.0229.

Figure 7 shows the results of the Year 2 Mid-Term Exam and the Final Exam in the first course (Fig. 5a) and in the second course (Fig. 5b), respectively. The student numbers are maintained the same from one course to the next (students 6, 7, 8 did not take the second course in Year 2). The figure shows that the percentage scores for the Final Exams in the first course are lower for all of the students except for one student (this student did not take the second course). The reason is that the concepts in the latter portion of the first course are harder, and the course emphasized the ability to obtain an estimate of the delay through a digital circuit by hand calculations (“timing”), and to estimate device sizes to minimize the delay through the circuit (“tuning”). Most students did not correctly complete the problems related to these concepts on the final exam in the first course. As a result, the second course emphasized drills to “time” and “tune” additional digital circuits, in addition to the new concepts introduced in the second course (calculating area and power of tuned and timed digital circuits). The laboratory final exam scores exceeded 80% for all students, and that the laboratory final exam scores were higher for three of the students compared to the laboratory mid-term scores.
Figure 7. Year 2 Mid-Term Exam results and Final Exam results for the first course (a) and second course (b).

Figure 8. Year 3 Mid-Term Exam results and Final Exam results for the first course (a) and second course (b).

Figure 9 shows the results of the Year 3 Mid-Term Exam and the Final Exam in the first course and in the second course, respectively. The student numbers are maintained the same from one course to the next (student 5 did not take the second course in Year 3).

We can conclude from these results that the student knowledge increased between the final exam of the first course and the mid-term exam of the second course, since these exams are cumulative. The reason for the relatively higher results for each student on the mid-term exam of the second course is that the mid-term followed many drills on the concepts of timing and tuning digital circuits, concepts that most students missed on the final exam of the first course).
In the Laboratory Mid-Term and Laboratory Final, the goal is mastery of software skills, since students will be project managers and supervise large grants and contracts at national organizations where there is a need to understand how the software works as well as the limitations and capabilities of the software. Figure 9 shows the results of the Year 2 Laboratory Mid-Term Exam, Laboratory Final Exam, and Project in the first course (Fig. 9a) and for the Laboratory Mid-Term Exam and Project in the second course (Fig. 9b), respectively. We can conclude from the student results in both courses that the students mastered the tasks required of them. The week allocated to each laboratory was sufficient to permit all students to succeed and complete the laboratories. In the second course, three weeks were allocated to complete the project. Only one student (student #8 in course 1) had relative difficulty with the project as shown in Fig. 9a. (Year 3 Laboratory Mid-Term and Laboratory Final data are not available because the software licenses expired).

**Survey Results**

In Year 2, the response rate for the optional anonymous on-line end-of-quarter surveys for the first course was 75% (N=6), and that for the laboratory of the first course was 63% (N=5). The response rates in the second course and its laboratory were respectively 40% (N=2) and 20% (N=1). In Year 3, the response rate for the optional anonymous on-line end-of-quarter surveys for the first course was 40% (N=2), and that for the laboratory of the first course was 40% (N=2). The response rates in the second course and its laboratory were 0% (N=0) (The laboratory could not be offered in the latter half of the second course because the software licenses expired; students did respond favorably in informal comments about the laboratory in the first half of the second course).

Survey results for both courses showed that students responded favorably to the introduction of nine learner-centered instructional techniques. The survey responses were all positive in the experimental years (Year 2 and Year 3) while they were quite negative in a previous more traditional offering of the course. All of the students who responded agreed or strongly agreed that the objectives of both courses and both laboratories were made clear at the beginning of the course and were all met, the students learned a lot, the work they were required to do promoted
their learning, and that the courses would be valuable to their education and careers. They also commented favorably on many individual aspects of the course.

**Adapting and Adopting this Course at Other Institutions**


Through the use of concrete examples in the refereed literature at a variety of silicon technology nodes, this course reflects the globalization of the semiconductor industry and the impact it has had on semiconductor manufacturing, national security, and workforce development, especially in the past two decades, as discussed in Defense Science Board Task (2005), Felder (1988), Wieman (2010), and Temple III (2013).

Students’ interest and motivation to learn is heightened by integrating the basic course material with applications to semiconductor manufacturing, industry, security, and national defense. The course graphic organizer, learning objectives, CAD Manual, Olympic Games instructions, exams, handouts, and worksheets are available from the instructor by email (marylanzerotti@post.harvard.edu) or by CD. Refereed journal publications, conference proceedings are available for download at IEEE Xplore and at journal websites provided in the references. Information provided by the International Technology Roadmap for Semiconductors is provided at the URL shown in the references. The CAD Manual was cleared by WPAFB Public Affairs and is posted by Prof. Jake Baker on his CMOSedu website here: <http://cmosedu.com/cmos1/cadence/cadence.htm>.

**Conclusions**

The subject of measuring student learning is of great importance. This paper describes a three-year study of the impact on student learning through incorporating nine learner-centered instructional techniques in a two-course electrical engineering graduate course sequence targeted to real-world problems in ICs in industry, defense, and security. The study is replicated to investigate if summative assessments that indicate substantial student learning in the first experimental year are duplicated. Student feedback is favorable in both experimental years, and summative assessments in both years indicate that substantial student learning occurred.

This paper also presents performance evaluations of students in EENG653 and EENG695 classes during a three-year period at AFIT. A statistically significant improvement was observed in EENG653 Year 2 class when the Diagnostic and Post-Diagnostic evaluation results were compared. The available data for EENG653 in Year 3 suggests that there is also improvement in the Post-Diagnostic test results in comparison with Diagnostic Test results, but the difference is not statistically significant.

An analysis of EENG653 Final test results for Year 2 and Year 3 shows that there is statistically significant improvement in performance. This change is attributed to the improved teaching methodology described in this paper. For EENG695, an analysis shows statistically significant
improvement between the Diagnostic and Post-Diagnostic evaluations in Year 3. However, for Year 2, the collected data shown that Diagnostic results were significantly higher than Post-Diagnostic results. A comparison of EENG695 Midterm Tests for Years 1, 2, and 3 did not reveal any statistically significant differences. The same conclusion was reached after analysis of EENG695 Final Tests for Years 1, 2, and 3.

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