I. Introduction

Historically, microcomputer interfacing has been taught using relatively low-performance 8 bit systems. While this generally provided students with a simple architecture and instruction set, it also presented serious limitations, particularly in obtaining real-time operation. To overcome this performance shortfall, the Texas Instruments TMS320C31 DSP Starter Kit (DSK) will be used as the engine for new laboratory stations in an advanced microcomputer course emphasizing real-time interface design and operation in embedded systems. Using the DSK as the basis of a prototyping system provides far greater speed, data bandwidth, and computational capabilities, while the straightforward register architecture and floating point hardware actually reduce programming complexity.

A first stage demonstration prototype was constructed that augmented the DSK with an electrically erasable memory, boot source selection, a reset controller, and a digital/analog wire-wrap prototyping area. This allowed for either hosted operation for debugging and programming, or stand-alone embedded operation. The demonstration system was designed to accept the DSK as a daughterboard, using the DSK expansion headers for direct board-to-board connection. The prototype served as a test vehicle for the development of the final laboratory station. Additionally, this prototype board was used to construct a low cost, variable frequency, precision three-phase power supply for use in our general electrical engineering courses. Implementation required only a small number of additional components and clearly demonstrated the utility of this prototyping system, particularly in design projects. By using this prototyping system as a foundation, the students are able to undertake much more ambitious interfacing and signal processing design projects, without having to design the entire system from the ground up.

The laboratory station retains all of the features of the demonstration system, and adds a high speed electrically programmable logic device (EPLD) (which our students learn and utilize in a prior course), a solderless bread-boarding area, and a multi-output power supply. This system allows interfacing to complex devices while eliminating the need for discrete device “glue logic” with its inherent power, delay and signal concerns. We view this or similar systems as being essential to maintaining a credible EE/ECE undergraduate program. This paper will discuss the two prototype development systems and how they will be integrated into the real-time interfacing curriculum.
II. Design Criteria and Constraints

There were a number of design criteria and constraints that were considered during the development of the real-time interfacing laboratory station. One key element is that the lab station needed to be physically accessible to the student, in particular that it be a stand-alone, bench-top device and not be located internally in a host computer. Although the design criteria did not specifically address a requirement for a digital signal processor, the combination of desired computational capabilities and register set simplicity effectively eliminated most current general-purpose microprocessors from consideration. Although there are numerous microprocessors that have the requisite speed and computational power, they are all burdened with complex register architectures, unwieldy packages, and/or excessively high cost. The specific design criteria were:

1) Speed / Computational Power
   The processor had to be capable of high operating speeds (>10 MIPS), in order to allow data acquisition and processing in real time. A 16 bit word size was considered the minimum acceptable, with a 32 bit word size desired. The processor also had to have the computational hardware necessary to do real-time digital filtering and spectral analysis. While this was not absolutely necessary for the real-time interfacing course, it was intended that the lab station would also be suitable for a hardware based DSP course that is under development at the current time. The inclusion of floating point hardware was deemed mandatory, as this facilitates more intuitive and less detail-intensive algorithms while improving dynamic range and computational speeds.

2) Register Architecture / Programming
   The register architecture and instruction set had to be amenable to assembly language programming by students who’s primary microcontroller exposure had been the Motorola 68HC11 family of processors. An overly complex architecture would be more confusing than useful, so simplicity of architecture was considered particularly important. In addition to assembly language programming, the processor had to be supported by a PC-based C language compiler.

3) Glue Logic
   The intent of the course is to design and implement relatively complex hardware interfaces, but to avoid getting bogged down in masses of discrete TTL glue logic. This mandated the inclusion of a medium-sized programmable logic device which could be reprogrammed in-circuit. In addition to eliminating discrete glue logic, this would utilize (and reinforce) the students’ use of programmable logic devices from their prerequisite course work.

4) Embedded Operation
   The end goal of the real-time interfacing course is to create systems capable of autonomously performing useful tasks. This requires that the lab station be capable of operating as an embedded system, but it had to be done without requiring any external programming devices or hardware. This mandated a stand-alone boot capability, and the ability to reprogram the boot memory using the PC host.
5) Solderless Prototyping
   The design intent was to be able to enable students to develop a complete and usable
   system on the lab station. To do this, a large solderless prototyping area was required to
   support multiple interface circuits and components, including discrete and VLSI digital
   devices as well as any required analog input and output circuits. Robust, current-limited
   analog and digital power supplies were required for fault-tolerance.

6) Host Interface
   The lab station had to be supported by a PC hosted assembler/loader/debugger, and allow
   a single computer connection to perform software development, downloading, debugging,
   and programming the embedded boot memory.

7) Manufacturer Support
   It was anticipated that we would eventually write custom software for debugging and
   special application host interaction with the lab station. Therefore, the processor and
   support software chosen had to be aggressively supported by the manufacturer, with
   source code availability a key consideration.

8) Low cost
   Lab station costs had to be held to a minimum, with a design target of $350 for all
   materials, including circuit board fabrication.

Based on these criteria, the Texas Instruments TMS320C31 DSK was ultimately selected as the
engine for the lab station. The DSK is augmented by an Altera MAX7000S EPLD, which is
currently used in our prerequisite EE461 course.

III. Lab Station Operation

The lab station is designed to support the DSK as a daughterboard using its four expansion
headers for direct board-to-board connection, structured as shown in Figure 1 below. The lab
station’s normal mode of operation is to disable the DEMO mode of the DSK and use the
/UBOOT and /USERX signals for the boot EEPROM and prototyping space, respectively. To
support stand-alone and embedded operation, the lab station uses a reset controller to establish a
power-up reset signal and to support a hardware reset pushbutton. Following the power-up or
pushbutton reset signal, a defeatable low-going pulse is generated on /INT0 to force a boot from
the EEPROM at location 0x1000. However, the PC host can override this function at any time
and force an /INT2 boot from the host port interface. This permits a manual reset to test the
EEPROM software, while allowing the PC host to regain control of the lab station by simply
sending a ‘RESET’ command from the DSK debugger.
A 28C64A 8 kilobyte EEPROM is used to hold program data for embedded system operation. This is tailored to match the TMS320C31's onboard RAM size. EEPROM write protection can be selected, or the EEPROM disabled entirely, if desired. To map address 0x0000 of the EEPROM to DSK address 0x1000 without additional decoding, the EEPROM uses the DSK A13 line as its A12 input.

To provide maximum electrical protection to the DSK, all signals to and from the prototyping area are buffered. Although this adds a small propagation delay, it is acceptable in the lab environment, and preferable to damage to the DSK board due to electrostatic discharge (ESD) or incorrect connections in the prototyping area. These buffers are all socketed parts that can be replaced easily and inexpensively if they are damaged during student use. With +/-12V voltages available in the prototyping area, there is some possibility of accidental cross-connection to the various logic lines that must be guarded against. There are 16 bits of buffered data lines mapped into the USERX space, as well as the 16 low order address lines. The /RDY line returning to the DSK is only enabled when the /TRI line is asserted, preventing contention with the DSK’s PAL output. A similar arrangement uses a single switch to prevent contention between the signals connected to the DSK’s analog interface circuit (AIC) and the same signals in the prototyping area when the AIC is used.

The lab station also holds a socketed Altera MAX7000S EEPROM based programmable logic device, containing 2500 usable gates and operating with a propagation delay of 7.5ns. The MAX7000S receives the system /RESET signal and a buffered 25 Mhz clock signal, and there is a provision to install a separate clock oscillator if desired. The MAX7000S supports in-circuit programmability through a 10 pin JTAG header. The remaining 62 available I/O pins are available at female headers to allow solderless connection to the prototyping area.
A multiple-output linear power supply provides +5V and +/-12V to the buffer logic and the prototyping area, with the ability to withstand short circuits and cross connections. A separate transformer feeds the DSK’s onboard regulator, which also provides power to the EEPROM and reset control circuits. Separate power indicators are provided for the two power sources. A large prototyping area is capable of supporting sixteen (16) 16-pin DIP packages and discrete components, with 6 power busses, 8 logic indicator LEDs, and 8 logic switches. The entire package is housed in a hard-shell suitcase enclosure.

IV. A Design Application

As part of the development of the lab station, an initial prototype circuit board was designed to test the concepts and hardware to be implemented in the final design. This board supported the DSK as daughterboard, augmented with reset and boot control, boot memory, and a wire-wrap prototyping area, all in an area of only thirty eight (38) square inches. To demonstrate the system’s capabilities, a precision three phase digital signal generator was constructed on one of the circuit boards. Using the floating point hardware, a single phase sinusoid is generated mathematically utilizing complex vector rotation. Due to this technique, no look-up table is necessary while obtaining a resolution up to 3600 samples per cycle. Output frequency control is obtained through a combination of interrupt timing and the angle of the rotation vector. The other two phases are obtained by complex vector rotation of the basic sinusoid. Using a serial interface, the three digital signals are fed to three multiplying digital to analog converters (MDACs). A precision voltage reference is fed to a fourth MDAC, which is then controlled to provide the voltage reference to the three phase signal MDACs, and thus control the output amplitude. No filtering is provided for the MDAC outputs, as the 12 bit resolution results in quantization noise below the required threshold in our application. An LCD panel and front panel switch bank allow display and control of amplitude and frequency.

The TMS320C31 instruction set and floating point hardware allows for a very compact implementation of the complex vector rotation algorithm, requiring only twenty-five machine instructions to load, calculate, and store each sinusoid sample. The speed of the TMS320C31 permits operating up to the design frequency of 100 Hz, with a sample rate of 36,000 samples per second per phase. The actual limiting factor on the sample rate is the serial transmission rate to the MDACs. This design clearly validated the selection of the ‘C31 DSK, and demonstrates the power and capability available in the final lab station.

For classroom demonstration use, the signal generator is augmented with a three channel power amplifier, allowing the direct drive of small motors or light bulbs. The use of light bulbs is a particularly effective visual method to demonstrate the concepts of phase rotation and the interrelation of the phase signals, by operating the three phase signal at very low frequencies (less than 1 Hz) and increasing slowly to the more conventional 60 Hz. Additionally, the three signals can be “frozen” at any time, permitting students the opportunity to obtain direct measurements to demonstrate phase voltage summation to zero.
V. The Curriculum

The EE462 Microcomputer Interfacing course syllabus was redesigned to reflect the use of the DSK based lab station. The syllabus includes the topics as summarized below.

- TMS320 Register Architecture and Instruction Set
- Lab Station Memory Map, Bus Signals and Timing
- Parallel Interfacing, Address Decoding and Bus Control
- Serial Interfacing Techniques and Protocols
- Hardware Interrupts and Interrupt Service Routines
- Direct Memory Access (DMA) Controller Applications
- Display and Control Interfaces
- Signal Acquisition
- Final Design Integration Project

Each topic area is supported by one or two hands-on laboratory design exercises that expose the students to a new device or concept amplifying the syllabus topic. The final design project involves incorporation of several interface elements and all necessary software into a completed system, such as, creating a digital meter that measures and displays the true RMS voltage of an analog signal, or an audio signal processor that acquires an analog signal, digitally manipulates it, and then outputs the converted audio signal.

In addition to providing glue logic functionality, the MAX7000S is also capable of implementing complex digital functions itself, providing an extra resource to the student and an extra dimension to the curriculum. To study communications peripherals, for example, there is the option of interfacing an existing UART device with the MAX7000S providing all required glue logic, or having the student design, implement and interface the UART completely within the MAX7000S itself. This presents an opportunity for two very different and complementary learning experiences using the same hardware and with the same functional objective.

VI. Conclusions

The ‘C31 DSK based lab station meets all design requirements, and provides a complete laboratory and development environment for student use. The marriage of the DSP’s power and speed, the programmability and flexibility of the MAX7000S EPLD, and the solderless prototyping area creates a mix of capabilities and flexibility not otherwise available. To support the hardware, a number of tools are available to support software development, code simulation, and real-time debugging.

The initial wire-wrap prototype circuit board can also be used to provide a ready expansion of the DSK capabilities, and allow students to use the DSK as the center of their design projects. At a fabrication cost of less than $50 in quantities of just four (4) circuit boards, it is possible to procure a complete, bootable DSK prototyping system for well under $200 total cost. This makes significant processing power available for student design projects on a very flexible platform, and is particularly suitable for projects that involve hardware and software design.
Rather than proceeding directly to a wire-wrap prototype or having to debug circuits piecemeal, the lab station can be used to test, evaluate, and debug the student’s hardware design prior to committing effort to wire-wrapping the circuits into place or constructing circuit boards.

With the power and capabilities of the lab station, it can also be used to support student research projects in signal acquisition and processing by serving as the vehicle for unique hardware system development.

The single greatest limitation of the DSK-based lab station is the modest amount of onboard memory. Memory can be added in the prototyping area for a specific application, but is limited to a 16 bit width. Although the available memory is quite adequate for use in the real-time interfacing course, additional memory would greatly expand the ability of the system to perform complex algorithmic computation and large scale signal processing, and may be provided in future versions of the lab station.

VII. Schematic Diagrams

Schematic diagrams for the lab station and the three phase signal generator are attached in enclosures (1) and (2), respectively.

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Notes:
(1) U1, U2 & U3 POWER FROM DSK +5V