An integrated usage of circuit simulation and spreadsheet for an enhancement of circuit design and semiconductor device instruction

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Abstract

The circuit simulation construct is a network of nodes interconnected by component devices that are responsive to the voltage and current stimuli applied as sources and signals. The component devices may be simple linear form or they may be non-linear devices, in which case they are usually of semiconductor origin. Each different type device owns a set of specific parameters that define its operation. The circuit simulator decomposes the circuit and ascertains the electrical facts of the circuit in the form of node voltages and branch currents, outcomes which are peculiar to the physical effects represented by the strengths of these device parameters and therefore of critical concern to a circuit designer.

Semiconductor devices are generally devolved in the classroom by their device physics and the principles of operation that control the flow of electrons and holes. Basic first-order concepts lend themselves to mathematics that is reasonably tractable and can be readily developed by the versatility of the spreadsheet environment. However, for sub-micron devices, where the field effects are very intense, much of the first-order physics loses ground to second-order effects, most of which are abstract and often impenetrable to the circuit designer. And often any exposition of these second-order effects is a time-consuming burden to the instructor, whether for circuit design or for device physics.

This paper identifies a technique that is invaluable to the circuit designer and/or semiconductor devices instructor by which the circuit simulations and the spreadsheet environments are integrated to resolve devices and/or circuit design questions. The environment can also be used for an empirical cross-coupling of device theory and circuit design. The student version of Cadence/ORCAD/pSPICE, which is the most common classroom circuit simulation platform, is the principal operational utility, with the Excel platform as the complementary spreadsheet utility.

Proceedings of the 2005 American Society for Engineering Education Annual Conference & Exposition

I. Introduction and Background

Design of modern circuit electronics is defined by a cycle for which circuit concepts are confirmed and assessed by means of a circuit simulation utility. The most common platform for circuit simulation in the academic environment is one of the several versions of the SPICE [1-3] utility, since it's emphasis is integrated circuit design. As the circuit design process has matured this utility has evolved into a friendly and flexible resource that has found a role in almost every part of the electrical and computer engineering curriculum.

The mathematics for device models is developed from semiconductor physics. Generally, the device physics dominates the classroom instruction, and application to device simulation is either an assumption or is passed along to other parts of the curriculum. Device physics usually demands a great deal of overhead, can dwell on anything from thermodynamics to field theory. And the devices themselves can range from two-terminal non-linear resistances to four-terminal transistors. Use of SPICE to illustrate performance characteristics of devices are not uncommon in the circuits courses, but are uncommon in the semiconductor devices courses. Uses of spreadsheet calculators are also not uncommon, and with their graphical enhancements have been used in many instances to define and formulate mathematical abstractions in a more visual sense.

Most of the instructional framework and time commitment given to semiconductor devices is submerged in the mathematical expositions necessary to describe the physics of the device [5]. This is particularly true for small-dimension devices where high-field effects [6-9] predominate and change the nature of the device performance. Most of the literature is dedicated to semi-empirical physics assessments and use of special test vehicles to evaluate the effects in question. The requirement then falls upon the instructional process to either commit to relatively selective literature analyses or to rely on the first-order physics to define the operational aspects of the semiconductor devices in question. Higher-order device models must accommodate so many effects that the analytical overhead becomes enormous, and an exposition can overwhelm both the semester time frame and the students, and often leaves the engineers in a subtended role for which they do not have a high confidence factor in their semiconductor device foundations.

It is good form to make use of the circuit simulator and its platform of models and embedded formulations to reveal physical effects, and this technique has been treated [10]. Circuit simulators, particular those in the public domain, give the instructor a very flexible and extensive platform and a considerable gain in coverage and throughput. Similar benefits may be derived from use of the spreadsheet environment. In this paper the two are integrated to form a platform that yields considerable perspective and insight into both the circuit domain and the device domain, whether as an educational platform or as an analysis platform.

II. Simulation/spreadsheet utility applied to two-terminal device constructs

The simplest constructs are often the most informative, and in this case identify both the most direct usage of the platform and a set of simple direct relationships. The situation shown relates to the semiconductor *pn* junction diode. It is embedded in almost all semiconductor parts, since most semiconductor devices are constructed of many layers and patterns of *p*-type and *n*-type semiconductor materials. In reverse-bias the *pn* junctions is a capacitance and its performance in this respect is readily explained by means of first-order electric field theory. The behavior is represented by figure 2-1, for which the charges that are 'uncovered' by the E-field represent a capacitance with distributed charge. This phenomenon is important for many devices and important to many circuit concepts.

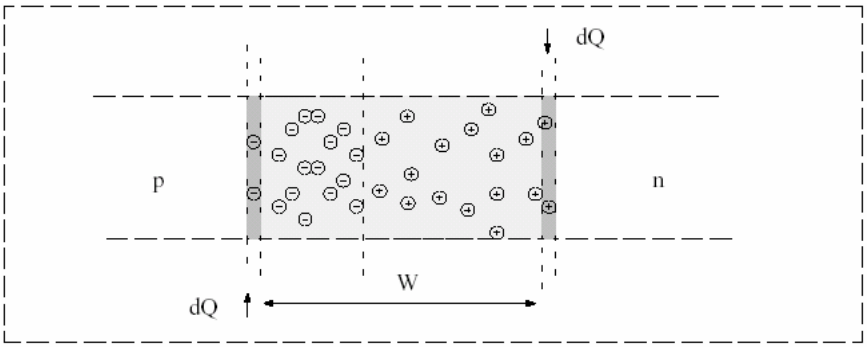


Figure 2-1 Uncovered (depletion) charge in the (reverse-biased) *pn* junction

The charge distribution follows the impurity profile since impurity sites are ionized by the junction E-fields. It takes manipulation of pSPICE using goal functions[10] to reveal this behavior, with a circuit construct that permits an uncontaminated assessment of C(V) via the form

$$C(V) = \text{imag}(\ I(\omega)/V(\omega))/(2\text{pf}) \qquad (2\text{-}3)$$

where $\omega = 2\pi f$, and with f being the applied frequency.

The impurity profile $N(x)$ is defined in terms of the slope of $1/(C(V))^2$, for which

$$N(x) = \frac{2}{q\,\varepsilon_S}\left[\frac{d}{dV}\left(\frac{1}{C_J^2}\right)\right]^{-1} \qquad (2\text{-}4)$$

The pSPICE utility is then called upon to present a plot of $1/C_J^2$, as shown by figure 2-3b. Figure 2-3a shows the test circuit. Voltage V(reverse) = V_R has been stepped from 0 to 20 in increments of 0.1V, and a frequency sweep from 1kHz to 2 kHz (relatively narrow range) has been invoked for each value of *V(reverse).* Figure 2-3a shows the pSPICE R-C schematic that must be applied to define *C(V).*

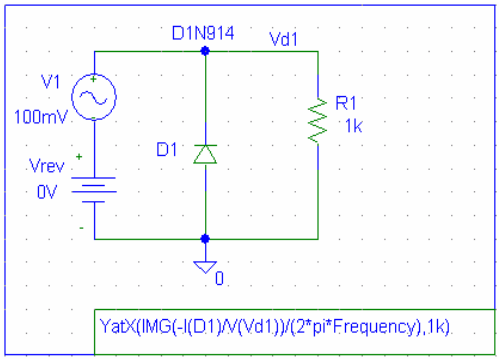


Figure 2-3(a)

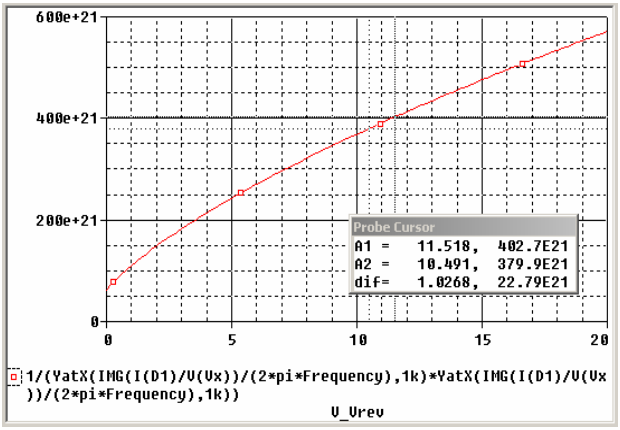


Figure 2-3(b)

Figure 2-3. pSPICE construct and performance analysis results for $1/C_J^2$ output

The pSPICE goal function (under the *Performance Analysis* menu) is of the form

YatX(IMG(I(D1)/V(VD1))/(2*pi*frequency),1kHz)

and this construct, as indicated by the trace specification of figure 2-3b is used to emulate equation (2-3). The value of slope of $1/C_J^2$ at any point along the trace can be extracted. One such point is indicated by the cursor window and gives value 22.79×10^{21}(1/VxF^2), for which, using equation (2-4) identifies a doping concentration of:

$$N(\text{doping}) = 2/[(1.602\times10^{-19})*(1.05\times10^{-12})*(22.79\times10^{21})*10^{-8}] = 5.22\times10^{16}\ \#\text{cm}^3$$

This level of N(doping) is not atypical of *pn* junction doping levels for a Si junction, even though this is a discrete part and the fabrication specifics are unknown. Physical constants $\varepsilon_S = 1.05\times10^{-12}$ F/cm and electronic charge $q = 1.602\times10^{-19}$C and area 1mm^2 = 10^{-8} cm^2 have been assumed in making the calculation.

However, a much more significant option which is not accessible to the circuit simulation is to take this same information and identify the doping profile as a function of depth. The E-field reaches into the semiconductor according to

$$W = L_B\sqrt{2(V_R + \phi\ )/V_T} \qquad (2.5)$$

where L_B is the Debye length and V_T is the thermal voltage = k_BT/q for which k_B is the Boltzmann constant, q is the charge on the electron and T = absolute temperature.

This environment can readily make use of the collateral platform provided by the spreadsheet. It is a nearly trivial exercise to copy and paste the data point generated by the circuit simulator into the

spreadsheet. The spreadsheet can be used to extract a derivative according to equation (2-4) and a profile depth according to equation (2-5) and create an X-Y plot. The result is indicated by figure 2-4.

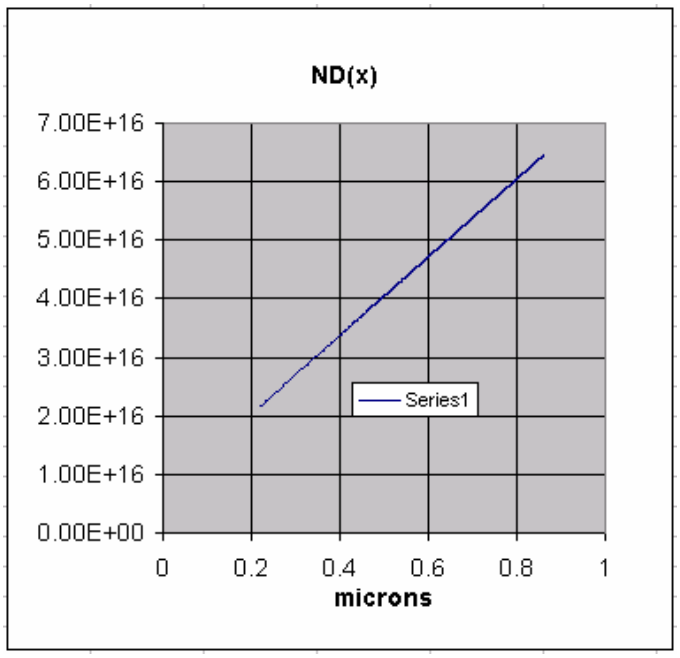


Figure 2-4. Spreadsheet (Excel) generated construct of *N*(doping) vs depth, using data taken from figure 2-3(b). In this case it is actually known that the doping profile is linear. The analysis is a confirmation of the technique.

Information of this type is often vital to the fabrication process since it takes a great deal of implant technology and thermal processing to create the semiconductor profile. The measurement (in this case represented by the simulation/spreadsheet process) of this profile is an important assurance test.

III. Illustrations of simple circuit constructs affected by component parameters.

The circuit simulation process is one for which a circuit is often assessed for performance as a function of any embedded parameter. The most likely situation is one for which an output response is assessed as a function of a given component value. For simple linear circuits output performance relationships such as amplitude or time responses can usually be derived. For circuits that include non-linear devices the performance relationships are less accessible, and so the circuit simulation itself becomes the performance indicator. Predictive mathematical relationships must be heuristically defined, and the simulation plus spreadsheet environment is an ideal combination for developing such information

A particularly simple and direct illustration is indicated by figure 3-1, which is a four-stage voltage multiplier. This circuit takes a sinusoidal signal of amplitude *Vp* and yields an output that ideally yield $V_{out} = 4 \times (2Vp)$.

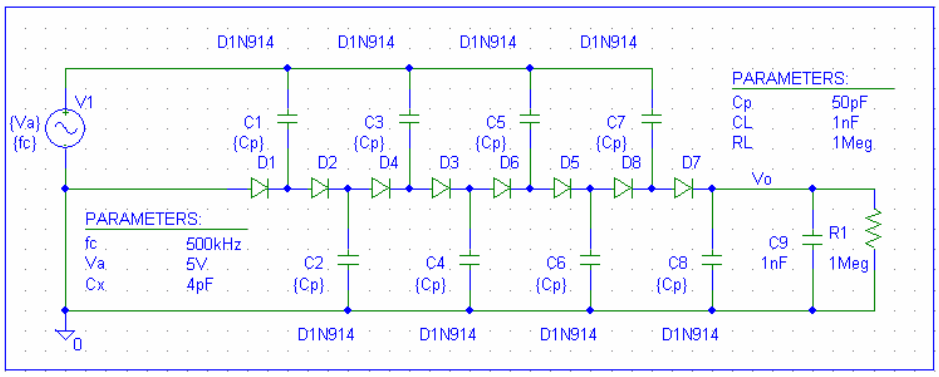


Figure 3-1. Four-stage diode-capacitance voltage multiplier

However, with non-ideal diodes, as are implicated by a circuit simulator, the charge transfer process is afflicted, and collateral circuit elements play a somewhat different role than expected. In this case, the capacitances are treated as circuit parameters. When the diodes are ideal rectifiers, the only aspect of the circuit that is affected is the rise time. When the ideal diodes are non-ideal, as represented in this case by parts from a device library, then the output level is also affected, as represented by figure 3-2.

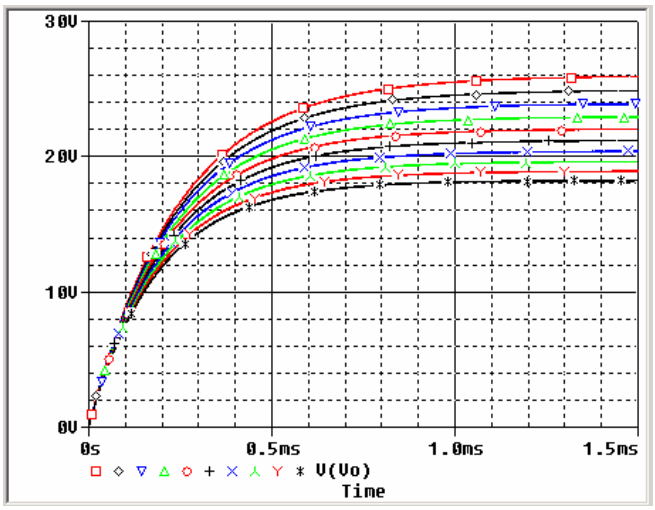


Figure 3-2. Vo(t) response of the four-stage diode-capacitance voltage multiplier

Ideally the output should rise uniformly to $Vo = 4 \times (2\ Vp) = 40V$. Vp in this case is 5V. With non-ideal diodes, the output level is not only afflicted, it becomes dependent on the value of the transfer and accumulation capacitances, as illustrated by figure 3-2. The output level is reduced because charges are split between the component capacitances and the parasitic junction capacitances of the diodes. And the relationships are non-trivial.

The non-ideal output behavior can be realized by a pSPICE goal function, as illustrated by figure 3-3. This response can then serve as a database that can be pasted into spreadsheet in exactly the same manner as that used in the previous section.

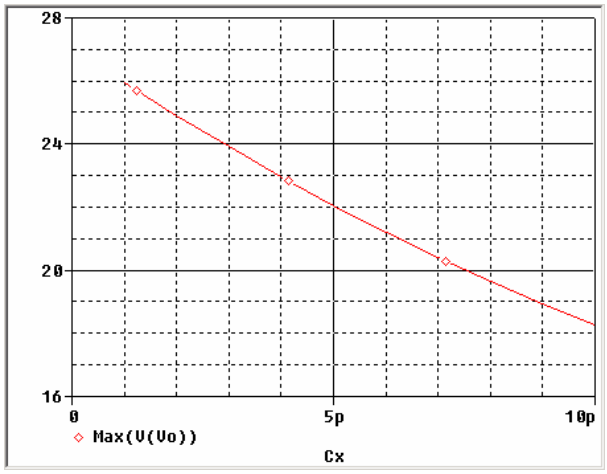
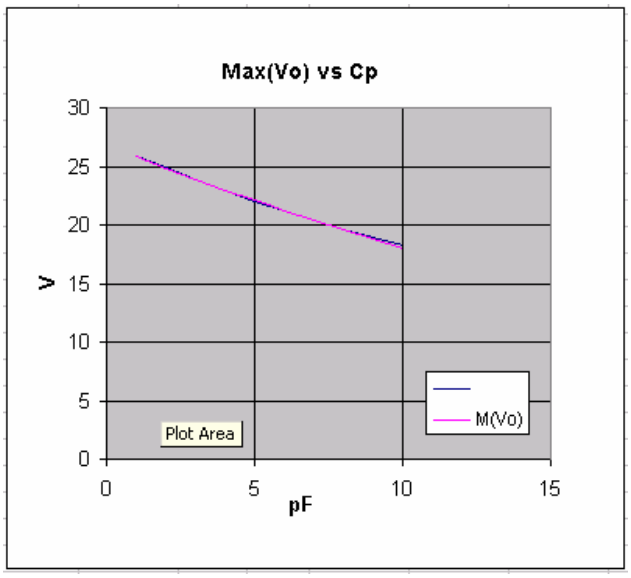


Figure 3-3 Goal function data for Max(Vo) vs Cp

It is evident from figure 3-3 that *Vo* decreases with *Cp*, and it may be important to the circuit designed that a relationship be defined as a predictor. An empirical model can be elected, and in this case it was (arbitrarily) chosen as

$$Vo(\max) = V_1 - V_n * (C_p - C_1)^a \qquad (3\text{-}1)$$

With data imported into the spreadsheet, the values of *V1, Vn, C1* and a can be incremented in a systematic manner and in the process a reasonable fit can be accomplished, as represented by figure 3-4a. The parameter table is identified by figure 3-4b



V1	25.9
Vn	1.1
Co	1
a	0.9

Figure 3-4b: Parameter values

Figure 3-4a: Overlay of data from figure 3-3 and empirical equation 3-1

The empirical relationship can be chosen as a matter of suspicion of a physical phenomenon that decouples the circuit or as a matter of data behavior, as represented by this illustration. It is apparent that *Vo(max)* decreases approximately linearly with *Cp* and the choice of relationship as given by equation (3-1) is a reflection of this observation.

IV Circuit constructs afflicted by device parameters.

Situations at the next level of abstraction are the instances in which the device parameters affect circuit performance, and these situations can either be of concern to the circuit performance or to the device performance, depending on the demand requirement. As a classroom artifact, the principal concern may be interpretation of device performance, probably devices of sub-micron feature size as used in present technologies. Sub-micron devices are subject to fields that are so intense that the device physics models are dominated by second-order effects. The effect of different parameters on the device is a difficult explanation and as many graphics utilities as possible need to be employed.

This exercise uses an analog IC deign circuit to examine micropower gain as a function of bias. The test circuit is shown by figure 4-1

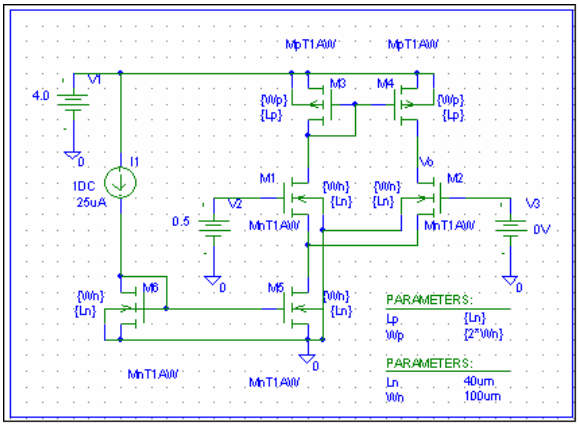


Figure 4-1a: Source-coupled pair

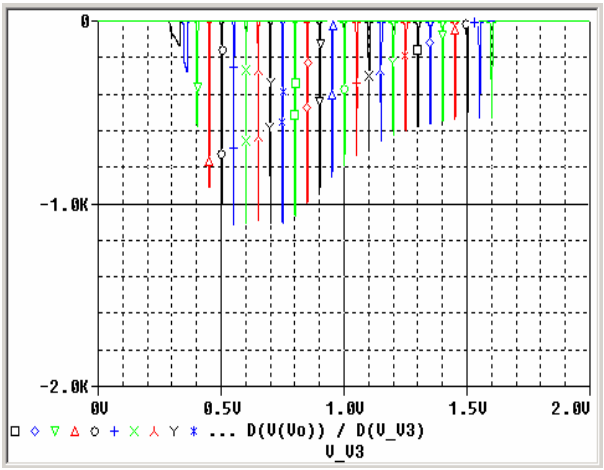


Figure 4-1b: SCP gain response

Figure 4.1b is a set of traces for which *Vo* is assessed as a function of a sweep of *Vin*, for which the derivative, which is the transfer gain of the circuit and can readily be accomplished by SPICE without any trauma on the part of either spice or the student. In this case the circuit is a micropower circuit for which MOSFET devices M1 and M2 are operating in the subthreshold regime. The subthreshold regime is a realm where few circuits dare to tread, and where the device physics models are even more suspect than they are in the normal 'conductive' regime. In this case bias voltage V2 is stepped, which not only shifts the position of the transfer slope but affects its magnitude. And the magnitude of the transfer slope is the small-signal transfer gain.

So the need of this circuit design is to identify gain behavior, preferably with some form of predictive mathematics. With the 'SPICE plus spreadsheet' usage, this can readily be accomplished, as represented by figures 4-2 and 4-3.

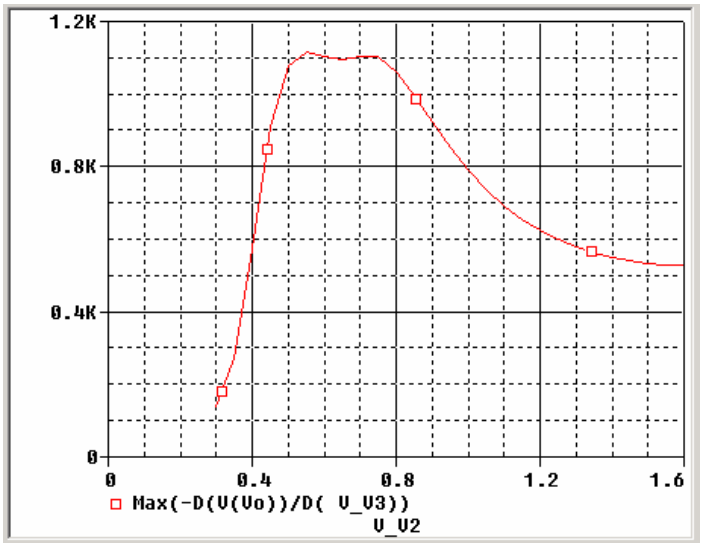


Figure 4-2: SCP gain response, extracted using goal function.

Figure 4-2 is an extraction of the amplitude(s) of the transfer gain using the 'goal function' indicated below the horizontal scale. Figure 4-3 is the same data as traced by figure 4-2 copied and pasted into the spreadsheet, which is re-plotted and fitted to the empirical function.

$$\text{Gain} = Av0+Av1*(Vb-V1)^{n1}+Av2*(Vb-V1)^{n2}*\exp[(Vb-V1)/Vx] \qquad (4\text{-}1)$$

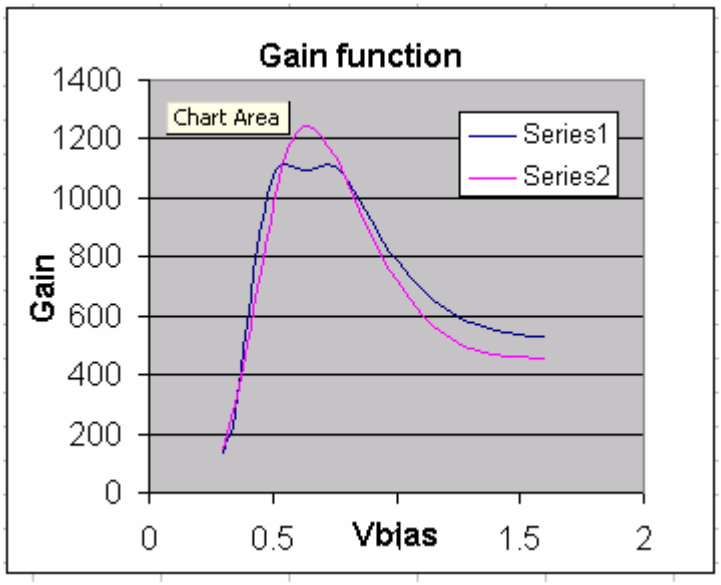


Figure 4-3: Excel fit to trial equation

for which the parameters, fitted by trial and error and a few obvious values (e.g. endpoints and transitions) are:

Av2	3.00E+05
Av1	2.70E+02
Av0	150
V1	0.3
Vx	0.12
n2	2.75
n1	0.35

Table 4-1: Fitted parameters for the analytical trace of figure 4-3

In this case, it is evident that a special fitting function has been chosen, not because it follows any physics, but because it is from a menu of functions that do resemble the behavior represented by the data response. This begins to take the student participant into the analytical realm where most device physics models are constructed and for which a response appears to obey mathematics that can likely be traced to the underlying physics. This approach then begins to draw the students into the realm where many journal publications flourish.

V. Conclusions

The constructs that have been identified in the preceding sections are but a few of many options, since the capability of the simulation-spreadsheet software pair to identify the effect on *I(V)* or *C(V)* behavior of working devices is extensive and has reached a point of viability that makes it a classroom tool that can be used to accomplish much more than proof tests for circuits and circuit design. Most of the capabilities of the simulator that have provided this enhancement are a consequence of upgrades in the post-processor. These upgrades now allow the simulation data to be manipulated in ways that are much more than a simple electrical analysis, and extend well beyond the focus of circuit proof and performance analysis. And likewise the spreadsheet is a friendly and mature product that gives considerable flexibility and analytical power.

And device models in pSPICE have evolved over time to a point that they now represent actual device behavior to a higher degree of accuracy than simplified models ordinarily necessary in the classroom or laboratory. This paper has found a practical and frienly platform for to investigation of device and circuit behavior from simulation that are more accurate and less complicated to implement than simple theories or laboratory measurements.

The capability to analyze devices is a demand item, since circuits of micron and sub-micron dimensions are difficult to assess both before and after the fact, since the devices are only assessed as part of a test vehicle, which leaves the engineer at the mercy of the complex relationships developed thereto. For example the level-49, BSIM3V3 model [3], as accepted and continuous a simulation model as it may be, is an engineer's nightmare, since the model requires 108 parameters and mathematics that is nearly impenetrable without large

investment of time and detailing. It is a model that is derived as a quadratic approximation, which provides a baseline simplicity, but requires a number of patches in order to assure continuity over all regimes of operation. The BSIMS3V3 model has then been upgraded and appended since its introduction and has since it has accumulated many small-geometry and short-channel effects, most of which are more than a little arcane, and it is a large task to unravel the relationships embedded thereto and their effect on circuit performance.

For example, the BSIM3V3 (now BSIM3V4) threshold voltage is of the form:

$$
\begin{aligned}
V_{TH} &= V_{TH0} + K_1\left(\sqrt{\phi_S - V_{BSeff}} - \sqrt{\phi_S}\right) - K_2 V_{BSeff} && \text{Zero-bias body effect}\\
&+ K_1\left(\sqrt{1+\frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\phi_S} + (K_3 + K_{3b}V_{BSeff})\frac{t_{OX}}{W'_{eff} + W_0}\phi_S && \text{LDD and narrow width}\\
&- D_{VT0w}\left(-\exp\left[-D_{VT1w}\frac{W_{eff}L_{eff}}{2l_{tw}}\right] + 2\exp\left[-D_{VT1w}\frac{W_{eff}L_{eff}}{l_{tw}}\right]\right)(V_{BI} - \phi_S) && \text{narrow width, short channel}\\
&- D_{VT0}\left(\exp\left[-D_{VT1w}\frac{L_{eff}}{2l_t}\right] + 2\exp\left[-D_{VT1w}\frac{L_{eff}}{l_t}\right]\right)(V_{BI} - \phi_S) && \text{charge-sharing}\\
&\left(\exp\left[-D_{sub}\frac{L_{eff}}{2l_{t0}}\right] + 2\exp\left[-D_{sub}\frac{L_{eff}}{l_{t0}}\right]\right)(E_{ta0} - E_{tab}V_{VBSeff})V_{DS} && \text{DIBL} \qquad (5\text{-}1),
\end{aligned}
$$

and many of the terms relate to more parameters than those evident within the expression. Relationships of this level of complexity make the process of interpreting device parameters and high-field effects sufficiently arcane so that many circuit designers adopt a plug and pray attitude toward circuit design. As represented by equation (5-1) the overhead necessary to diagnose device effects can consume an ocean of time, and still leave the design engineer relatively insecure about his interpretation. When the model take pages to describe the exhibit, much less the explanations, even the probability of typographic errors becomes a significant concern, and they do exist in some of the documentation for the BSIM3V3 and BSIM3V4 models.

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