# An Open-ended Design Project for a First Communications Course

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Abstract

The United States Naval Academy offers a junior level communications systems course that includes a significant amount of hardware design. A signals and systems class is the prerequisite for this course, during which the necessary fundamentals are developed to allow for an immediate discussion of higher order modulation schemes. The open-ended design project deals with designing, building, and testing a 16-QAM communications link. This project allows for a significant amount of design experience prior to starting the traditional senior-year design sequence.

## 1. Introduction

The United States Naval Academy offers a junior level communications systems course[1] that includes a significant amount of hardware design. This course is taught in a 3-2-4 format (three hr/wk of lecture, two hr/wk of lab, for four hours of total credit). This course represents the student's sixth EE course and the beginning of their sixth semester in college. *Signals and Systems*[2] is the prerequisite for this course, during which the necessary fundamentals are developed to allow for an immediate discussion of higher order modulation schemes.

The open-ended design project deals with designing, building, and testing a sixteen level quadrature amplitude modulation[3] (16-QAM) communications link and allows for a significant amount of design experience prior to starting the traditional senior-year design sequence.

## 2. Design project discussion

The design project is presented to the students with only four specifications;

- the minimum data rate of approximately 1,000 bits/second (bps),
- the need to be able to easily increase the data rate from 1,000 bps to at least 10,000 bps,
- the signal constellation points must be at $\pm 3$ volts and $\pm 1$ volt, and
- pre-fabricated D/A converters may not be used.

Few specifications are provided in the hope that the students will re-examine the 16-QAM modulator from an implementation perspective. A simplified block diagram of a 16-QAM baseband modulator is provided in figure 1.

Note: the students are not given a parts list to draw from. However, components are available from several labs and the general parts rooms for the EE department.

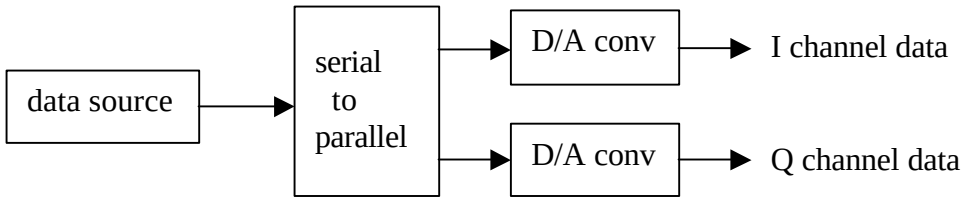


Figure 1. 16-QAM baseband modulator block diagram.

A group brainstorming session usually lasts about an hour, during which dozens of possible ways to implement the 3 major blocks shown in figure 1 are proposed. During the brainstorming session, the reasons for each one of the specifications becomes clear. Specifically,

- The minimum data rate is necessary to allow audio frequency components to be used.
- The need for a variable data rate allows intersymbol interference (ISI) to be investigated later in the semester.
- The specified constellation voltages allow for minimal noise effects.
- The restriction on not using prefabricated D/A converters allows the students to explore the internal circuitry of a very simple (2 bit) D/A converter.

Brainstorming is followed rapidly by team partner selection and an initial design. The first few lab periods allow for equipment familiarization and an investigation of the properties of pseudorandom (PN) codes. A PN code generator can be used to generate a digital message and is routinely considered as a source for the random data block shown in figure 1. Four lab periods deal with the 16-QAM baseband modulator design, construction, and testing.

At this point, labs using student-designed hardware investigate a dispersive channel, intersymbol interference (ISI), and the eye-diagram. Mid-way through the semester, in class presentations allow valuable communication skills to be gained and every student to learn from the design successes or failures of their peers. These presentations are necessary since most of the student designs are unique. As an example, a few of the solutions to the random data source design challenge are provided below,

- Pseudo-noise (PN) generator using CMOS gates on a protoboard,
- PN code generator using a field programmable gate array (FPGA),
- Sampling and thresholding a white noise source,
- Sampling and thresholding a music source, and a
- C++ program that generates PN code using a PC, then streaming the data to the PC's parallel port for connection to the student built D/A converters.

Periodic "reset labs" allow design teams that are struggling to get their systems working, to get caught up. Later, spectral translation to a few hundred kHz, allows for class and lab discussions

of bandwidth and spectral masking. To avoid RF circuit design issues, the "few hundred kHz" carrier frequency is used. Analog mixers, such as the AD-633N, prevent traditional RF passive mixers from being needed. The block diagram associated with the spectral translation circuitry is shown in figure 2. The summation operation shown in figure 2 is actually accomplished by the digitizing oscilloscope using the "ch 1 + ch 2" math function.

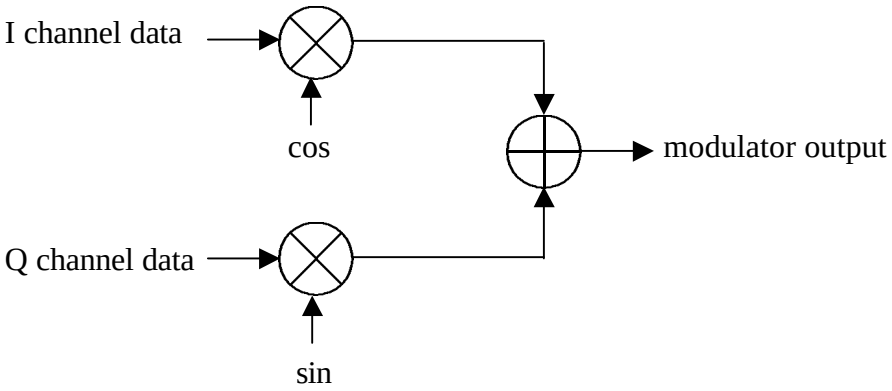


Figure 2. Spectral translation block diagram.

Finally, demodulator design and symbol/bit recovery labs follow. The semester ends with a complete simplex communication system having been designed, built, and tested.

## 3. Conclusions

This open-ended design experience lasts the entire semester and requires a methodical approach to solving an ill-defined problem. During the design lab, valuable team and presentation skills are developed. This project allows for a significant amount of design experience prior to starting the traditional senior-year design sequence. Student opinion of this lab experience was overwhelmingly positive!

## References

[1] L.W. Couch II, *Digital and Analog Communication Systems*, Prentice-Hall, 1997

[2] A.V. Oppenheim and A.S. Willsky, with S.H. Nawab, *Signals and Systems*, Prentice-Hall, 1997

[3] W.T. Webb and L. Hanzo, *Modern Quadrature Amplitude Modulation*, IEEE Press, 1994

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