Analog and Mixed-Signal IC Design in a Junior Electronics Course Sequence

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Abstract

The integrated circuit revolution has impacted virtually all fields of engineering. The main driving force behind this revolution is Complementary Metal-Oxide Semiconductor (CMOS) transistor technology. As CMOS integrated circuit "chips" have come to dominate analog and digital electronics, introductory electronics courses in Electrical and Computer Engineering programs have evolved to place greater emphasis on CMOS transistors and amplifiers. However, due to the perception that chip design is too esoteric, both lecture and laboratory coverage of this important topic are usually deferred to more advanced courses. Design experiences are instead limited to "breadboard" circuits using discrete components and operational amplifiers.

This paper presents a new approach to teaching introductory electronics that incorporates the design and layout of CMOS chips. The coverage of topics in the two-semester sequence only needs minor changes from the traditional approach. Topics on the physics and design of bipolar devices are de-emphasized, but not eliminated. Similarly, we retain basic coverage of discrete-component design. We add coverage of integrated circuit processing and the design of basic analog and mixed-signal circuits at the transistor and layout levels.

In the lab, students start with traditional exercises using operational amplifiers, discrete components, and circuit simulation. They next undertake integrated circuit projects that include the design and layout of basic logic gates and differential pairs. The lab concludes with a capstone project where students design, lay out, and simulate complex circuits based on material found in IEEE technical publications.

The resulting course sequence gives ECE students a better understanding of the relationship between chip design and electronics. It also offers hands-on experience with circuit design at the chip level. The design and fabrication of student projects generates enthusiasm and motivates students' efforts to grasp underlying fundamentals and theory.

1. Introduction

Continued improvements in transistor and integrated circuit technology have brought about major changes in the design of electronic systems. While early integrated circuits

(ICs) combined a few dozen transistors to form primitive building blocks, today's Very Large Scale Integration (VLSI) chips commonly contain millions of transistors.

Over the last 15 years, Complementary Metal Oxide Semiconductor (CMOS) integrated technology has come to dominate analog, digital, and mixed-signal electronic design. The building blocks of this technology are Metal Oxide Semiconductor Field Effect Transistors (MOSFETS). Depending on the doping of the semiconductors from which they are made, MOSFETs are characterized as either positive (PMOS) or negative (NMOS) transistors. CMOS uses PMOS and NMOS transistors in a complementary fashion to implement common circuit functions.

While CMOS circuits have historically shown lower performance than alternative technologies, recent improvements have yielded performance that is acceptable except in very extreme cases. In these cases, the designer has a choice of traditional bipolar transistors, Bi-CMOS (a hybrid of the two technologies), or compound semiconductor technologies such as gallium arsenide. However, these technologies are more expensive to manufacture and exhibit much higher power consumption. For these reasons, most mainstream designs are now done with CMOS.

At the same time, changing design practices have revolutionized the way that electronic system design is performed. At the board level, small-scale integrated circuits such as operational amplifiers have replaced discrete components because of their reduced cost. With increasing frequency these board-level designs are themselves replaced by very complex application-specific parts that are designed especially for mass-produced applications. Often these components are designed as intellectual property *cores* which are reused on several different chips, especially large chips that incorporate an entire *System on a Chip*.

One might expect that this trend would remove many engineers from the process of transistor-level design, with only a few large semiconductor companies providing pre-designed and pre-manufactured components. However, the emergence of *silicon foundries* has made chip-level design more accessible to engineers than ever before. These foundries act as manufacturing services for a large number of customers, making it possible for even small companies to create custom chips without the expense of a fabrication facility. Most of these foundries support only CMOS, reinforcing its dominance in electronic design.

We believe that electronics courses in undergraduate Electrical and Computer Engineering curricula must adapt to this new landscape. Specifically, these courses must follow the transition from bipolar to CMOS devices and provide exposure to transistor-level design at the chip level. To do this, the laboratory component of such a course must provide students with exposure to design at the integrated circuit level as well as with discrete components and high-level building blocks such as operational amplifiers.

This paper describes the integration of these issues into the two-semester junior electronics course sequence at Lafayette College[3]. We rearrange topics from a traditional

electronics sequence to give students a better handle on modern circuit analysis and design techniques. We believe that this scheme gives students a better appreciation of the design issues that they are likely to see in practice.

A key part of this effort is the integration of IC design in the accompanying laboratory. While students continue to use breadboards to build circuits, this experience is augmented with projects that require students to design, simulate, and lay out circuits at the chip level. This experience concludes with a capstone Junior Design Project in which students apply what they have learned in the design, analysis, and layout of a more complex analog or mixed-signal circuit.

The revised course takes advantage of a number of resources that have been used in the past primarily for graduate courses and senior-level undergraduate courses in VLSI Design[4]. The MOS Implementation Service (MOSIS)[5] provides the ability to fabricate small chips in a number of design processes, extending the "foundry" model to small-volume prototyping. Public design information provided by MOSIS – layout design rules, circuit simulation models, and electrical parameters – can be used by students with a number of low-cost CAD tools to design real chip layouts. Moreover, through its industry-sponsored Education Program, MOSIS makes chip prototyping available to chip design courses in the US at no cost to the students.

A major difference in our approach is the migration of what was previously advanced elective material[4] into a required junior-level course. This guarantees that all ECE students at Lafayette are exposed to this important material and gives them a better understanding of how electronic design is practiced in industry. Moreover, learning the mechanics of simple layout reinforces their intuitive understanding of transistor operation and circuit design. The material taught in this course also allows senior-level courses involving integrated circuit design to start at a higher level and cover more advanced material[4]. Finally, the experience with analog and mixed-signal design offered by this sequence gives students a competitive edge in their search for employment or graduate study.

This paper is organized as follows: Section 2 provides an overview of the revised courses and the material covered in the lecture part of the course. Section 3 discusses the laboratory experiments performed in the courses, while Section 4 discusses the junior capstone design project. Section 5 concludes the paper.

2. Course Sequence Organization

Tables 1 and 2 show the topics covered in the first and second semesters of the new course sequence and compare these topics to the topics in a "standard" electronics course sequence. Most of these changes are incremental, with small reductions in coverage of older topics to make room for the new topics on CMOS processing, layout, and circuit design. The remainder of this section discusses each topic in more detail.

2.1 Amplifier Models and Principles

To prepare students for the design of complex integrated devices in the later stages of the course, we begin by introducing modeling of amplifier blocks (including voltage-mode, transconductance, and transresistance models). The notion of a unilateral model is introduced, and we emphasize the importance of allowing amplifier models to be independent of source and load resistors. In turn, we follow this material with an overall model of cascaded single amplifier blocks.

Topic	Weeks	Comparision (to Standard Sequence)
1. Amplifier Models and Principles	2	Same
2. Diode Devices and Circuits	2	Slight Reduction
3. Single Transistor Bipolar Amplifiers	3	Same
4. Single Transistor MOSFET Circuits	3	Slight Increase
5. Digital CMOS Gates	3	Expanded
6A. Bipolar Differential Pairs & Op Amps	1	Reduced

Table 1 – Lecture Topics in Semester 1

Topic	Weeks	Comparision (to Standard Sequence)
6B. MOSFET Differential Pairs & Op Amps	3	Expanded
7. Frequency Response – Part I	2	2 non-consecutive sections
8. Feedback Amplifiers – Part I (Introduction and Compensation Methods)	2	2 non-consecutive sections
9. CMOS Op Amp: Specification, Analysis, & Design	2	
10. Feedback Amplifiers – Part II	2	
11. Frequency Response – Part II	1	
12. Designing Circuits with Operational Amplifiers	2	Typically follows Topic 1

Table 2 – Lecture Topics in Semester 2

2.2 Operational Amplifiers

The analysis of operational amplifiers including amplifier imperfections is often presented at this point in the course. Instead, we prefer to delay this topic until the students are familiar with building blocks of the operational amplifier, such as the differential pair. Concepts such as input impedance, input bias current, input offset current, voltage offset, and common-mode rejection are easier to grasp when students understand the circuit block from which these specifications originate. The origin of dynamic specification, such as unit-gain frequency or slew rate, can only be understood from the operation of electronic circuits at high frequencies, and the theory and methods of compensation in an operational amplifier to achieve closed-loop stability.

2.3 Diode Devices and Circuits

We retain the standard course flow for this topic, but abbreviate the standard discussion of the device physics of the forward-biased semiconductor diode.

2.4 Single Transistor Bipolar Amplifiers

We follow the normal course sequence but give the device physics of the bipolar transistor abbreviated coverage to save time for other material. Bipolar devices are taught first because useful discrete circuits are more readily constructed in the lab. We emphasize small-signal modeling concepts while stressing the relationships between small-signal models and the large-signal device equations. Follow-through of concepts from the amplifier models section is apparent in this part of the course. Both the common-source and common-base three-component models are developed independent of source and load. Sources and loads are purposely divorced from the analysis of these circuits. This permits students to quickly progress to the analysis and design of cascaded bipolar transistor stages. Students' abilities to understand, analyze, design and model multi-transistor circuits are key to their success in the course's capstone design project.

We stress an understanding of the ranges which the input and output voltages can span while a given device model remains valid. This supports the analysis of circuit simulations that the students must undertake in the capstone design project. Often first-cut designs of these circuits result in a device that is unexpectedly biased in the cutoff and saturation regions. Accordingly, students must have an appreciation of the relationship of the circuit's bias conditions when the AC gains of the circuits are unexpectedly low.

We conclude this section with emitter-followers. The analysis of this circuit must be modified since an emitter-follower cannot be represented as a unilateral model that is independent of their source and load impedance.

2.5 Single Transistor MOSFET Circuits

We develop MOSFET device physics in slightly more depth than bipolar devices. The development of the small-signal models of the MOSFET closely follows the development the bipolar signal model. It is important that students become comfortable with the small-signal modeling concept as a model of an active device operation at a given bias point. The limits under which the small-signal model remains valid as bias conditions change is emphasized. When using circuit simulation tools such as SPICE, it is helpful for students to understand where to find the small signal and DC parameter lists for each transistor, and to understand how the list is calculated. Once students can read this data block format of the SPICE printout, they are able to visualize how well a “paper” small-signal analysis of a given transistor circuit corresponds to the circuit's operation as predicted by circuit simulation using small-signal SPICE transistor models.

As we progress towards common-source and common-gate amplifiers, we encounter a problem with biasing the MOSFET. Some texts adopt four-resistor biasing[6] that mimics

the bipolar device. However, this approach is rarely used in practice: it is not effective in producing stable operating currents and it degrades input impedance in the case of common source amplifiers. The more common method of biasing a MOSFET using current sources is introduced in some texts[7]. Unfortunately, introducing techniques requiring current-mirror biasing circuits as active loads this early in course confuses many students.

In our opinion, it is best to bias single-stage MOSFET amplifiers with a voltage source between the gate and source, and address the issue of biasing with current sources later. Care must be taken, however, to reinforce with students that it is not possible to practically bias a MOSFET circuit with a voltage source since any change in the device's parameters or operating conditions can cause the MOSFET to migrate from the active region.

As in the bipolar lecture section, we stress the development of unilateral models of single-stage MOSFET amplifiers. The limited range of biasing conditions under which the amplifier model remains valid is a significant part of the lecture.

We briefly discuss source-followers. These are difficult to use in IC designs with power supplies below five volts. We explain the rationale for the transconductance (gm) of the device in the source- follower stage to be higher than the reciprocal of the load impedance if the gain of the stage is to approach one. We draw a contrast between calculating the bias current of the follower through small-signal analysis and the large-signal bias current calculations that arise from output swing requirements into low impedance loads.

2.6 Digital CMOS Gates

This topic is typically covered in detail in a senior elective course in VLSI circuits and systems. We choose to include coverage of this topic in the junior electronics sequence for a number of reasons. First of all, students who choose not to study electronics further after the junior year would otherwise not be exposed to this important topic. Second, simple CMOS gates provide a good starting point for laboratory experience in CMOS layout and post-layout simulation. Third, they are useful in many of the capstone projects later in the course.

Coverage of bipolar logic families is excluded, either because they are obsolete (e.g., Transistor-Transistor Logic), or because their advanced operation (e.g., Emitter-Coupled Logic) is better suited for coverage in later courses.

After a brief introduction to logic functions implemented by switches, we present the elements of CMOS process technology and a CMOS layout flow. We next discuss layout techniques for simple logic gates and simple design rules. We use a supplemental text authored by Saint[8] to help students comprehend this material. Coverage of the topic in standard electronics texts is insufficient to allow students to quickly grasp the concepts of IC layout and apply these concepts to layout tasks performed in laboratory exercises.

The transfer curve of a CMOS inverter is derived in detail. This motivates the use of large-signal MOS device equations in multiple regions of operation. As the inverter transitions from an output logic-high to an output logic-low, the pull-up and pull-down devices move through the three regions of MOSFET operation (cutoff, saturation, and non-saturation). Students who absorb this relatively complex analysis are well prepared to handle circuits in the capstone design project that require similar analysis. A discussion of noise margins and device sizes follows directly from the lecture on the inverter transfer characteristic.

We present a thorough analysis of the switching time of a CMOS gate. Many texts use an approximate method that models the MOSFET as a resistor. We have found the accurate derivation, in which the MOSFET transitions from the saturation to non-saturation region as the output transition occurs, can be presented in nearly the same amount of time. These switching time calculations are the first time the students deal with reactive elements in this course. This topic allows them to connect the material they learned in circuits with concepts that are familiar to them such as microprocessor clocking speeds. A brief analysis of power consumption in CMOS inverters follows.

A discussion of pass-transistor logic and CMOS complementary switches builds on the material from the lectures that covered common-source amplifiers and source-followers. The NMOS pass-transistor is shown to act as a common-source amplifier as a pull-down device and a source-follower as a pull-up device. The inability of NMOS devices to pull-up to the supply rail is then readily understood. The complementary nature of the PMOS pass transistor follows naturally from this analysis.

2.7 Differential Pairs and Active Loads

Most texts start coverage of differential pairs with bipolar devices. Skipping these sections and moving directly to MOSFETs is confusing for students since terminology and analysis techniques are only presented in the preliminary sections on bipolar devices. For this reason, we follow the text and start with bipolar devices. We do not veer from the standard approach for teaching bipolar, which includes presentations on current sources and mirrors, active loads, and the analysis of differential pairs using the half-circuit analysis concept.

While simple complete bipolar operational amplifiers may be covered briefly, the design of the complete 741 bipolar op amp is not. Although this operational amplifier is widely used, its analysis is time consuming, its input stage is unusual (as it was designed for a a now-obsolete bipolar process), and, as explained above, it is unlikely that students would be faced with the design of such circuits. Despite this, many textbooks[7] cover the 741 in detail.

Lectures on CMOS current mirrors, differential pairs, and active loads follow in the same manner as the bipolar devices, and can be accomplished with most textbooks. The unilateral model of the common-source amplifier with active load is developed. The

dependence of the gain of the circuit on bias current is derived. We also highlight the ranges in which the input and output signals can move while the small-signal amplifier model remains valid.

Some textbooks do not have an accessible derivation of a CMOS differential pair with an active current-mirror load. In our development students understand how to construct the unilateral model of differential gain of this circuit. They also understand why the common mode gain is zero for matched devices. Nor do most textbooks clearly present the calculation of common- mode range limitations of the differential pair. This is an essential operational amplifier specification and one that will be needed for the operational amplifier design procedure discussed below.

Unfortunately, most texts lack reasonable coverage of CMOS operational amplifier analysis. We have found two texts[6,9] that offer good coverage of the topic including a comprehensive discussion of the circuit's voltage and current bias levels and the small-signal gain analysis of a simple two-stage CMOS operational amplifier. The Hambley text[6] is particularly useful since the development of the CMOS operational amplifier is in the same chapter that introduces differential pairs and current-mirror biasing.

2.8 Frequency Response

Students at Lafayette enter the electronics sequence with a single semester of circuit analysis. Accordingly, we start at “square one” with respect to steady-state frequency domain analysis of circuits with reactive components in symbolic form. Moreover, students have limited experience with drawing Bode plots. This material must be reviewed before moving to topics related to frequency response. The concept of the right-half plane zero is introduced, as it will soon manifest itself in the frequency response of a common-source amplifier, and will play a key role in stabilizing an amplifier using a common-source stage.

With the fundamentals in place, students can proceed to the frequency response of the common-source amplifier. A complete derivation is undertaken including load capacitance. These equations, and their simplifications using dominant pole analysis, will be identical to the equations that are presented when Miller's compensation of operational amplifiers is discussed in the next lecture block.

Miller's theorem is introduced, but with a great deal of care. Many students (and some textbooks) misuse this theorem and try to adapt it for calculating the frequency response or output impedance of a gain stage. In both instances, the results are inaccurate.

In a traditional course flow, lectures would next shift to the high-frequency response of the common-emitter stage, the differential and common-mode high-frequency response of differential pairs, the high-frequency response of the cascode stage, and the high-frequency response of the source- and emitter-follower. We push these topics towards the end of the course, and instead consider compensation techniques for operational amplifiers. The timetable of the capstone design project can influence the lecture

sequence, and this is one example. Students will be actively designing operational amplifiers in their final projects, and the start of this project closely corresponds to the point in the lecture when high-frequency response of source-followers is discussed.

2.9 Feedback and Compensation

Typically, four types of feedback in electronic systems are presented. Related topics include the identification of the type of feedback being used for a circuit schematic, the use of feedback for gain stabilization and reduction of nonlinear distortion, and feedback effects on input and output impedance of a system. We postpone this lecture to permit a discussion of frequency compensation of operational amplifiers.

Accordingly, we analyze the effects of feedback on single-pole and two-pole amplifiers. Root locus for a two-stage feedback amplifier is presented, as is the transient response of the feedback amplifier. This leads to a discussion of the gain and phase margin of a feedback system, and dominant pole compensation by both the addition of a new pole into the amplifier and by moving an existing pole in the amplifier to become a dominant pole. Miller's compensation and pole splitting in a two-stage CMOS operational amplifier then follow this discussion. At this point, the concepts of slew rate and full-power bandwidth can be introduced. The tradeoffs between slew rate and the small-signal gain bandwidth of an operational amplifier when designing for good phase margins are presented.

With the aforementioned fundamentals in hand, students are well-positioned to design CMOS operational amplifiers. The systematic design procedure from a set of specifications, as outlined by Allen[10], is followed. Each equation that is used in the procedure is derived and discussed to make the evolution of the process clear to the student. The procedure is for a simple Miller-compensated operational amplifier. No additional circuitry is introduced to cancel the right-half plane zero in the transfer function. The design procedure includes consideration of placement the zero to a frequency where the zero does not markedly degrade phase margin.

Students design an operational amplifier to a given set of specifications and simulate the resultant amplifier with Spice for homework. Some students develop a spreadsheet for the design procedure. This is helpful because it illustrates that the operational amplifier is realizable for a given process technology within a limited range of specifications. Students can observe how certain specifications, such as slew rate, gain bandwidth product, and power consumption can be traded-off for a given phase margin. The specifications list used in the design procedure covers the majority of key design parameters for an operational amplifier including those cited above and open-loop gain, common-mode range, and linear output swing range.

Once the operational amplifier design section is completed, it may be desirable to continue with related topics, such as the performance difference between MOS and bipolar operational amplifiers. The origin of static DC errors, such as output voltage offset, input bias current, and input offset current may be introduced at this point. Topics

on different operational amplifier topologies, such as single gain stage op amps, op amps that use telescoping and folded cascode gain stages, and op amps with circuits to enhance slew rate can be presented. The presentation of class A and class AB output stages for driving low impedance loads is also a relevant topic at this point in the course.

Unfortunately, we reach the conclusion of the design of the two-stage CMOS operational amplifier with only four weeks left in the course. Since the discussion of the topics listed above would consume most of the remaining time, we have chosen to devote the balance of the semester to frequency response of MOS and bipolar circuits and topics on basic feedback amplifiers. These aforementioned topics are often included in senior / first-year graduate classes on analog electronics. Therefore, interested students will see the material in due course. Students who conclude their study of electronics with this first year sequence are better served by the choice to transition to topics away from operational amplifier design.

The instructor may also opt to review the design of circuits with operational amplifiers and/or present new circuits such as the Schmitt trigger and the instrumentation amplifier[11]. With their new-found understanding of operational amplifier fundamentals and limitations on device performance, students are better prepared to absorb this material at the end of the course.

3. Laboratory Exercises

Tables 3 and 4 summarize the laboratory exercises in the revised electronics sequence. Early exercises on diodes, simple bipolar, and MOSFET transistor amplifiers follow experiments traditionally used in an introductory electronics class[12]. In addition, SPICE assignments are taken from a standard text on PSpice (a commercial version of the SPICE circuit simulator)[13].

Topic	Weeks
1. Diode Circuits Lab	2
2. DC and Small-Signal Characteristics of Bipolar Amplifier	2
3. Transistor Bipolar Amplifiers with Bias Stability	1
4. Transisotr Bipolar Amplifier Design	2
5. DC and small-signal characteristics of MOSFET operation	2
6. Device Parameter Modeling of MOSFET Transistor	1
7. CMOS Inverter and Gates Transfer Function	2
8. Introduction to Layout CAD Tools	2

Table 3 – Laboratory Sequence for Semester 1

Topic	Weeks
9. Layout of Logic Gates and Differential Pairs	2
10. Design of Op Amps using CD4007 Building Blocks	3
11. Layout of a CMOS Op Amp and Parameter Extraction	1
12. Design Project (see Table 5)	7

13. Project Presentation	1

Table 4 – Laboratory Sequence for Semester 2

Students are next required to design a bipolar amplifier with no global feedback loop to specifications, including 1) requirements for power consumption, 2) a maximum and minimum range of temperature under which the circuit must remain functional, 3) a minimum output voltage swing that the circuit can produce for a specified distortion level and load impedance. The design usually requires two or three transistors. Students often have difficulty getting their arms around the design process when faced with a blank sheet of paper. This lab gives them experience in the design process and helps build confidence for the more challenging projects that follow.

Lab experiments involving MOSFETs include the characterization of the NMOS and PMOS devices on a CD4007 device – an integrated circuit package that contains several unconnected transistors that can be used as discrete components. Students measure common characteristics of these transistors, including threshold voltage VT, gain factor Beta, channel-length modulation factor Lambda, and sub-threshold parameters. These parameters are related to Spice parameters in the Level 1 transistor model, allowing students to see the origin of the parameters.

Students also use the transistors in the CD4007 device to construct and characterize the transfer characteristics of the three most common CMOS logic gates: the inverter, the NAND gate, and the NOR gate. They compare their measurements with the analytical model developed in the lectures using the device parameters that they extracted in the prior lab. In addition, they compare their analytical and empirical work with Spice runs of the digital gates using a Spice model that the students develop from the device parameters extracted in the prior lab.

The next three labs explore the layout of simple CMOS digital logic gates (inverter, NAND gate, and NOR gate) and a differential pair with active load and current-mirror to bias the differential pair tail.

This requires the use of a layout editor, circuit extractor, and circuit simulator to verify the proper operation of these gates. We use the Berkeley Magic layout editor[14], which is easy to learn, freely available, and has several useful features, including interactive design rule checking and built-in circuit extraction.

Layout is done using MOSIS scaleable CMOS design rules and the Advanced Microsystems Inc. 1.5µm nwell process, which supports analog features such as dual polysilicon capacitors which are useful in later projects. While not very aggressive by current standards, this technology is an excellent pedagogical tool for teaching layout. Process information and Spice transistor models for this process are publicly available on the MOSIS website; this information is proprietary in more aggressive processes.

Circuit simulation of extracted layouts is performed using Pspice[13], which is also used in earlier labs to simulate discrete-component circuits. However, while previous

experiments used graphical entry of schematic diagrams for input, these experiments use netlists extracted from actual layouts. These are generated from Magic using the built-in extraction capability (some slight customization is required to include the proper device models and generate input files in a format acceptable to PSpice).

Working effectively with extracted netlist files requires that students learn to read and understand the "Spice Deck" file format. At this time they are given a brief introduction to the nature of parasitic capacitances and how these can affect circuit performance, since these are included in the extracted netlist. In addition, they learn to add power supplies, AC and transient sources, and external components such as bias transistors. Once the simulation is set up properly, they can use the built in plotting tool they have used in previous labs to view the simulation output.

After these layout and simulation exercises, students return to the lab bench to build a two gain stage operational amplifier using the CD 4007 devices[15]. Students must compensate the amplifier with a Miller compensation capacitor. This can confound students, as they have not been introduced to the role of compensation in stabilizing the amplifier in a closed-loop feedback configuration. We explain the purpose of the capacitor, and stress that it will become clearer later in the course

Students measure the gain of both the differential stage and the common-source stages of their operational amplifier. These measurements are difficult to perform on the individual building blocks because of the issue of establishing the correct DC bias conditions without global feedback, as discussed above. It would be desirable to schedule lab experiments that cover common-source amplifiers with active loads concurrently with the lecture on bias network (e.g., a replica bias stage needed to establish a midpoint DC bias[15]). However, such approaches are complex to describe, consuming valuable class time on bias schemes that are rarely used in practice. It is thus preferable to wait and perform the experiments on the complete operational amplifier when students are conversant with DC biasing of internal operational amplifier stages by closed-loop feedback. This material is developed within the lectures on CMOS operational amplifier design.

The formal lab section concludes when students lay out a version of their operational amplifier (using their differential pair layout as part of the larger layout) and run the post-layout simulation on PSpice. Students perform operating-point analysis, AC, and transient analysis using the netlist. In this manner, they familiarize themselves with the complete design flow needed for the extended design project.

4. The Capstone Design Project

The extended project takes place during the second half of the second semester course. Table 5 summarizes the timetable for this project. Students work in teams of two or three and pick projects under the guidance of the lab instructor.

We encourage our students to canvass the IEEE search engine to locate interesting and promising circuit topologies as project candidates. While students may not be prepared to assimilate many of the papers that they unearth, they often find accessible journal articles written by first-year graduate students or papers that describe subblocks of a large- scale system. For example a paper on the design of a clocking system for a large-scale digital system may describe blocks such as phase detectors, charge pumps, and VCOs at a level that can be understood by the students. Advanced texts[10,16,17] on analog electronics can also be a fertile source for circuits. However, we caution that these texts may present obstacles to the student since the circuits that make for quality projects could be presented well into the text. If the text is written with the expectation that the contents are to be read sequentially, then juniors will lack the necessary preliminaries and have difficulty comprehending the material.

Topic	Weeks
Topic Selection and Preparation of Project Proposal	1
Circuit Design and SPICE Simulation	3.5
Layout	1.5
Post-Layout Verification and Circuit Revision	1

Table 5 – Design Project Timetable

Once a topic is selected, the lab instructor assists student teams in focusing their efforts and refining their designs. During the design process, students gain an appreciation of circuit operation -- for example, they discover what factors influence the oscillation frequency of a current-controlled oscillator. Students must ensure that their devices work in the desired operating regions for all current and voltage swings that the circuit will see under normal operation. For example, a team designing an operational amplifier must check that all devices in the differential pair remain active for the full common-mode input range specified for the circuit.

Once plausible designs are outlined, teams use Spice to check them. Circuits are entered using the PSpice schematic editor, using parameterized schematic symbols to describe the MOS transistors.

The instructor should take care that students have an understanding of the operation of their circuits to enforce that this is a verification phase of the project, not a design phase. When running Spice, students verify that the DC bias currents and voltages match their hand calculations. We also encourage students to check the values of the small-signal operating condition of the transistors given by Spice relative to their computational analysis. In so doing, it becomes readily apparent if devices are correctly biased.

Once teams have refined a design using analytics and additional Spice simulations so that it operates under DC conditions, the group proceeds to the requisite AC and transient runs. PSpice is likely to come up in the meta-stable state of an oscillator. As a consequence, we often must include a start-up circuit to coax the primary circuit into one of its normal operating states. It is incumbent upon the lab instructor to quickly identify

circuits where these circumstances have occurred; otherwise, students become frustrated with their circuit's inability to oscillate.

Functional designs are next simulated over temperature and supply voltage variations to examine their robustness. As much as we would like to use case file variations and device mismatch file, given their efficacy in shaping robust designs, we elect not to do so since this step can significantly lengthen the project's timetable. It is left to the instructor's design experience to ensure that student designs are inherently process insensitive.

During the Spice phase of the project cycle, students often show a lack of patience and have a tendency to tune out when the instructor cannot quickly identify the cause of a circuit failure. This frustration is compounded when the instructor discovers that a team's topology (taken from an IEEE paper or textbook) is not functional and needs to be modified or replaced. Reasons for this can range from a circuit having been simplified for presentation in journal paper or text to the possibility that the authors have not disclosed whether added circuitry is needed to enable robust. Other problems can occur when a circuit does not translate well to the MOS process being used by the students.

Frustration with the iterative design process (students tend to prefer linear processes) can also be magnified when an instructor changes a circuit to solve a problem resulting from second-order effects with which the students are not familiar. As one of the objectives of the project is to give students exposure to real-world design issues, we feel these bumps-in-the-road are an essential learning tool -- they are part and parcel of any project life cycle when circuits are not pre-chosen or pre-tested, and they require nimble reactions and creative thinking on the part of the team to constructively deal with them. Some students come to appreciate this part of the design process, while others have suggested to us that the project should be more structured with known outcomes. We resist the latter because it would be to the students' disadvantage were we to sanitize the process for them.

Once a design works properly on Spice, the team starts circuit layout. Because of the limited time for the project, it is critical that the circuit design in Spice be robust at the start of this step since we do not want to modify the circuit post-layout. The instructor carefully guided layout since students have limited experience with this task. Layout techniques must ensure, for example, 1) proper matching of current mirrors and differential pairs 2) high-impedance nodes are not excessively loaded with parasitics and/or brought near lines that could cause stability or crosstalk problems, and 3) proper use of multiple-striped devices. The instructor must also raise issues of adequate power supply routing. Frustration can set in here as well when the team is asked to re-layout parts of the circuit to address issues of which they have not been made aware until the instructor discovers these problems in the layout.

All designs are converted to Spice files using the Magic extraction tool as outlined above. Students must re-simulate the extracted design on Spice before it can be sent for fabrication. The instructor's input is often is needed at this stage to rid Spice decks of any

parasitic nodes that may be floating or otherwise incorrectly extracted. In addition, the student or instructor must use the Spice netlist as a method to ensure that the layout matches the circuit (Magic lacks a direct LVS tool). Since the netlist becomes the debugging tool, all internal nodes of the circuit must have clear net names. Nodes not connected to power supplies, floating nodes, and shorts are more easily identified under these circumstances. Students need to check that they have not tied a well or substrate to the wrong power supply. Optionally, Magic can be set to include wells and substrates as conductive layers. Using this option leaves open the possibility that either a section of the circuit may be powered off a well or a substrate contact will not be detected. Circuits powered in such a manner can readily latch up.

A sampling of projects developed last semester and submitted for fabrication are listed below:

- Analog Multiplier using MOSFETs in the Triode Region
- Charge Pump for an IC Phase-Locked Loop (PLL)
- Low Voltage CMOS Bootstrapped Switch for a Sample-and-Hold Circuit
- Operational Amplifier with Cascode Output Stage
- Operational Amplifier with Class AB Output Stage
- Operational Amplifier with Constant gm Biasing
- High-Speed CMOS Phase Detector with Deadband Suppression for an IC PLL
- Ring-Oscillator based Voltage-Controlled Oscillator Design for an IC PLL

Note that many of these projects have enabled our students to explore topics in electronics that could not possibly be covered in an introductory class. Some students tackled advanced topic in operational amplifiers, some examined the design of relaxation oscillators, and others took up the challenge of nonlinear electronics. This wide range of topics places heavy demands on the instructor since the advanced material that each group will need must be taught to them individually. While it is hoped that the groups chop much of the wood themselves, the reality is that a large time commitment will be required for the average group to make certain that the students are grounded in proper theory, that they are on pace towards making acceptable progress, and that the designs will be robust enough to work as individual samples when produced by the MOSIS foundry.

At the conclusion of the course, groups write a design memo that covers an explanation of the circuit's operation, hand calculations used in the design process, Spice runs used to verify device performance, a discussion of the layout of the circuit, and a discussion of any performance degradation that occurs after post-layout Spice simulation. An oral PowerPoint presentation and defense is also required and members of the faculty are invited to participate.

Figure 1 shows the Magic layout of a Charge Pump designed by a team of three students at Lafayette during the Spring 2002 semester. This Phase-Locked Loop building block converts a phase-error input into a voltage level that drives a voltage-controlled oscillator in the proper direction (up or down) to lock the PLL to an input frequency. This design

makes use of operational amplifier layouts designed by a second team of three students. It has been submitted for fabrication by MOSIS and will be tested during the Spring 2003 semester.

5. Conclusion

This paper has presented a revised curriculum for a two-semester electronics sequence that better parallels the state of modern design practice. This curriculum emphasizes IC design with MOS transistors as the main vehicle for modern electronic systems design. Analysis of the circuit aspects of CMOS logic motivates first-principles concepts in solid-state device operation and allows an easy transition into basic amplifier analysis techniques. With this background, students can experiment with leading methods of modern solid-state circuit design in their capstone design projects. This has been accomplished by the introduction new lecture topics, the addition of new laboratory experiments that integrate CAD tools, and the elimination of material no longer core to the discipline at the undergraduate level.

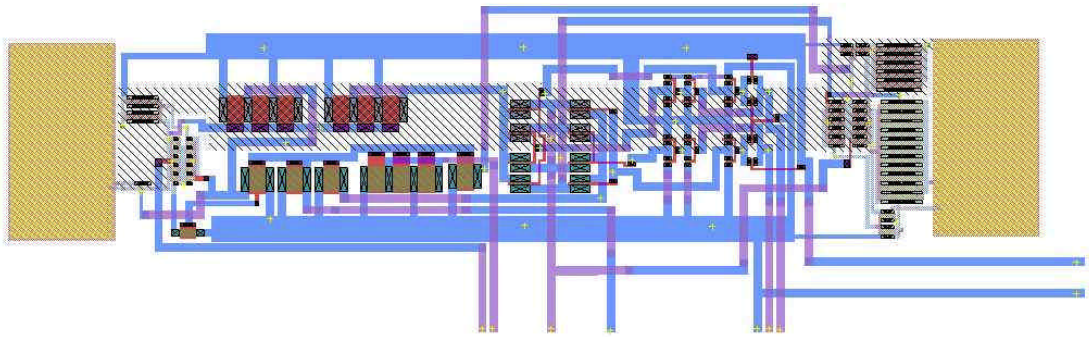

Figure 1 – Example Project - Charge Pump

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