Applying the Flipped Classroom Pedagogy in a Digital Design Course

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Abstract

The goal of this paper is to describe the motivation, methodology and results of converting several modules in a Digital Design course to a "flipped classroom". The course introduces students to VHDL Hardware Description Language as the design entry method for digital circuits and to Field Programmable Gate Arrays (FPGA) platforms for the implementation of the digital circuits. The students enrolled in this course have a large range of skills in term of experience with laboratory equipment, computer-based-tools and programming. The paper will summarize the process of implementing the flipped classroom pedagogy in the digital design course and will present challenges, lessons learned and assessment data.

I. Introduction

In traditional approaches to teaching engineering classes, the instructor plays the role of information conveyor, while the students assume a receiver role with primary responsibilities of listening and note taking. Research into how students learn suggests that students need to be more actively engaged with the course material to maximize their understanding[1]. The fundamental idea behind flipping the classroom is that more classroom time can be dedicated to active learning where the instructor can provide immediate feedback and assistance. Students can collaborate on in-class problems and submit their work for review and discussions[1-2]. In this model, lecture content is removed from the classroom to allow time for active learning, and the content that was removed is delivered to students via on-line video. Research has supported that active learning strategies result in higher student engagement and greater learning gains as compared to traditional instructor-centered methods such as lecture[1,3].

This paper presents the results of converting several modules in an undergraduate engineering course in a "flipped classroom". The target course is EET 316 - Digital Design. This course is a four credit junior level course (theory-3 credits, lab-1 credit) for electrical and computer engineering technology majors at Farmingdale State College-State University of New York. The course introduces students to VHDL Hardware Description Language as the design entry method for digital circuits and to Field Programmable Gate Arrays (FPGA) platforms for the implementation of the circuits, using Xilinx design tools.

The students enrolled in this course have a large range of skills in term of experience with laboratory equipment, computer-based-tools, programming, approximately 40-50 % of the class being transfer students from community colleges. To address this problem, the author of this paper decided to convert three major modules of the course to a "flipped classroom". The following modules of the Digital Design course were converted to a "flipped classroom": *Description and functional verification of combinational circuits using VHDL; Description and functional verification of sequential circuits using VHDL; Description and functional verification of Finite State Machine using VHDL.*

The remainder of this paper is organized as follow: Section II presents similar work. Section III presents the characteristics of student population at Farmingdale State College. Section IV presents the Digital Design course. Section V presents the methodology. Section VI presents results. Section VII concludes the paper.

II. Similar Work

Being considered one of the high impact active learning practices, the flipping classroom pedagogy is routinely implemented in undergraduate and graduate level courses and in all STEM fields. While there is an overwhelming evidence provided by literature for the added value of the flipping classroom concept, the majority of the surveyed papers presents examples of courses "completely flipped" not only specific modules. Also the majority of the papers presents "flipped courses" for four years engineering programs such as electrical and computer engineering, chemical engineering, architectural engineering, etc. Only few papers present flipped courses for engineering technology programs, to the best knowledge of the author of this paper.

Reference[4] uses "focus group interviews and the student perspective in order to investigate student perceptions of flipped classroom in engineering education in many courses and subjects. The perceived advantages, strengths, drawbacks, or difficulties, and students' views on learning with flipped classroom were investigated". Reference[5] presents how a flipped classroom technique was incorporated into a three-credit electrical engineering course. The paper discusses "student survey results, and describes plans to improve the delivery of this and similar courses". Reference[6] focuses on the implementation, development, documentation, analysis, and assessment of the flipped classroom methodology for a pilot group of chemical and materials engineering undergraduate students at the University of Barcelona. "Results show that this technique promotes self-learning, autonomy, time management as well as an increase in the effectiveness of classroom hours". Reference[7] discusses the flipping classroom model in an undergraduate architectural engineering class. It is interesting to note that "students' feedback suggests that while the active learning and additional project time available in class improved their understanding, they would prefer that only about half the classes be flipped and some use of traditional lectures should be maintained". Reference[8] presents the lessons learned from flipping the classroom of an entry-level graduate course on digital hardware design. The course cover hardware description languages (HDLs) and requires students to successfully design, simulate, synthesize, and verify digital circuits using hands-on projects and in-class activities. It is important to note that the authors of this papers notice that "typically, students struggle with provided in-class activities, assignments, and projects in any digital hardware design class". The authors conclude that "from an instructional perspective, regardless of drawbacks, the new active-learning environment and teaching techniques allowed for the instructor to reinforce and delve deeper into course content while allowing students to work efficiently with new material". Reference[9] discusses the implementation of the flipped classroom method in a Fluid Mechanics course in an Engineering Technology program. "A survey was distributed to the students at the end of the course as a post-class activity, concluding the implementation considered in the study. The results of the survey showed that the students were satisfied with the teaching method and found it important in their learning process".

III. Characteristics of Students Population at Farmingdale State College

The flipped classroom pedagogy presented in this paper was designed for students enrolled in the Electrical and Computer Engineering Technology programs at Farmingdale State College. The Department of Electrical and Computer Engineering Technology attracts a large number of transfer students from the community colleges located in Long Island, NY. Students enrolled in these programs have a large range of skills and aptitudes, in terms of math, sciences, experience with laboratory test equipment, computer-based-tools, programming.

The general characteristics of student population at Farmingdale State College was taken into consideration also. A study of student population at Farmingdale State College shows the following: over 90 % of the students are commuting on daily basis from the greater New York metropolitan area and they hold full time jobs; around 35% are first-generation college students (e.g., neither parent has earned a 4-year degree); 30% are minority; the student population includes large numbers of "New Americans" (i.e., they or their parents were born outside of the US), coming from extremely diverse educational and cultural backgrounds; many students have considerable financial need (30% receiving Pell grants)[10]. One of the conclusion of the study is: "*to educate today's new undergraduate student effectively, one needs to engage students in active, experiential learning*", which is the main focus of the pedagogy presented in this paper.

IV. Description of the Digital Design Course at Farmingdale State College

The digital design education in the Department of Electrical and Computer Engineering Technology at Farmingdale State College is accomplished by a sequence of three courses: *EET 105-Introduction to Digital Electronics, EET 223-Digital Electronics and EET 316-Digital Design*. Each course is taught by various instructors, both from academia and industry. The first digital course in the sequence, *Introduction to Digital Electronics*, presents fundamental concepts of digital electronics, specifically combinational logic circuits. The second one, *Digital Electronics* reinforces the analysis and design of combinational and introduces sequential logic circuits. The third one, *Digital Design*, introduces students to more advanced concepts in digital design.

EET 316 Digital Design is a four credit junior level course (theory-3 credits, lab-1 credit). The course introduces students to VHDL Hardware Description Language as the design entry method and to Field Programmable Gate Arrays (FPGA) platforms for the implementation of digital circuits, using Xilinx design tools. Computers are used extensively throughout the course, being a design oriented course. The course outline is presented in Appendix 1.

After taking this course, students should be able to: (i) design and analyze combinational and sequential logic circuits; (ii) trace the behavior of digital circuits by completing and analyzing timing diagrams. (iii) Use VHDL and Schematic Capture to design, simulate, and implement digital circuits; (iv) Draw a state diagram and implement solution to a digital design using Finite State Machine based controller.

In the last five academic years, EET 316-Digital Design was updated continuously. The changes were made by the author of this paper, who was appointed course coordinator in the Fall of 2014, in collaboration with an adjunct faculty. Feedback from the Industrial Advisory Board was also considered. The changes are presented in details in reference [11].

The platforms currently used for the lab experiments are Nexys™3, based on XILINX Spartan-6 FPGA chip and manufactured by DigilentInc[12]. The Nexys™3 board is presented in figure 1.

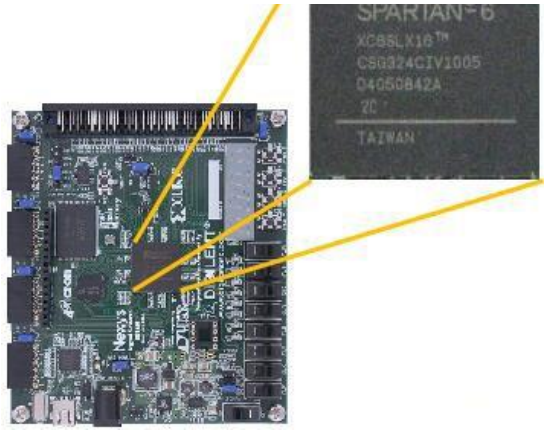

Figure 1. Nexys™3 Spartan-6 FPGA boards

In the academic year 2013-2014, a new lab manual was created, teaching students design entry (Schematics and VHDL), using Xilinx ISE tools and Digilent ADEPT software. The laboratory tutorials were based on materials provided at workshops sponsored by the NSF ATE grant *"DUE- 1003736 – Developing the Digital Technologist for the New Millennium"*. The author of this paper attended the NSF workshops, finding them extremely informative. In the academic year 2014-2015, the lab manual was updated, adding more experiments, but no changes were made to the theory class, compared with the previous academic year. In the academic year 2015-2016**,** changes were made to the course topics, based on instructor's observations and students' strong feedback. The VHDL language was introduced earlier in the semester. New concepts such as clock skew and meta-stability of digital circuits were introduced. In the academic year 2016-2017, the lab manual was updated again, incorporating more complex labs covering VHDL and Functional Verification (Test Benches). The number of Labs covering Schematics was reduced significantly. In the academic year 2017-2018, the Flipped Classroom pedagogy was introduced. In the current academic year, a Project Based Learning pedagogical approach was introduced. Students design, simulate, implement and test a Vending Machine Controller during the last two weeks of the semester.

V. Methodology

For EET 316 Digital Design course, the following topics (modules) were identified to benefit mainly from the flipped classroom pedagogy, starting in the academic year 2017-2018.

- Description and functional verification of combinational circuits using VHDL
- Description and functional verification of sequential circuits using VHDL
- Description and functional verification of Finite State Machine using VHDL

In the traditional Digital Design course, prior to Fall 2017, description and functional verification of digital circuits using VHDL were covered using PowerPoint slides. All the Power slides (lectures) are posted on-line at the beginning of each semester, allowing students to access them before the class (available on Black Board). For the "flipped classroom", the existing Power Point lectures were converted into Panopto video lectures. The intention was to record the PowerPoint slides and on-screen content along with audio of the instructor presenting. The flipped classroom modules were created and were added to the EET 316 course content on Blackboard, as seen in Figure 2.

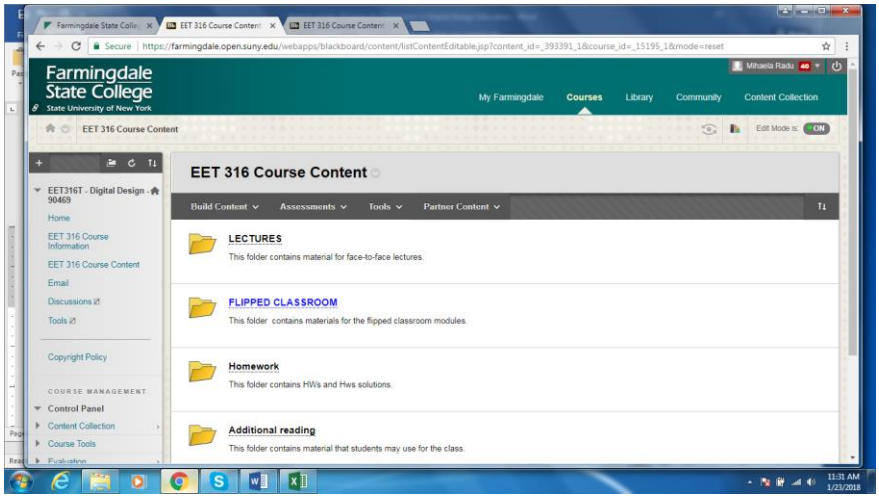

Figure 2-EET 316 Course Content

The flipped classroom folder has three separate modules, one for each topic, as seen in Figure 3.

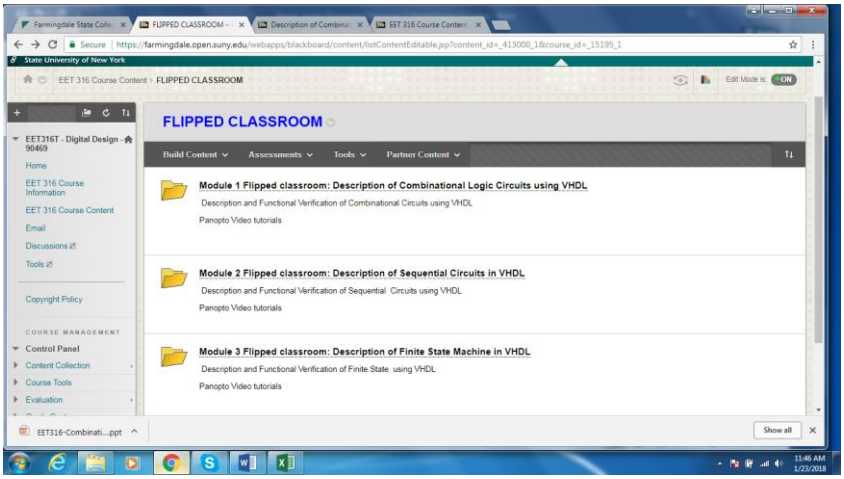

Figure 3-Flipped Classroom Content

Out of class activities: Before the class, students are tasked to listen to the audio tutorials and come prepared to the class. They are provided with adequate information before every flipped classroom module. Figure 4 presents the Panopto tutorial for Description of Combinational Circuits using VHDL.

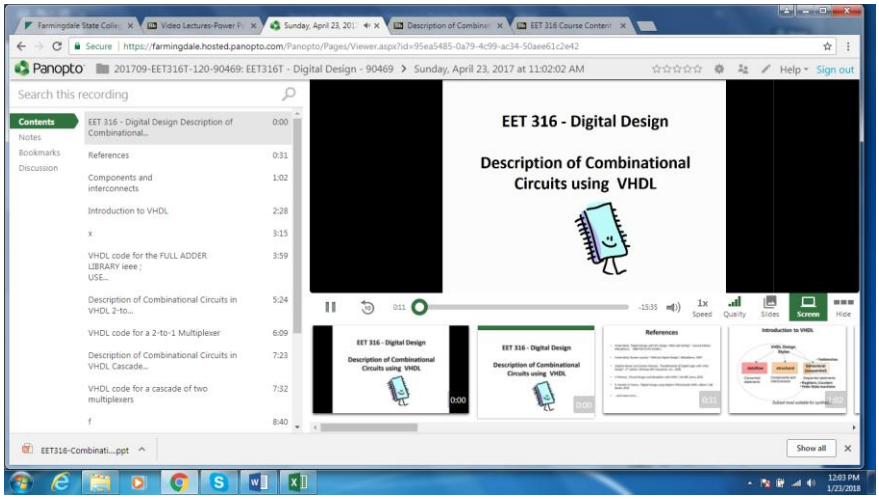

Figure 4-Example of Panopto tutorial –Description of Combinational Circuits using VHDL

In class activities: At the beginning of the class, students receive a quiz regarding the content of the Panopto tutorial. Then the instructor covers briefly the PowerPoints slides, reinforces key concepts and answers students' questions. Figure 5 presents the organization of in class activities for the one of the "flipped" module. It contains quizzes, in class assignment and tutorials for using Xilinx tools. The existing tutorials regarding the use of Xilinx design tool (currently available on Black Board for use in the lab) were updated for use during the theory class.

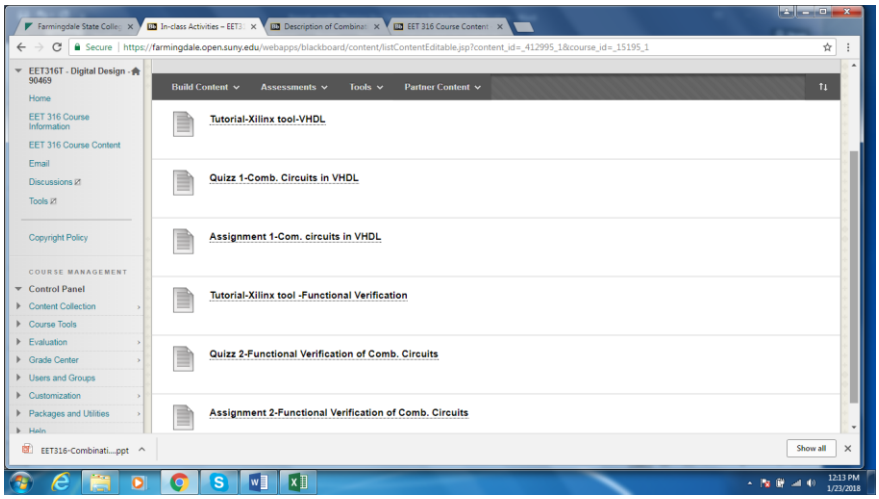

Figure 5-In class activities for a flipped classroom module

During the rest of the class period students engage in activities specific to digital design: *Design Entry* (using VHDL language) and *Design Synthesis* (translation of VHDL into an industry standard format) using Xilinx design tools. Students design digital circuits following examples ("VHDL templates") provided in the notes posted on line (Power Point lectures). They perform also functional verification, by writing and applying test benches to digital circuits and analyzing the resulting waveforms. Writing synthesizable VHDL code following templates and performing functional verification of digital circuits prove sometimes difficult for the students.

By implementing these hands-on activities during the class, students are better prepared for the laboratory experiments and more time can be dedicated to the implementation processes of complex logic circuits: ***Design Implementation*** (translate, map, place and route) and ***Device Programming*** (generate a configuration file and download on the FPGA platform). In the previous traditional approach (no flipped classroom) students performed all the steps of the design during three hours of laboratory, which proved sometimes insufficient. Sometimes students struggle to finish the activities in the allotted time and often wind up missing the main points in an effort to complete the detailed steps for the lab. The planned in-class activities have the potential to improve students' problem solving skills, analytical and critical skills, which are essentials in the engineering field.

VI. Results

First implementation of the "flipped" classroom for EET 316-Digital Design course was in the academic year 2017-2018, Fall semester. Thirty seven students were enrolled in this class, including a large number of transfer students from community college (18 students out of 37 students). The maximum enrollment for this course is 24 students. The room assigned to teach this course is equipped with 25 computers. Students were encouraged to install the Xilinx design tools on their laptops for use in the classroom.

One of the challenge was the size of the class. During in-class activities, the instructor had to help a large number of students in a limited amount of time (debug VHDL code, fix XILINX tools problem, clarify concepts for students, etc.). The limited number of computers in the room was another challenge. On several occasions, students showed willingness to stay after class to finish the in-class assignments, with or without instructor's support. This was a positive note of the course, showing students' dedication and desire to learn.

One of the lessons learned was to take in account the size of the class, and to plan accordingly the in-class assignments. Each assignment should take about 30-40 minutes to complete. The size of the class is currently solved by offering this course twice a year. The in-class assignments were redesigned after the first offering of the course using the "flipped classroom" pedagogy.

Student knowledge was assessed from answers to selected questions of the final exam, related to course objectives. The goal for the course is that 70% of the students to meet the course assessment standard, which states that an overall score over 84 % exceeds the standard, an overall score between 70 % and 84 % meets the standard, an overall score between 60% and 69% approaches the standard, while an overall score below 60 % does not meet the standard, according to ABET accreditation for the EET department.

Note: An IRB (Institutional Review Board) protocol was secured, allowing to present data starting Fall 2017. Only the courses and the associated labs that were taught by the same instructor were considered for the assessment.

Table I presents students' final exam scores in the Fall 2017, Spring 2018 and Fall 2018 semesters and the average scores for two questions. The questions considered for the assessment are related to the analysis and design of Finite State Machine, the most complex topic of the course. Question 5 asks students to draw a state diagram for a Finite State Machine being given specifications

(statements). Question 6 asks students to implement a FSM using VHDL language being given specifications and the state diagram. In both cases students had to identify inputs, outputs, states, transitions, add an asynchronous reset, explain the type of FSM, identify the number of FFs, etc.

TABLE I

Academic Year	Final exam (100 points)	Final exam question 5 (15 points)	Final exam question 6 (15 points)
Fall 2017	76.30	11.24	10.51
Spring 2018	81.04	11.25	11.94
Fall 2018	82.00	11.42	11.54

Fall Semester 2017

Problem 5: Design a FSM state diagram from specifications

Twenty three students out of thirty seven students (62 % of the student population) scored a minimum of 11 points on problem 5 (max 15 points) and fourteen students scored less than 11 points. Seventeen students exceed the standard (min 13 points out of 15), and six students scored 11 and 12 (overall score between 70 % and 84 %) points. The goal for the course that 70% of the students to meet the course assessment standard was not met.

Problem 6: Analysis and Design of FSM using VHDL language

Seventeen students out of 37 students (46 % of the student population) scored a minimum of 11 points on problem 5 (max 15 points) and twenty students scored less than 11 points. Sixteen students exceeds the standard (min 13 points out of 15), one student scored 12 points (overall score between 70 % and 84 %) points. The goal for the course that 70% of the students to meet the course assessment standard was not met.

Spring Semester 2018

Problem 5: Problem 5: Design a FSM state diagram from specifications

Sixteen students out of twenty four students (67 % of the student population) scored a minimum of 11 points on problem 5 (max 15 points) and eight students scored less than 11 points. Thirteen students scored 13 points (exceeds the standard) and three students scored 11 and 12 points (overall score between 70 % and 84 %). The goal for the course that 70% of the students to meet the course assessment standard was approached.

Problem 6: Problem 6: Analysis and Design of FSM using VHDL language

Sixteen students out of twenty four students (71 % of the student population) scored a minimum of 11 points on problem 5 (max 15 points) and seven students scored less than 11 points. Twelve students scored 13 points (over 84 %) and four students scored 11 and 12 points (overall score between 70 % and 84 %) points. The goal for the course that 70% of the students to meet the course assessment standard was met.

Fall semester 2018

Problem 5: Design a FSM state diagram from specifications

Sixteen students out of twenty one students (76 % of the student population) scored a minimum of 11 points on problem 5 (max 15 points) and five students scored less than 11 points. Ten students scored 13 points (exceed the standard) and six students scored 11 and 12 points (overall score between 70 % and 84 %). The goal for the course that 70% of the students to meet the course assessment standard was met.

Problem 6: Analysis and Design of FSM using VHDL language Fourteen students out of o twenty one students (71 % of the student population) scored a minimum of 11 points on problem 6 (max 15 points) and seven students scored less than 11 points. Ten students exceeds the standard (min 13 points out of 15), and four students scored 11 and 12 points. The goal for the course that 70% of the students to meet the course assessment standard was met.

Final exam average score presents a positive trend. It is important to notice that in the Fall 2017, due to the large class, the flipped classroom did not seem to influence exam's scores and the 70 % standard goal was not met. After properly applying the flipped classroom in the spring semester 2018, the exam scores increased and the 70 % standard was met, starting Fall 2018.

VII. Conclusions

The goal of this paper is to describe the motivation, methodology and results of converting several modules in a Digital Design course to a "flipped classroom". The author of this paper is confident that the flipped classroom concept has the potential to improve student's engagement and learning in digital design. Students gain an in-depth knowledge of digital design applied to practical, real-life applications. It has the potential benefit to help students to achieve a higher level of learning in the field of electrical circuits and digital electronics and to develop essential employability skills. By giving students more opportunities to improve their employability skills, they will be better prepared to enter the competitive work force and to compete with graduates from other prestigious universities.

Acknowledgements

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APPENDIX 1

Week by week class outline:

Tentative Course Schedule

This course is an introduction to Digital Design using FPGA (Field Programmable Gate Arrays) and VHDL. Computers are used extensively throughout the course, this being a design oriented course using mainly XILINX Design tools and hardware.

DATE	TOPIC	Course Resources	Student Learning Outcomes	Hws and Out _of_ class_ assign.
1	Introduction to Xilinx FPGA, Hardware Description Languages (HDLs), CAD Tools and Design Process *Review:* Digital Design Number systems	Course notes Chapters 1 and 2	*1,2*	*Hw 1*
2	*Combinational Logic Design:* Logic gates, Boolean algebra, Boolean Functions and Equations, Truth Table Combinational logic optimization (K-maps)	Course notes Chapter 2.1-2.6, 2.8	*1, 2*	*Hw 2*
3	*Combinational Logic Design:* MSI logic circuits: Decoders, Encoders, Multiplexers, Code converters Adders, comparators, multipliers, subtractors	Course notes Chapter 2.9-2.10 Chapter 4.1, 4.3, 4.4, 4.6 Chapter 6.1-6.2	*1,2*	*Hw3*
4	*Hardware Description Languages:* Introduction to VHDL, Description of Combinational Logic Circuits using VHDL **MODULE 1-Flipped Classroom Video Tutorial**	Course notes Chapter 9.1 – 9.2. *Optional:* *VHDL book: Ch. 1, 2, and reference material in Ch. 6*	*1,2*	*HW 4* ***Video tutorial***
	EXAM 1			
5	Simulation (Functional Verification) and Test Benches for combinational circuits **MODULE 1-Flipped Classroom Video Tutorial**	Course notes Chapter 9.1 – 9.2.	*2,3*	*Hw 5 … and so on..* ***Video tutorial***

6	*Sequential Logic Design*: Synchronous and Asynchronous Sequential Circuits, Clock Flip-Flops and Latches	Course notes Chapter 3.1, 3.2, 3.5	*1,2,3*	....
7	Registers, Shift Registers, Counters, Timers Impediments to Synchronous Design: Asynchronous Inputs, Clock Skew	Chapter 4.2, 4.8, 4.9 – 4.15 Course notes	*1,2,3*	....
8	Description of Sequential Circuits in VHDL **MODULE 2-Flipped Classroom** **Video Tutorial**	Section 9.3 *Optional: VHDL book:* *Ch. 3*	*1,2,3*	.... **Video Tutorial**
9	Simulation (Functional Verification) and Test Benches for sequential circuits **MODULE 2-Flipped Classroom** **Video Tutorial**	Course notes *Optional: VHDL book:* *Chapter 3, 4*	2,3	.... **Video Tutorial**
10	More Sequential and Combinational Logic description using VHDL	Course notes *Optional VHDL book:* *Chapter 3, 4*	*1,2,3*	....
	EXAM 2			
11	Introduction to FSM (Finite State Machine). Controller design	Course notes Chapter 3.3-3.4	*4*	...
12	Mealy and Moore type FSM	Course notes Chapter6.3	*4*	....
13	Description of Finite State Machine in VHDL **MODULE 3-Flipped Classroom** **Video Tutorial**	Course notes *Optional VHDL book:* *Chapter 3*	*3,4*	.... **Video Tutorial**
14	Simulation and Testbenches for FSM VHDL **MODULE 3-Flipped Classroom** **Video Tutorial** Review	Course notes	3,4	**Video Tutorial**
	EXAM 3			
	FINAL EXAM **Exam Week**			