

Arbitrary Function Generator Laboratory Project

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Abstract

This paper describes the design and operation of a relatively simple ROM-based arbitrary function generator¹ that is suitable for use as an intermediate-level laboratory project in the electronics/electrical engineering technology curriculum. The project integrates many aspects of both analog and digital electronics. From the hardware perspective, the digital portion of the system includes counters, timers, read-only memory (ROM) and a digital-to-analog converter (DAC). The analog portion of the system incorporates operational amplifiers, discrete bipolar transistors and RC filters. This project tends to generate much interest from students, and it provides an effective way of relating many different concepts, such as sampling and quantization, resolution and accuracy, data conversion, lookup tables, linear amplification, summing, buffering and filtering.

Introduction

Electronics students obtain very valuable experience and skills through the design and construction of one or more projects. It is the author's experience that the majority of the current incoming electronics technology students have little or no experience in constructing electronic circuits. Prefabricated kits are acceptable for providing some experience with soldering and basic assembly techniques. However, much more is gained when the student designs and constructs a circuit from scratch.

In terms of courses in which the student is required to construct a project of some sort, the major problem that we encounter at the two-year technology or engineering technology level is that the typical sophomore is simply not knowledgeable enough to any design of a significant nature. The function generator project discussed in this paper is simple enough that the instructor can walk through the design process section by section with the students. In lieu of having the students design the circuit from scratch, they can suggest modifications and alternative design approaches for the various sections that make up the project.

Circuit Description

The function generator schematic diagram is shown in Fig. 1. The circuit may be broken into five sections. Each section may be modified or implemented using an alternative

design approach. It is helpful to have an overall understanding of the operation of the circuit before analyzing each section in detail.

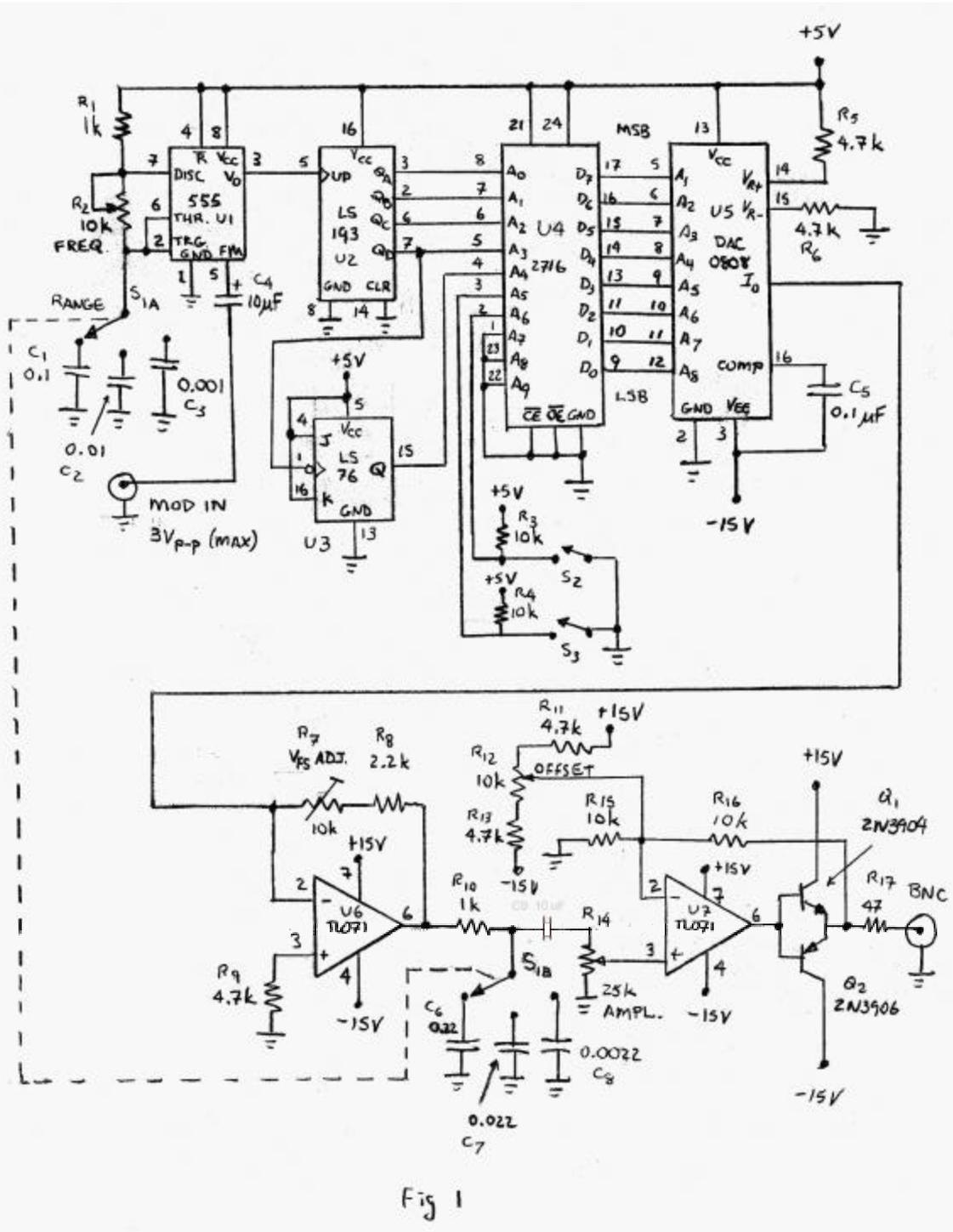


Fig 1

A variable frequency, TTL-compatible clock signal is used to drive a 5-bit binary counter. The output of the counter is used to select waveform data from an EPROM. The EPROM stores one or more lookup tables, each of which consists of 32 bytes. These 8-bit numbers may represent the approximation of a continuous, periodic, analog signal such

as a sine wave or triangular waveform. Using this approach, each cycle of the periodic output signal is divided into 32 equal sample periods that are quantized to 8-bits of resolution. The output of the EPROM is applied to an 8-bit digital-to-analog converter (DAC). The DAC converts a given binary number taken from the lookup table into a proportional current. This current is converted into a voltage by an op amp I/V converter. The resulting output signal will typically appear as shown in Fig. 2(a), where $n = 32$ for the design as shown.

The output of the I/V converter is filtered via a first-order RC LP filter and applied through a variable voltage divider potentiometer to a second op amp. The second op amp is buffered by discrete transistors configured as a push-pull complementary-symmetry amplifier. This op amp also sums an adjustable dc voltage that allows an output offset to be produced if desired.

Clock Generator/Counter

The variable frequency clock source is implemented using a 555 timer IC configured as an astable multivibrator. Continuous frequency adjustment is provided by R_2 , a 10 k Ω potentiometer. Three frequency ranges are selected via half of a DP3T rotary switch S_{1A} , which selects one of three frequency-determining capacitors. This provides roughly 3 decades of adjustment from approximately 686 Hz to near 1 MHz. The modulation input of the 555 timer may be used to allow for experimentation with frequency modulation applications.

The timer drives a 5-bit binary counter. The counter is implemented with a 74LS193 4-bit binary counter providing the four least significant bits (LSBs) of the count while a 74LS76 dual JK flip-flop provides the most significant bit (MSB). A five-bit counter was chosen to provide a reasonable tradeoff between quantization noise and maximum output frequency. The maximum oscillation frequency of a 555 timer is around 1 MHz. Because the output frequency is $f_{cl}/32$ we have $f_{out(max)} \cong 31$ kHz. Reducing the counter to 4 bits would double the maximum output frequency to approximately 62 kHz. This also reduces the lookup table size by one-half to 16 values as well, which would make the output waveform a much less accurate approximation of a continuous signal, and making the filtering of the signal much more difficult.

Because the 555 timer is rather limited in maximum oscillation frequency, students could be encouraged to devise alternative variable frequency clock circuits that would allow higher output frequencies to be produced.

The Data Lookup Table

In order to provide different output waveforms, switches S_2 and S_3 allow the selection of any of four different 32-byte lookup tables within the 2716 1024x8 EPROM. Setting both switches low selects addresses 000000000₂ through 000001111₂ of the EPROM as the lookup table. This section may contain data for a sine wave, for example. Setting S_3 (the MSB of the lookup table base address) low and S_2 high selects the next 32 bytes of the

EPROM as the lookup table (addresses 0000100000₂ through 0000111111₂). This section of the EPROM could contain data for a triangular output waveform, for example. A given lookup table is read through once every 32 clock cycles, and assuming that the lookup table contains data for one cycle of the desired output signal, the frequency is

$$f_{out} = f_{clk}/32.$$

Because the 2716 can hold 1024 bytes of data, it is possible to implement as many as 32 different 32-byte lookup tables, with the addition of more select switches. As one of many possible modifications, the students could be asked to design a digital circuit that allows these waveform tables to be selected using a pushbutton switch that sequences through the waveforms.

Generating data for a waveform such as triangular or sawtooth signal is very easy. It is a little more difficult to generate the data for a sine wave, however. This is another task that could be assigned to the students. The author used the following BASIC program to generate the sine wave data.

```
for theta = 0 to 6.2832 step 0.196      ;Divide cycle into 32 parts
n = sin(theta)*127 + 128                ;Calculate sine, scale and shift above zero
print hex$(n)                          ;Print hexadecimal value
next theta                              ;Repeat until theta = 2π
```

The values generated entered into the EEPROM using a standard EPROM programmer. Additional data for other waveforms may be entered as necessary into successive 32 byte blocks of the EPROM. The lookup table approach is very flexible, allowing very unusual signals such as heart rhythms or seismic waveforms to be simulated relatively easily.

The DAC

A given byte that is output from the lookup table is applied to a DAC0808. The DAC0808 is configured to sink a proportional output current to the negative supply rail. Full-scale output current is given by

$$\begin{aligned} I_{FS} &= -V_{CC}/R_5 \\ &= -5 \text{ V}/4.7 \text{ k}\Omega \\ &\cong -1.063 \text{ mA} \end{aligned}$$

The LSB size of the DAC output is

$$\begin{aligned} 1 \text{ LSB} &= I_{FS}/2^8 \\ &= -1.063 \text{ mA}/256 \\ &\cong -4.152 \mu\text{A} \end{aligned}$$

Suggestions for student modifications at this point include the use of an alternate DAC.

The I/V Converter

The output of the DAC is converted into a proportional voltage by U6, a TL071 JFET input op amp. Resistor R_7 is a trimmer potentiometer that is used to set the full-scale output of the I/V converter² for $V_{FS} = 5.00$ V. The TL071 was chosen because it has a slew rate of 13 V/ μ s, which allows signals with fast rise and fall times to be generated, if necessary. This is another place where the student could be asked to determine the limitations imposed by op amp slew rate. For example, the student could be asked to investigate the effects of using an op amp such as the 741, which has a slew rate of approximately 0.5 V/ μ s.

The Low-Pass Filter

When a signal such as a sine wave is produced, the output of the I/V converter will contain a significant level of quantization noise³. This noise gives the output signal a stair-step appearance, as shown in Fig. 2(a). The quantization noise frequency components begin at approximately 32 times the output signal frequency (because there are 32 steps in each cycle of the output). A first order low-pass filter is used to smooth this noise. The corner frequency of the filter should be somewhat higher than the highest output frequency on a given range, but significantly lower than the first quantization noise component at $32f_{out}$. This allows good rejection of the noise, while having minimal effect on the amplitude of the desired signal. A representation of the signal spectrum and the desired filter response is shown in Fig. 2(b). The corner frequency of the filter is switched simultaneously with the range of the clock source via capacitors C_6 through C_8 and S_{1B} .

Topics of discussion that could be expanded upon at this point include higher-order

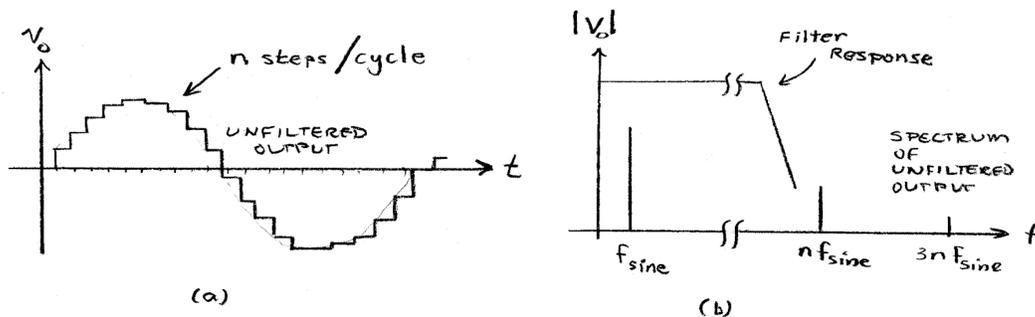


Fig 2

Output Stage/Summer

The output of the LP filter is coupled through C_{10} in order to remove the dc offset produced by the DAC and I/V converter. This final stage utilizes a second TL071 op amp configured for a voltage-gain of 2, effectively providing a -10 V to 10 V range at the

output. A discrete bipolar transistor push-pull output stage added for increased current drive capability. The push-pull pair is within the feedback loop of the op amp, which effectively eliminates crossover distortion and the need for biasing circuitry. This section also serves to sum a variable offset voltage with the output signal. The maximum output voltage is approximately $20 V_{P-P}$.

As the circuit is presented in Fig. 1, it is possible for the output to have a significant dc offset, unless a dc voltmeter or an oscilloscope is used in conjunction with the offset adjust potentiometer. This section of the function generator could be modified by the inclusion of circuitry that allows the offset voltage to be set to 0 V.

Final Considerations

The function generator presented in this paper has been breadboarded successfully many times by the author's students. No special attention to layout is required other than the usual practices such as keeping interconnect and power supply lead lengths to a minimum. It is also advised to use $0.01 \mu\text{F}$ decoupling capacitors mounted across the power and ground pins of the TTL devices, which helps prevent erratic operation.

Bibliography

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