# **BOARD #356: ECR: BCSER: Are Females Better at Debugging Circuits?**

#### Andrew Jay Ash, Oklahoma State University

Andrew J. Ash is a PhD student in Electrical Engineering in the School of Electrical and Computer Engineering at OSU and he is a research assistant in Dr. John Hu's Analog VLSI Laboratory. He received his B.S. in Electrical Engineering from Oklahoma Christian University. Andrew's research interests include engineering education and hardware security of data converters and neural networks.

#### Dr. John Hu, Oklahoma State University

John Hu received his B.S. in Electronics and Information Engineering from Beihang University, Beijing, China, in 2006 and his M.S. and Ph.D. in electrical and computer engineering from the Ohio State University, Columbus, OH, in 2007 and 2010, respectively. He worked as an analog IC designer at Texas Instruments, Dallas, between 2011 and 2012. He was a Member of Technical Staff, IC Design at Maxim Integrated, San Diego, CA, between 2012 and 2016, and a Staff Engineer at Qualcomm, Tempe, AZ, between 2016 and 2019. In 2019, he joined the School of Electrical and Computer Engineering at Oklahoma State University, where he is currently an assistant professor and Jack H. Graham Endowed Fellow of Engineering. His research interests include power management IC design, hardware security, and energy-efficient computing.

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## Introduction

In the semiconductor industry, debugging is sometimes called "The Schedule Killer" due to its unpredictable and costly nature [1]. Some electronics engineers spend up to 44% of their time on debugging tasks [2], yet this industry-critical skill is frequently omitted from undergraduate curricula [3], [4]. Instead, students are often expected to develop debugging skills indirectly through projects and labs without targeted training. These challenges make teaching debugging a "million-dollar" question [5] that could improve undergraduate student outcomes and increase workplace readiness. To address this gap, our team developed customized, laboratory-based tests to assess circuit debugging performance and better understand ECE students' skills. This brief summarizes findings from the first semester of data collection and highlights emerging trends for further exploration as additional data is gathered.

# **Debugging Exam Overview**

We collected student data using three problems focused on a malfunctioning op-amp, incorrect equipment settings, and selecting a component with the wrong specifications. Fig. 1 illustrates a correct non-inverting op-amp circuit alongside two buggy implementations on a TL074 IC [6]. The middle image depicts a bug caused by misorienting the integrated circuit (IC) on the PCB. The swapped +15 V and -15 V power supply connections force the output to remain near 0 V. The right image shows a bug caused by incorrect equipment settings. An oscilloscope probe is set to attenuate the signal by a factor of ten, while the oscilloscope expects an unattenuated signal. This results in a measured gain that is one-tenth of the actual value. Fig. 2 shows the correctly implemented Greinacher voltage doubler [7] using Schottky diodes and a circuit using diodes with a larger voltage drop that prevents the expected output behavior. Detailed circuit and exam format descriptions can be found in [8].

Students were randomly assigned one of the three debugging problems. Each test had a 15-minute time limit, with the option to request an additional 15 minutes to continue debugging the circuit if a student was not ready to submit their solution.

The test handout instructed students to identify circuit symptoms based on lab measurements, use the symptoms to hypothesize potential root causes, and attempt to resolve the issue to restore the expected circuit operation. Written responses and the research team's observation notes were qualitatively analyzed to identify key themes in the debugging skills of undergraduate ECE students. Qualitative data analysis was conducted with a constant comparative method [9]. The time to complete the exam and the performance parameters of the debugged circuit serve as quantitative data sources for our ongoing research.

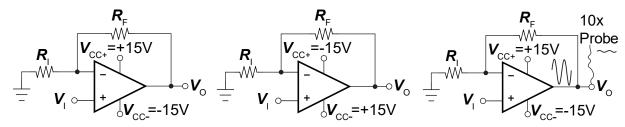


Fig. 1: The functional non-inverting amplifier (left) and the resulting bugs from misorienting the amplifier (center) and using the wrong oscilloscope probe settings (right)

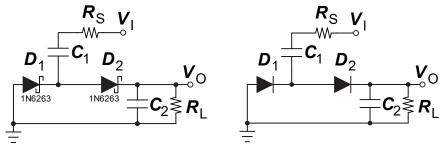


Fig 2: The Greinacher voltage doubler (left) high voltage drop diodes cause a bug (right)

Students were informed that the test was experimental and that declining data collection would not affect their final grades. Consent forms were signed privately before taking the exam. Data from students who chose not to participate were excluded from the analysis.

### **Results**

In the Spring 2024 semester, of the students who agreed to participate, 26 were assigned the flipped op-amp circuit. Trial runs of the 10x probe (2 students) and voltage doubler (1 student) problems were conducted to evaluate their suitability for future debugging exams.

Table I summarizes the success rates of the three problems. Overall, 9 out of 29 students (31%) successfully debugged their assigned circuit within 30 minutes. Of the 26 students who attempted the flipped op-amp circuit, 8 (31%) successfully identified and corrected the bug. The 10x probe problem had a 50% success rate, with one student finding the problem almost immediately while the other never considered the equipment as a source of error. The one student who attempted the voltage doubler could not identify the problem.

The malfunctioning op-amp and equipment settings bugs were determined to be worth further exploration in their current form. However, the research team concluded that the diode problem was too difficult to solve within the time limit. Diode part numbers were illegible without a vision aid. Students would need to characterize each diode and compare the results to the datasheets for all diodes available in the lab to determine the appropriate diode for the circuit.

**Table I: Student Success Rates for Four Debugging Problems** 

	Success Rate		
Problem	Total	Female	Male
Misoriented Op-amp	8 / 26 (31%)	3 / 3 (100%)	5 / 23 (22%)
10x Probe	1 / 2 (50%)	N/A	1 / 2 (50%)
Diode	0 / 1 (0%)	N/A	0 / 1 (0%)
Total	9 / 29 (31%)	3 / 3 (100%)	6 / 26 (23%)

Student responses highlighted common trends in debugging mistakes. The most frequent issue is attributing errors to a faulty resistor without exploring other potential causes. Students also misinterpreted in-situ resistance measurements or the results of oscilloscope readings, leading to flawed solutions. For more information on these themes, refer to [10]. Identifying these common pitfalls informs the development of the debugging training curriculum to be implemented in later research stages.

## Gender Gap

Although the sample size is too small for definitive conclusions, data from the first group of students suggests an emerging trend. All three female (100%) students successfully debugged the misoriented op-amp circuit within 30 minutes, compared to 5 of 23 (22%) male students. Only male students attempted the incorrect equipment settings and component specification problems.

Are female students better at debugging? It may be too early to tell. If this trend persists as the sample size grows, we plan to investigate other potential contributing factors, such as final course grades and composite GPAs, before determining whether a baseline difference in debugging habits exists between male and female students. However, our ability to recruit a more statistically significant number of female participants is limited, as students must be enrolled in our university's Fundamentals of Microelectronics course to participate. A statistically significant sample will likely require several more semesters of data collection. While further data is necessary for conclusive insights, preliminary findings support the need to broaden female student participation in ECE. A wide range of debugging perspectives could help mitigate the impact of "the schedule killer" in the semiconductor industry.

#### Conclusion

The results of the first semester indicate that our debug assessments identify gaps in students' debugging skills. As we introduce targeted debugging skills training in the next research phase, we will monitor trends across gender and other demographic categories to ensure the program enhances debugging skills for all students.

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### References

- [1] B. Bailey, "Debug: The schedule killer," Jun. 2021. [Online]. Available: https://semiengineering.com/debug-the-schedule-killer/
- [2] A. Mutschler, "Debug tops verification tasks," Dec. 2018. [Online]. Available: https://semiengineering.com/debug-tops-verification-tasks/
- [3] H. Duwe, D. T. Rover, P. H. Jones, N. D. Fila, and M. Mina, "Defining and supporting a debugging mindset in computer engineering courses," in *2022 IEEE Frontiers in Educ. Conf. (FIE)*, Oct. 2022, pp. 1–9, iSSN: 2377-634X.
- [4] M. E. Radu and S. M. Sexton, "Integrating extensive functional verification into digital design education," *IEEE Trans. on Educ.*, vol. 51, no. 3, pp. 385–393, Aug. 2008.
- [5] H. Mehraban and J. Hu, "Board 293: How to teach debugging? The next million-dollar question in microelectronics education," in *2024 ASEE Annu. Conf. & Expo. Proc.*, Portland, Oregon: ASEE Conferences, Jun. 2024, p. 46869. doi: 10.18260/1-2--46869.
- [6] Texas Instruments, "TL07xx low-noise FET-input operational amplifiers," ti.com. [Online]. Available: https://www.ti.com/lit/ds/symlink/tl074.pdf
- [7] H. Greinacher, "Über eine Methode, Wechselstrom mittels elektrischer Ventile und Kondensatoren in hochgespannten Gleichstrom umzuwandeln," *Z. Physik*, vol. 4, no. 2, pp. 195–205, Jun. 1921, doi: 10.1007/BF01328615.
- [8] A. Ash, J. Cribbs, and J. Hu, "Board 94: Work in progress: Development of lab-based assessment tools to gauge undergraduates' circuit debugging skills and performance," in 2024 ASEE Annu. Conf. & Expo. Proc., Portland, Oregon: ASEE Conferences, Jun. 2024, p. 48395. doi: 10.18260/1-2--48395.
- [9] K. Charmaz, Constructing grounded theory: A practical guide through qualitative analysis. Sage, 2006.
- [10] A. Ash and J. Hu, "It must be the resistor!' A pilot study unveiling student debugging misconceptions and biases" in 2025 IEEE Int. Symp. Circuits Syst. (ISCAS), 2025, to appear.