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Cadence setup for chip layout

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Abstract. This paper describes an effort at understanding the Cadence flow set up for VLSI design in 180nm technology and updating it to the newer 45nm technology node. This project was undertaken because there are four VLSI design courses offered in our department that use Cadence. When the Cadence software license was updated to the latest version, the original set up for all these courses stopped working. So, we decided to systematically study the current setup files for Cadence tool for the 180nm technology and update it to 45nm. To integrate the update into machine problems (MPs) for our course, the manuals were updated to utilize the new library. Once updated, the MPs were tested to ensure proper integration. As part of this project, we learned how to set up Cadence for any technology library and learned the scripting language for writing the files. This work will be useful for anyone looking to set up a new Cadence license for use in circuit design, simulation, layout, and tape out for chip fabrication.

1. Introduction

The Cadence software is used for testing and creating schematics and layouts for VLSI circuits. The set up of the software can be modified according to user requirements – in this case for a VLSI design course. To set up Cadence, some files are required. These files include information on license, the library used (specific to the technology node) and any testing software being used. The files are written using the scripting language. Here we describe how one can do the Cadence set up to incorporate the license, technology library and any testing software required for the project. To check proper integration with the newer technology files, the updated software was tested on a set of four machine problems for the course. In these machine problems (MP0-MP3), the students create layout for a 4-bit AM2901 processor after thoroughly testing it. The last MP for the course (MP3) also requires automatic synthesis of AM2901 controller from the Verilog files. This was done in Synopsys. Therefore, the files required for Synopsys setup were also updated. The following sections describe both Cadence set up and update of Synopsys setup to enable chip layout using 45nm technology node.

2. Methods: studying and updating the files

This section describes the files and libraries that were updated to set up Cadence and Synopsys to create schematics and layouts using the 45nm technology node instead of the 180nm.

A. Adding 45nm Cadence Library

For 45nm technology, the gpdk045 (general process development kit for 45nm technology) library file was taken from the Cadence webpage [1]. A student account was created with the university's approval. Most of the required environment files such as cds.lib, simrc, cdsplotinit, cdsenv, cdsinit were also included in this kit. The gpdk045 library was added to the class folder which will be copied over into each student's working directory using the initialization script described below.

B. The set up files

The cdsplotinit, cdsenv, cdsinit and simrc files were downloaded along with the gpdk045 library from the Cadence website. And included in the library folder provided for the students to copy.

As a student will source the initialization script, these files will be copied along with the gpdk045 library into the student's work directory.

C. Initialization Script

The primary objective of the initialization script is to facilitate copying the 45nm technology development kit within the student work directory without manually handling the library, files and license information. The file is written using scripting language. In 180nm technology, this script referenced the Cadence and Synopsys licenses, defined an easy acronym for path to Virtuoso, path to Assura and changed the CDS netlisting mode to analog. This part of the script was retained for the 45nm technology. For 180nm, the file also referenced the libraries and environment files used for 180nm technology. To adapt the script for 45nm technology, a copy command was added to it to copy over the gpdk045 library into the students' working directory. And this gpdk045 library contains all the set up files as mentioned above.

Table 1. Summary of changes made to files to update the Cadence & Synopsys set up and the source of files

Files Updated	180nm technology	45nm technology	Source
Gpdk045 library. Is the 45nm technology node library	tsmc library was used	Replaced tsmc with gpdk045 library	Cadence website [1]
Init_gpdk045.sh file. Automates setting up the environment in each student's work directory without accessing license file	References 180nm technology node specific files	Updated to reference 45nm technology node specific files	Course files
Cds.lib file. Defines different libraries used for the design	References old versions of libraries and tutorials	References libraries specific to 45nm node	Gpdk045 library
.**cdsplotinit file.** Configures plotting environment. **.cdsenv file.** Configures overall environment. .**cdsinit file.** Configures initialization settings. .**simrc file.** Configures simulation environment	from tsmc 180nm library	Replaced with files specific to 45nm technology	Gpdk045 library from Cadence
Target45.dc file. script used to specify library for physical design.	References the tsmc lib file	References to gscl45nm.db	Course files
Gscl45nm.lib file. Technology library file for 45nm technology (it is in ASCII format) **Gscl45nm.db file.** Binary version of the .lib file which is eventually read by Synopsys **Gscl45nm.lef file**. Contains information about the physical and logical properties of standard cell libraries	Tsmc files for 180nm are used	Gscl45nm files are used	Free45PDK[2]
Mp3.conf file. Configures library and lef files for innovus.	Points to tsmc .lib and .lef files	points to gscl45nm.lib and gscl45nm.lef	Course files
Nmos1v file. Defines the nmos functionality for NC Verilog Simulation. **pmos1v file**. Defines the pmos functionality in Verilog code for NC Verilog Simulation.	180nm library came with the Verilog code	Added Verilog file	Cadence Support[3]
Comptut.pdf file. Tutorial to create schematic in Cadence Virtuoso. **Celltut.pdf file**. Tutorial to create layout in Cadence Virtuoso and check DRC and LVS.	Instructions for 180nm technology	Updated to 45nm technology	Course files

D. **Cds.lb file**

Its primary purpose is to define and organize Cadence design libraries for projects using the designated technology. In the context of the 180nm technology, the cds.lib file contained libraries and settings for the 180nm process and those used in the MP0 tutorials for schematic and layout. These libraries included- the TTL_tutor which contains the standard TTL parts used in the tutorial design, the US_8ths which comes with the Virtuoso Schematic Editor software and contains templates for page borders, the Basic library that comes with the schematic editor software and contains basic symbols as ground and power, the Master library that contains copies of the designs used in the tutorial, the Sample library which has a sample of gates and other electronic circuitry, the tutorial library which is a design library in which the students create schematics, the user_ASIC library that contains the Arithmetic Logic Unit (ALU) used and the analogLib which is a reference library for analog parts. To adapt the cds.lib file to the 45nm technology, paths to the gpdk045 library and a new library, MP0 was added. MP0 library enclosed: tutorial, user_ASIC, sample, TTL_tutor, US_8ths, analogLib and master libraries. Hence, the libraries included in 45nm technology node cds.lib are the basic library as for 180nm, the gpdk045 library that contains all cells for 45nm technology node and the mp0 library in which the students create the schematic and layout of inverter, ALU and multiplexer.

E. **Tutorial files**

The Comptut tutorial file is used in MP0 to guide through creating schematics, adding pins, and navigating hierarchies in Cadence Virtuoso. This file outlines how to set up the environment, to add new cell view and libraries to create schematic of an accumulator. For 45nm, it was updated to include new commands to set up the environment and to include screenshots of the results. Correspondingly, the designs provided to students were also updated to 45nm technology node and included in the mp0 folder that was created. This folder was created inside the gpdk045 library folder so it will also be copied into the student work directory when they copy the gpdk045 library from the course folder. The Celltut tutorial file begins by teaching layout of a simple inverter given its schematic, and then teaches combination of nand2 and inverter layouts to create a multiplexer layout. It also guides through the DRC and LVS errors. The contents of celltut.pdf were updated to conform to the stricter layout rules for the 45nm technology. Additionally, all schematics (inverter, nand and multiplexer) and layout of nand2 were created in 45nm technology.

F. **UPDATING NC VERILOG**

NC Verilog is used to visualize simulation waveforms. It requires Verilog code of the pmos and nmos cells. The gpdk045 kit from Cadence website does not include these Verilog codes, which caused errors (shown in screenshot below). To resolve these errors, the Verilog codes were added from Cadence Support[3].

G. **Target45.dc File**

In Synopsys Design Vision, the target45.dc file is a script or command file used to specify various settings and constraints for the synthesis process. It is employed with Design Compiler (DC), which is a synthesis tool used in the digital design flow to convert RTL (Register-Transfer Level) code into a gate-level netlist. The primary purpose of the target.dc file is to provide a set of directives, commands, and settings to guide the Design Compiler during the synthesis process. For 180nm technology, the file uses the tsmc 180nm library's .db file by using the following command.

set target_library {vtvt/Synopsys_Libraries/libs/vtvt_tsmc250.db};

The vtvt folder was downloaded into the student work directory for the tsmc250.db file. For the 45nm technology, the target45.dc sets the library to gscl45nm.db which was downloaded from the Free45PDK[2] as described below.

H. **Gscl45nm.lb file**

The gscl45nm.lib file is a library file associated with the 45nm semiconductor manufacturing process and is commonly used in conjunction with Synopsys tools, such as Design Compiler. The primary purpose of the gscl45nm.lib file is to serve as a technology library that contains information about standard cells, I/O cells, and other elements specific to the 45nm technology node. The gscl45nm.lib file describes the timing, power, area, and other relevant characteristics of standard cells used in digital design. For the 45nm technology, the gscl45nm.lib file was procured from an open source [2] Free45 PDK (process development kit). This kit was compatible with the Cadence gpdk045 and worked well for place and route tools such as Synopsys Design Vision and Cadence Innovus.

I. **Gscl45nm.lib file**

It is a binary version of the gscl45nm.lib file and is created by using a script to convert the .lib file to .db file. For 45nm technology, this file was taken from Free45PDK [2].

J. **Gscl45nm.lef file**

The gscl45nm.lef file is a Library Exchange Format (LEF) file that provides a standardized format for describing the geometric and electrical properties of standard cells within the 45nm technology node. LEF files enable interoperability between different EDA tools, allowing chip designers to use a consistent format for exchanging information about the physical layout of standard cells. It contains entries describing the physical characteristics of standard cells, including their dimensions, locations of pins, metal layer information, and other layout details. LEF files are crucial for physical design tools such as place and route tools, as they provide essential information about the physical implementation of standard cells on the chip. For 45nm technology, this file was taken from Free45PDK.

K. **MP3.Conf**

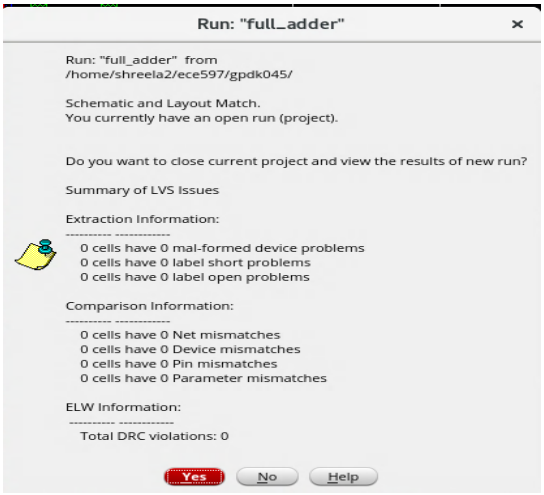
The mp3.conf file stores configuration settings and parameters for creating an automated layout from Verilog file for AM2901 controller in Synopsys. For 180nm, this file references the files such as .lib and .lef. This file was updated to point to the gscl45nm.lib and gscl45nm.lef files instead of to the 180nm library specific files.

3. Testing and results

After updating all the required files for setting Cadence and Synopsys to the 45nm technology node, it was tested on the MPs from the course.

Machine Problem 0. This MP familiarizes students with the basics of Cadence Virtuoso using the celltut and comptut tutorials. Since the tutorial files were re-written for 45nm technology node, they had to be tested. The schematics and layout of inverter, NAND2, MUX were created and then used to create the schematic of an accumulator. For the schematic, "check and save" was used to see whether the design was correct. For the layout, DRC and LVS were performed. These passed successfully.

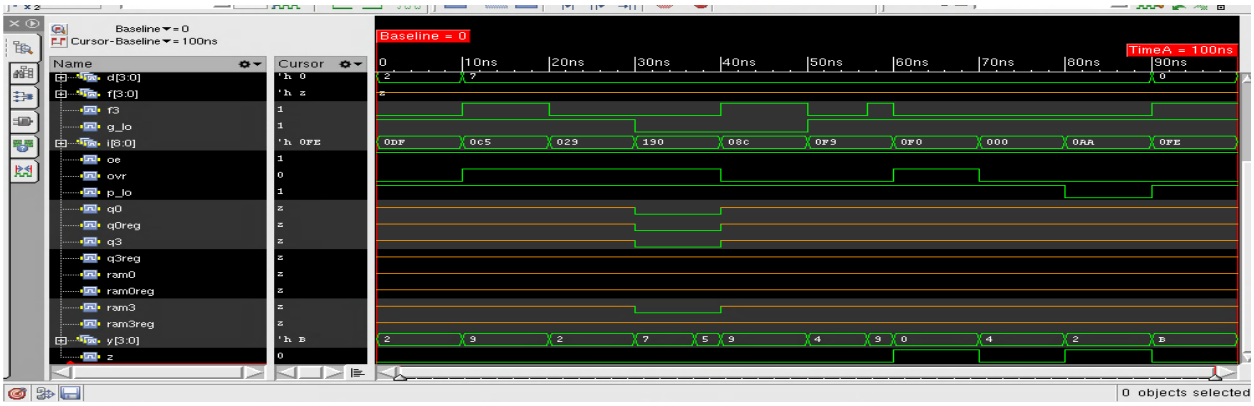
Machine Problem 1. It guides students to create schematic and layout of an 8-bit adder. Once MP0 was successfully tested and updated, MP1 could be completed without any additional updates. Schematics and layouts of xor2, nand2, inv, half adder, full adder and 8-bit adder were successfully created and checked with DRC, LVS and NC Verilog simulation. LVS results from the 8-bit adder are shown here.



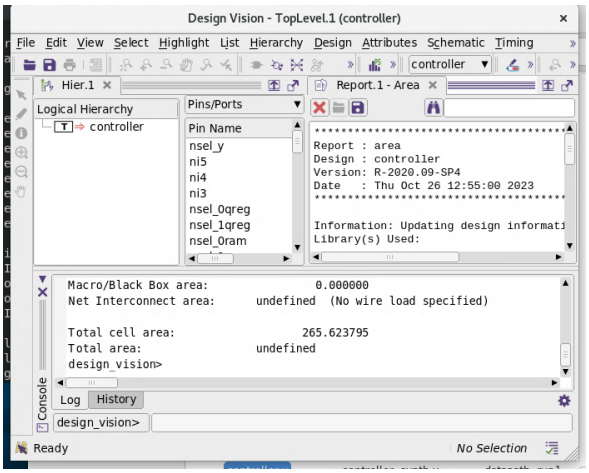
NC Verilog simulation comparison report of 8-bit adder with the golden file was as below.

```
28 Comparison summary:
29
30   Successful compares: 6/6
31   No problems found.
```

Machine Problem 2. Includes designing the schematic and layout of the 4-bit am2901 microprocessor. So, schematic and layout of the am2901 datapath and memory modules was created using 45nm technology. The layout was successfully tested using DRC and LVS. Circuit simulation was successfully analyzed using NC Verilog, result from which is shown below.



Machine Problem 3. Teaches the automated synthesis of the AM2901 controller using Verilog code in Synopsys. The design was automated using the updated files for the 45nm technology library as described earlier. The controller layout from Synopsys was successfully integrated with that of the datapath generated in Cadence in MP2. The results from design vision are shown below.



4. Conclusion

The project aimed to learn Cadence setup and update it from 180nm to 45nm technology node for a VLSI design course. Since Synopsys was used for the automated controller synthesis in this course, set up for it was also updated to 45nm technology. This update included various setup files written in the scripting language. Once the setup files were updated, it was successfully tested by working through the machine problems (MPs) designated for the course. Based on this experience, any further updates to the technology node can be integrated.

5. References

[1] Cadence, General Process Design Kit for 45nm technology < https://support.cadence.com/apex/ArticleAttachmentPortal?id=a1Od000000051TqEAI&pageName=GPDKs > Accessed in March 2023.

[2] Free45 PDK < https://github.com/The-OpenROAD-Project-Attic/OpenROAD-Utilities/tree/master/TimerCalibration/Free45PDK > Accessed in September 2023.

[3] NC Verilog Error Resolution from Cadence Support < https://support.cadence.com/apex/ArticleAttachmentPortal?id=a1O0V000009MqKvUAK&pageName=ArticleContent > Accessed June 2023.