# AC 2011-892: COLLABORATIVE CURRICULUM DEVELOPMENT OF AN INDUSTRY-DRIVEN DIGITAL LOGIC DESIGN

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# Collaborative Curriculum Development of an Industry-Driven Digital Logic Design


## Abstract

Hardware Description Language and Field Programmable Gate Array (FPGA) have revolutionized the way Digital Logic Design is taught and implemented. Traditional ways of teaching logic design using discrete components (TTL: Transistor-Transistor Logic and CMOS: Complementary Metal Oxide Semiconductors) have been replaced by Programmable Logic Devices (CPLD: Complex Programmable Logic Devices and FPGA). Today, a more standard development process is widely used in industry. The process uses Hardware Description Languages as a design entry to describe the digital systems. The two most widely used Hardware Description Languages in industry are VHDL (Very High Speed Integrated Circuit Hardware Description Language) and Verilog (Verifying Logic). Although most traditional electrical and computer engineering programs have updated their curriculum to include topics in hardware description language and programmable logic design (FPGA/CPLD), two-year and four-year electrical engineering technology programs have fallen behind and moved slowly in updating their curriculum. This paper describes the industry-led faculty training and digital logic design curriculum development that will reshape the way digital logic design is taught in the electrical engineering technology programs. The new curriculum development will provide students with a hands-on educational experience well-respected by industry.


## I. Introduction

Programmable Logic Devices in general and FPGA-based re-programmable logic design became more attractive as a design medium during the last decade, and as a result, industrial use of FPGA in digital logic design is increasing rapidly. As would be expected following technology change in industry, the need for highly qualified logic designers with FPGA expertise is increasing at a fast rate. According to the United States Department of Labor, the job outlook is on the rise and will continue to expand for at least the short- to medium-term future [1]. To respond to the industry needs for FPGA design skills, universities are updating their curriculum with courses in hardware description languages and programmable logic design. Although most traditional electrical and computer engineering programs have updated their curriculum to include topics in hardware description language and programmable logic design (FPGA/CPLD), only 19.5 % of 4-year and 16.5 % of 2-year electrical and computer engineering technology programs at US academic institutions currently have a curriculum component in hardware description language and programmable logic design [3]. To effectively meet the next generation's workforce needs, the electrical and computer engineering technology curriculum must be current, relevant, and teach technology that is widely used in industry. To meet this goal, we propose a curriculum development in the electrical engineering technology program digital logic design series. Faculty involved in developing and teaching the new curriculum must be well-informed of advances in technology currently used in industry. Likewise, industry wants to have qualified and well-educated employees coming out of academia who are ready to implement their knowledge on day one of their employment. As a result, while academia needs to be fully aware of the current state-of-the-art knowledge requirements, industry must be driving the curriculum development. Therefore, in this curriculum development, a strong link between

academia and industry must be established. This partnership is a "two-way street" and advantageous for both parties. The Electrical Engineering Technology (EET) program is collaborating with Altera University program in which the involved faculty members will attend a set of training workshops developed by Altera's university program. These workshops are targeted toward professional individuals and college faculty seeking knowledge and expertise in programmable logic design. Faculty members having the opportunity to attend these workshops will gain the knowledge and expertise to teach both VHDL digital Design and Programmable Logic (FPGA) design courses. The exposure to industry-taught courses will help the faculty members to impact the learning experience of his/her undergraduate students by providing them with skills that are highly marketable and appreciated by industry.

## II. Research Background

Historically, electrical engineering technology Baccalaureate programs have included a traditional logic design course that covers topics in combinational logic and sequential logic circuits. The course is usually based on discrete components (such as TTL and CMOS), and although these topics represent fundamental concepts in logic design and optimization theory, they are far from most current industry practice in logic design. Topics that are traditionally taught in logic design courses are less important to current employers. The time spent teaching Boolean algebra and how to minimize Boolean expressions using Boolean algebra or Karranugh Map (K-Map) can be better spent teaching current and industry-relevant practice in logic design. This line of thought applies to design of combinational circuits and also to the design of sequential circuits [3]. For the curriculum to adequately meet the current industry needs, the EET programs must teach digital logic using VHDL and FPGA [3] to equip students with design skills that are current, relevant, and widely used in industry.

Recent research also suggests that the proposed courses are industry-relevant. Furtner and Widmer conducted an employer survey to rank currently taught logic design concepts at Purdue University [3]. The survey included questions about many topics that are heavily explained in logic design courses such as Boolean algebra, design simplifications using K-Map or Quine Mclusky, and design implementation using discrete gates. Each was given a low priority from the employer perspective. On the other hand, topics that cover designing with hardware description language (such as VHDL or Verilog) received high-priority rankings from employers [3].

Unfortunately, the curriculum has not yet "caught up" to industry needs. A survey of digital design textbooks users by Pearson's Press shows that only 19.5% of the total of 52 four-year electrical engineering technology programs who responded to the survey cover topics in logic design using hardware description languages, and only 40% of the four-year are planning to introduce hardware description languages in the near future [3].

Clearly, electrical engineering technology programs are far behind in teaching the skills that represent current and future industry needs. As a result, the School of Technology is stepping up to this challenge by developing and introducing curriculum in hardware description languages and programmable logic design. The major objectives of this curriculum shift are to give the students in the Electrical Engineering Technology program the opportunity to learn and experience logic design using FPGA that is in line with industry expectations.

## III. Faculty Development

Most of the FPGA vendors regularly offer a set of training workshops targeted toward professional individuals and college faculty seeking knowledge and expertise in programmable logic design with some of the workshops are offered online. Faculty members participating in these workshops will gain the knowledge and expertise necessary to teach both VHDL digital Design and Programmable Logic (FPGA) design courses.

Altera Corporation represents a market leader and holds a large market share in programmable logic. Each FPGA vendor development software is device dependent, for example, Altera's Quartus® II development software only targets Altera's device family. Learning Altera's Quartus® II development software will give students the opportunity to learn FPGA design flow using the most widely used tools for FPGA design. At the same time, these skills are largely transferable to other design tools, so students will learn valuable skills useful across industrial platforms. The exposure to industry-taught courses will help the faculty members to impact the learning experience of undergraduate students by providing them with skills that are highly marketable and appreciated by industry. So far, two faculty members have enrolled and successfully completed the following Altera University program courses:

**Introduction to VHDL:**
**Course Description**
This course provides introduction to the VHDL language and its use in programmable logic design. The emphasis is on the synthesis constructs of VHDL. Faculty members will gain a basic understanding of VHDL. The course is laboratory intensive and includes a hands-on experiment to design, test, and simulate and synthesize a basic logic circuit as part of Quartus® II development software [2]. The course objectives are to have class participants are able to:

- Understand simulation versus synthesis environments
- Build basic VHDL models using the VHDL design units (entity, architecture, configuration, package)
- Use behavioral modeling constructs and techniques to describe logic functionality
- Use structural modeling constructs and techniques to create hierarchical designs

**Advanced VHDL:**
**Course Description:**
Faculty members will learn how to write efficient coding techniques for VHDL synthesis, particularly for Altera® devices. The faculty member will gain experience writing behavioral and structural code and learn how to effectively code common logic functions including registered, memory, and arithmetic functions. As part of the course topics, faculty members will learn how to write testbenches to verify the functionality of the design [2]. The course objectives are to have class participants are able to:

- Develop coding styles for efficient synthesis when:
- Targeting device features
- Inferring logic functions
- Using arithmetic operators
- Writing state machines
- Use Quartus II software RTL Viewer to verify correct synthesis results

- Incorporate Altera structural blocks in VHDL designs
- Write simple testbenches for verification
- Create parameterized designs

**The Quartus II Software Design Series:**
**Course Description**
The course provides extensive training on how to use Quartus® II development software to develop an FPGA or CPLD. Faculty will be able to create a new project, enter in new or existing design files, and compile their design. Faculty will learn how to plan and manage I/O assignments and apply timing analysis of design to achieve design goals using Quartus® II development software [2]. The course objectives are to have class participants are able to:

- Make pre-project decisions to prepare for Quartus II design
- Create, manage & compile Quartus II projects
- Use Quartus II tools to view the results of compilation
- Plan & manage device I/O assignments using Pin Planner
- Use the basics of the TimeQuest timing tool
- Review compilation results in various Quartus II software reports and graphical viewers

**The Quartus II Software Design Series: Timing Analysis**
**Course Description**
Faculty members will learn how to constrain & analyze a design for timing using the TimeQuest timing analyzer in the Quartus® II software. This includes understanding FPGA timing parameters, writing Synopsys Design Constraint (SDC) files, generating various timing reports in the TimeQuest timing analyzer, and applying this knowledge to an FPGA design. Faculty will learn how to ensure that the design meets timing requirements [2]. The course objectives are to have class participants are able to:

- Understand the TimeQuest timing analyzer timing analysis design flow
- Apply basic and complex timing constraints to an FPGA design
- Analyze an FPGA design for timing using the TimeQuest timing analyzer
- Write and manipulate SDC files for analysis and controlling the Quartus II compilation

**Interfacing to External Memory with Altera FPGAs**
**Course Description:**
Faculty members will learn how to implement external memory interfaces with Altera® FPGAs & Quartus® II development software. Topics covered include memory interface and how to implement it, designing a memory controller with focus on implementing DDR 1 & 2 memory interfaces. The course includes a complete a memory interfacing design [2]. The course objectives are to have class participants are able to:

- Understand the external memory interface options & how to choose one (eg. DDR/2/3, RLDRAM II, QDR II/+, SRAM)
- Implement the high performance controller and PHY (ALTMEMPHY or UniPHY) using the MegaWizard® plug-in manager
- Verify controller functionality with the ModelSim simulator
- Close timing on your design
- Connect your own logic to the High Performance controller
- Implement multiple controllers in a single FPGA

- Learn how to use the controller within SOPC Builder

## IV. Assessment of Industry Led courses

Assessment is a vital part of any curriculum reform and will help providing useful information for continuous improvements and determining if the overall objectives have been met. A rubric has been developed and used to assess the learning outcomes and evaluate the effectiveness of the Altera's courses. Faculty members are asked to rate on how well the course objectives were achieved on a scale of 1 to 5 with 5 being Strongly Agree and 1 being Strongly Disagree. Table 1 reflects a great interest of faculty members who were enrolled in Altera's training, they rated highly their overall experience as well as their willingness to recommend Altera's training to a colleague.

| **Course Objective** | **Overall Rate** |
|---|---|
| My knowledge and/or skills increased as a result of this course | 4.5 |
| The knowledge and/or skills gained through this course are directly applicable to my job | 4.5 |
| Overall I was satisfied with the course | 4.67 |
| Based on my experience with this course I am willing to recommend Altera training to a colleague | 4.75 |

**Table 1**: Altera's Training assessment results

## V. Electrical Engineering Technology Curriculum Revision

Figure 1 shows the current and the proposed digital design logic sequence based on faculty feedback who are enrolled in the Altera University program courses. Curriculum revision incorporates the addition of two new courses that will be added to the current course (Digital Electronics). The EET program will introduce two new courses (Digital Design Using VHDL and Topics in Programmable Logic). Each of these courses is three credit hours (2 class, 3 lab). The descriptions of the two new courses are provided below. The current EET program has a shortage of courses in digital logic design; only one course (Digital Electronics) is currently offered.

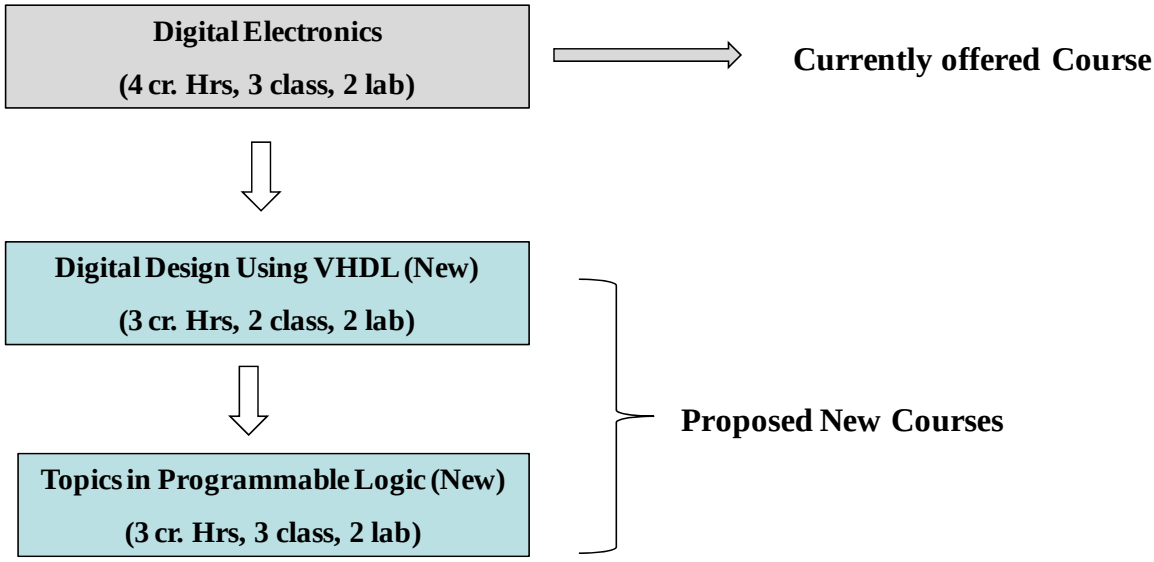


**Figure 1**: Proposed Digital Logic Design Courses Sequence

**<u>New Course 1: Digital Design Using VHDL</u> (3 Cr hrs, Class 2 hrs, Lab 2 hrs)**

**Course Objectives**

The course places an emphasis on the language concepts of digital systems design using Hardware Description Language (VHDL). The course will focus on good digital design practices and writing testbenches for design verification. Low-level gate modeling techniques with varying timing details will be presented, as well as structural level of abstraction for wiring predefined gates and other predefined components. The information gained can be applied to any digital design by using a top-down design approach. Students will gain valuable hands-on experience in writing efficient hardware designs using VHDL and performing high-level HDL simulations.

The academic objectives of the "Digital Design using VHDL" course are to provide students with skills and experience that will help them to be attractive in the job market and as employees with high-value skills in the workplace. The students will learn the design of major components of digital systems, such as arithmetic logic units (ALUs), floating points, memory, and controller using hardware description language (VHDL). In addition, the students will learn FPGA design flow starting from HDL design entry and circuit simulation to verify the correctness of the intended design, writing testbenches.

**Course Structure**

The course "Digital Design using VHDL" is three credit hours with two hours per week of recitation and three hours per week in the lab. The course will be open for sophomore or higher students and the pre-requisite is "Circuits I" and "Programming Languages". The course will integrate Altera's Quartus® II development software, and Modelsim®-Altera 6.5b [4].

**New Course 2: Topics in Programmable Logic Design ( 3 Cr hrs, Class 2 hrs, Lab 2 hrs)**

**Course Objectives**

Due to industry's increased demand for FPGA designers, the intention of this course is to give students real-world experience in FPGA logic design and give them the necessary training with design tools widely used in industry. Tools used will include Altera's Quartus® II development software and FPGA design implementation on Altera's DE2 FPGA evaluation board. The long-term objective of this course is to provide a learning opportunity that will result in research activities focused on FPGA design. This research will provide more in-depth training for senior students and engage undergraduate students in applied research opportunities.

The academic objectives of the FPGA logic design course are to provide students with skills and experience in the FPGA design process. The students will learn the FPGA design flow using Quartus® II [2] development software to develop an FPGA, starting from HDL design entry, circuit simulation followed by FPGA Synthesis for Altera FPGA devices, Place and Route and timing analysis.

**Course Structure**

The course "Topics in Programmable Logic" is three credit hours with two hours per week of recitation and three hours of lab. The course will be open to senior students and the pre-requisite is "Digital Design using VHDL". The course will integrate Altera's Quartus® II development software. The lab will use Altera's DE2 FPGA evaluation board, the FPGA boards will be used as target platforms for lab experiments. Students will learn how to implement a complete system on the FPGA evaluation boards.

**Relationship between EET Program courses and Altera's courses:**

Table 2 shows the relationship of the Altera's training courses and the proposed EET digital logic courses. Faculty members enrolled in Altera's training have now the knowledge and expertise to teach both VHDL digital Design and Programmable Logic (FPGA) design courses.

| Altera Training Course | Digital Design using VHDL proposed course | Topics in Programmable Logic proposed course |
|---|---|---|
| Introduction to VHDL | X | |
| Advanced VHDL | X | |
| The Quartus II Software Design Series: Foundation | X | X |
| The Quartus II Software Design Series: Timing Analysis | | X |
| Interfacing to External Memory with Altera FPGAs | | X |

**Table 2**: Mapping of Altera's Training to Proposed curriculum revision

## VI.Conclusion

The EET program digital logic design curriculum must be current and relevant to industry. This paper describes a new curriculum revision that is industry-driven. With the demand of skilled FPGA designers on the rise, the objectives of this paper was to present the curriculum development in Hardware Description Language and FPGA designed to meet the needs of

industry. The goals of this new curriculum revision are to give students a real-world experience on FPGA logic design and give them the necessary training with industry widely used design tools. A strong link between academia and industry has been established, this partnership is a "two-way street" and advantageous for both parties. The Electrical Engineering Technology program is collaborating with Altera's university program in which the involved faculty members enrolled in a set of training courses provided by Altera's university program. Results of training led to the development of two new courses in Digital logic design using VHDL and Programmable logic devices. Faculty members who attended these courses rated highly their overall experience as well as their willingness to recommend Altera's training to a colleague. The exposure to industry-taught courses helped the faculty members to impact the learning experience of undergraduate students by providing them with skills that are highly marketable and appreciated by industry.

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