AC 2009-2099: COLLABORATIVE PROJECT-BASED LEARNING TO ENHANCE FRESHMAN DESIGN EXPERIENCE IN DIGITAL ENGINEERING

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Collaborative Project-based Learning to Enhance Freshman Design Experience in Digital Engineering

Abstract

One great challenge for engineering education is to increase the retention rate for freshman and sophomore students. In 2008, CSULA received an NSF CCLI grant to redesign the Introduction to Digital Engineering course to enhance students’ interest in engineering by exposing them to fun hands-on in class projects. The proposed course redesign employs the Tablet PC-based Collaborative Project-Based Learning model (CPBL) that has been proven to be effective in our upper division computer engineering courses. This paper presents our current progress on the CCLI project. To study the impact of the CPBL model in freshman/sophomore level courses, a series of interactive in-class projects was developed that: 1) stimulate students’ learning and make them more engaged in the classroom; 2) tie the theory taught in class to real-world design experience; and 3) provide a clearer insight into possible engineering careers. So far five in-class projects using Verilog HDL design, simulation, and synthesis with Xilinx FPGA boards have been developed in our course redesign effort. In this paper, we will share our practice on how to incorporate the projects into the classroom instruction to deepen the students’ understanding of number systems, logic function simplification, and combinational/sequential logic design. In addition to focusing on a fundamental concept in digital design, each project progressively introduces different aspects of the design process. Preliminary assessment results are presented to show the impact of the in-class design project on student learning outcomes.

Introduction

In recent years, engineering design activities at the freshman level have become a common practice in many institutions across the U.S. It has been widely recognized by engineering educators that the capstone design experience itself is not sufficient for students to develop a thorough understanding of the engineering design process [1-3]. There have been numerous successful efforts in exploring efficient methods to integrate engineering design education into the first year curriculum in undergraduate programs [4-7]. According to Sheri Sheppard and Rollie Jenison’s study [8], one of the most important reasons for an increase in design practice at the freshman level is the “Recognition of Freshman Attrition.” A U.S. Department of Education (DOE) longitudinal study of undergraduate engineering programs pointed out that the retention rate during the freshman and sophomore years in an engineering program is much lower than that during the junior and senior years [9]. Although there are various reasons that lead to the high dropout rate during the first two years’ of engineering programs, a common one is that many students become so frustrated with the lengthy mathematics and physics sequence that they choose to give up even before taking the first engineering course. In this case, a fun and inspiring engineering design course at the freshman level not only contributes to the development of the students’ design skills from the early stage, but also helps stimulate the students’ interest in engineering fields to increase the retention rate.

Although the importance of freshman design experience has been well recognized, how to effectively embed it into the first year curriculum still remains a challenging task. A common
practice is to introduce a freshman design course where students learn how to design and create a simple working product. However, the impact of a standalone freshmen design course is usually limited and may fade quickly if not reinforced by other design-oriented courses. This problem is more significant at institutions that traditionally serve underrepresented and educationally disadvantaged minority students who tend to take a longer sequence of remedial math and English courses. In 2008, CSULA received an NSF CCLI grant to explore solutions to address the above problem. In our proposed project, real-world design experience is to be embedded in existing engineering courses at the freshmen and sophomore level to reinforce the effect of the first freshman design course (ENGR100). As a result, a pipelined curricular structure will be created to enhance students’ design skills progressively.

This paper presents our current progress on the redesign of our Introduction to Digital Engineering course (EE244), which is usually the first electrical engineering course taken by students after ENGR100. The Tablet PC-based Collaborative Project-Based Learning model (CPBL) is used to embed practical design experience into classroom instruction and reinforce students’ understanding of design principles learned in ENGR100. Our current course redesign effort focuses on the development of a series of interactive in-class projects to: 1) stimulate students’ learning and make them more engaged in the classroom; 2) tie the theory taught in class to real-world design experience; and 3) provide a clearer insight into possible engineering careers. So far five in-class projects using Verilog HDL design, simulation, and synthesis with Xilinx FPGA boards have been developed. In this paper, we will share our practice on how to incorporate the projects into the classroom instruction to deepen the students’ understanding of number systems, logic function simplification, and combinational/sequential logic design. In addition to focusing on a fundamental concept in digital design, each project progressively introduces different aspects of the design process. Preliminary assessment results are presented to show the impact of the in-class design project on student learning outcomes.

Project Overview

Digital engineering (EE244 at CSULA) is the logical place to introduce a design experience early into the electrical and computer engineering curriculum. The prerequisite knowledge for this required course is high school algebra. Further, at CSULA this course is one of the few lower division courses not offered at our major community college feeder, East Los Angeles College. Thus, we can provide a common design experience for most of our students, both freshman and transfer. Tablet PC-based Collaborative Project-Based Learning (CPBL) was developed by the authors in their previous education practice to enhance the design components in junior and senior-level engineering courses. Preliminary study [10, 11] has shown a positive impact on students’ learning outcomes. In this project, efforts have been made to adapt the model to a freshman level course, and new instructional technologies are being explored to maximize teaching effectiveness.

The main components of the course redesign are: Tablet PC-based dynamic lectures to more efficiently and effectively deliver course content; interactive in-class exercises using InkSurvey [12, 13] to collect student feedback to measure student learning and stimulate class discussions; integrated in-class design projects to progressively teach students about the design tools and process; and peer-facilitated workshops to reinforce and expand upon lecture material. Tablet
PC-based instructional technology has been proven to be helpful in improving the teaching efficiency in past educational practice [14, 15]. The successful implementation of the first two components allows the students to learn the course material more effectively in a shorter time frame, which makes it possible to add a design component in the same amount of instructional time.

Our current course redesign effort focuses on the development of a set of well-designed small projects to build the students’ knowledge and design skills step-by-step. Since a significant percentage of minority students are struggling with mathematics at the freshman year, they lack confidence in their ability to tackle engineering designs (even simple ones). Hence, our in-class project sequence starts from very simple design practice that is easy to understand and requires a relatively small amount of time to complete. The students can receive immediate help from the instructor since the project is conducted in class. In addition, peer-facilitated workshops are hosted to offer extra help to students in need. Eventually, the initial simple practice builds up to a real-world design with reasonable complexity. Through this process, the students can gain design experience as well as confidence that they can do engineering design, which will significantly benefit their future study.

In summary, the objectives of our CCLI projects are threefold: 1) Foster students’ skill in engineering design from the freshman level; 2) Stimulate students’ interests and increase the retention rate via a pipelined design experience; 3) Improve teaching and learning efficiency by highly interactive instruction using Tablet PCs. The redesigned EE244 class bridges the gap in the pipeline of design education between an introduction freshman engineering class (ENGR100) and upper division design courses in computer engineering curriculum, as shown in Figure 1. As a result, students can gradually acquire an increasingly in-depth knowledge of the design process and simulation/synthesis tools in step with their understanding of the theoretical course material.

![Design Pipeline](image)

**Figure 1. Building the pipeline to integrate design throughout the computer engineering curriculum.**
Tablet PC-based PBL in Digital Engineering

In this section, we will present the details of the in-class projects, as well as how Tablet PC-based CPBL was incorporated into the classroom instruction in EE244 in Fall 2008. We would like to share our experience about how to successfully embed project-based learning components in the tight 10-week schedule of a quarter system. In addition, we will also discuss the lessons learned in the implementation process.

1) Project Development Platform
The project development platform consists of two main components: a Tablet PC and a Xilinx FPGA development board. The Tablet PC is a very useful engineering design tool that allows the students to sketch their design and share their ideas with the instructor and their teammates easily. The Xilinx board is attached to the Tablet PC. The hardware interface was pre-configured to allow the students without prior knowledge to synthesize their design easily. Figure 2 shows the platform with a running project.

![Figure 2. Tablet PC-based project development platform.](image)

2) In-class FPGA Design Projects

While similar to digital laboratory courses that use FPGA boards, the in-class design projects are narrower in scope and have the goal of leading a student through the entire design process while reinforcing digital logic design fundamentals. In addition, the projects introduce students to the Verilog HDL and Xilinx ISE digital design tools for both behaviorally simulating designs and synthesizing them onto the Digilent Xilinx FPGA board. In subsequent quarters, students take a sequence of associated laboratories where they will explore in more detail the concepts of digital design and implementation through more in-depth laboratory experiments. Table 1 provides a summary of the in-class projects including the digital logic knowledge objectives, and the targeted design skills and tools.
Table 1. In-class Design Projects using Tablet PCs, Verilog, Xilinx ISE, and Digilent FPGA Board.

<table>
<thead>
<tr>
<th>Class Project</th>
<th>Knowledge Objectives</th>
<th>Design Skills and Tools</th>
</tr>
</thead>
</table>
| 1             | Number Systems and Waveforms  
• Binary, Hexadecimal, and Decimal  
• Signed and Unsigned Numbers  
• Waveforms  
  o Individual Signals  
  o Bundled Signals | Introduction to Verilog HDL and Xilinx ISE  
• Verilog syntax, wires, registers, and arrays  
• Xilinx ISE  
  o Projects  
  o Verilog Syntax Checking  
  o Running a Behavioral Simulation |
| 2             | Logic gates and DeMorgan’s Theorem  
• Logic gates: AND, OR, NOT, NAND, NOR, XOR, and XNOR  
• Truth tables and waveform equivalents  
• Logic diagrams and connection to structural modeling | Structural modeling in Verilog  
• Logic gate primitives  
• Interconnecting gates using wires (labels)  
Behavioral Simulation in Xilinx ISE  
• Creating test bench waveforms |
| 3             | Karnaugh Maps and a 7-Segment Display Decoder  
• K-maps for logic simplification  
• 7-Segment Displays  
• BCD-to-7-Segment Display Controller  
• SPDT switches | Synthesis in Xilinx ISE  
• Defining target device  
• Floorplan IO editor for pin assignment  
• Generating Programming Files for FPGA  
Introduction to Digilent BASYS FPGA Board  
• 7-Segment Display Control  
• Digilent Export software for programming FPGA device |
| 4             | Binary Adder/Subtractor  
• Full Adder, multiplexers, parallel adder/subtract  
• Overflow detection | Hierarchical Design and Test using Behavioral Simulation in Xilinx ISE  
• Step 1. Design and Test Full Adder  
• Step 2. Integrate Full Adder, multiplexer, and overflow detection to implement a 4-bit adder subtractor  
• Step 3. Create test cases for signed and unsigned addition and subtraction with and without overflow/carry |
| 5             | Simple Calculator  
• 4-bit adder/subtractor  
• 4-bit parallel load register  
• D flip-flops  
• 7-segment display controller  
• LEDs and pushbutton switches | Digital System Design and Test using Xilinx Synthesis tools and Digilent FPGA Board  
• Integrate 4-bit adder/subtractor, 7-segment display decoder, and flip-flop latches  
• Interface to SPDT switches for data input, push button switches for functionality (add, sub, clear, and signed/unsigned display mode), LEDs for binary output, and 7-segment display for decimal output |
3) Classroom Implementation

Class project worksheets and associated Verilog files were available for download from the class webpage. Worksheets included step-by-step instructions for implementing the projects. Using the Tablet PCs, students were required to illustrate their designs, capture and paste their Verilog code and simulation waveforms, and write their observations. At the end of each worksheet more in-depth questions were provided to probe the students understanding of the project and their knowledge of the underlying digital design fundamentals.

The class projects were designed to be completed within one 100-minute class period. Afterwards students had one week to submit their worksheets. During the five class periods, students worked on their designs independently but received help from the professor and their peers. If students needed additional time or help, they could attend a peer-facilitated workshop or the professor’s office hours. Students were also encouraged to install the Xilinx and Digilent software at home. While the Tablet PCs were only for in-class and workshop use, each student was assigned a Digilent Xilinx FPGA board for use in-class and at home. Due to software installation problems on some platforms, we have also installed the software in the college’s open access laboratories.

Figure 3 shows different learning scenarios in EE244 class. Tablet PCs provide an excellent platform for student-professor interaction. In Figure 3(a), the student was using InkSurvey [12] to do in-class exercise. InkSurvey allows the students to submit their handwritten answer anonymously, so the instructor can provide immediate feedback based on the submitted answers to reinforce the students’ understanding of the course material. In Figure 3(b), the student was learning about the functionality of the Basys Xilinx FPGA board by downloading and playing a simple “PingPong” game on the FPGA board. Accordingly to our classroom experience in Fall 2008, Tablet PC based PBL was effective to improve the teaching efficiency. As a result, we were able to cover the same course material although adding in-class project did cost some instructional time.

Figure 3. Tablet PC based PBL in EE244 classroom: a) Students use InkSurvey for interactive exercise; b) Students have fun with in-class project using FPGA board.
Preliminary Assessment

To evaluate the effectiveness of the course redesign and to quantify the impact of CPBL on student learning outcomes, assessment was conducted to collect the feedback from both the instructor and the students. Both direct and indirect measurements are used to achieve a comprehensive evaluation result.

**Direct measurements:**
- Scores on various course components such as projects, quizzes and exams are archived and compared to measure the students’ understanding of course material, their design ability and overall performance.
- Classroom observation/evaluation was performed to measure the students’ advancement in design ability exhibited by their in-class projects.

**Indirect measurement:**
- Pre and post survey has been devised to evaluate the change of the students’ learning attitude, their understanding of the engineering design process, and their efficiency in completing a real world design project.
- A focus group discussion was conducted by our external evaluator to collect the students’ feedback on various course components including Tablet PC-based dynamic instruction, in-class projects, interactive exercise, etc., as well as their recommendations for future improvement.

The assessment instruments were jointly designed by the PIs and the external evaluator. Table 2 lists a set of knowledge and skills that were evaluated by the pre and post survey. Analysis of the survey results reflects how well the redesigned course contributed to the development of the listed knowledge/skill set.

**Table 2. Knowledge and skill sets evaluated via pre and post surveys.**

<table>
<thead>
<tr>
<th>Concepts related to digital design</th>
<th>Skills</th>
</tr>
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<tbody>
<tr>
<td>1. Knowledge of engineering design process</td>
<td>1. General computing skills</td>
</tr>
<tr>
<td>2. Knowledge of computer simulation</td>
<td>2. Communication skills</td>
</tr>
<tr>
<td>3. Knowledge of design verification and testing</td>
<td>3. Math skills</td>
</tr>
<tr>
<td>4. Knowledge of binary number system</td>
<td>4. General design skills</td>
</tr>
<tr>
<td>5. Knowledge of binary calculation</td>
<td>5. Engineering design skills</td>
</tr>
<tr>
<td>6. Knowledge of logic functions</td>
<td>6. Ability to modularize the design process</td>
</tr>
<tr>
<td>7. Knowledge of Karnaugh-maps (K-maps)</td>
<td>7. Ability to design a digital component or system</td>
</tr>
<tr>
<td>8. Knowledge of adder, decoder or multiplexer</td>
<td>8. Ability to implement and verify a digital design using a simulation model</td>
</tr>
<tr>
<td>9. Knowledge of latches or flip-flops</td>
<td>9. Ability to implement a digital design in hardware</td>
</tr>
<tr>
<td>10. Knowledge of register or memory</td>
<td></td>
</tr>
<tr>
<td>11. Knowledge of FPGA (Field Programmable Gate Array)</td>
<td></td>
</tr>
<tr>
<td>12. Knowledge of Verilog HDL (Hardware Description Language)</td>
<td></td>
</tr>
</tbody>
</table>
Figures 4 and 5 depict the analysis results of the pre and post survey. In the surveys, students ranked their knowledge and skills using the sets listed in Table 2 (1- “None”, 2- “poor”, 3- “Fair”, 4- “Good”, 5-“Excellent”). From the comparison, we can see a consistent increase on the self ranking scores in the post survey for both knowledge and skills. Specifically, for knowledge set, the biggest improvement occurred on:
- Knowledge of Karnaugh-maps (K-maps)
- Knowledge of adder, decoder or multiplexer
- Knowledge of Verilog HDL (Hardware Description Language)

And for skill set, the biggest improvement occurred on:
- Ability to design a digital component or system
- Ability to implement and verify a digital design using a simulation model
- Ability to implement a digital design in hardware

It is encouraging to see that these knowledge/skill sets are exactly the focus of the learning objectives of our developed in-class project. However, the pre and post survey results showed relatively small improvement on general skills (computing, communication, math). This is expected since the development of these general skills requires a longer learning period via a variety of courses. In addition, the average rating of the general skills is quite high in the pre-survey, which leaves little room for improvement.

In general, the results of both direct and indirect measurements are very promising. Classroom observation showed that the students were more engaged in the learning process with the in-class design component. A preliminary analysis of the focus group discussion indicated that the in-class design projects were very helpful for them to develop a clear understanding of the design process and create a link between theory and engineering practice. We are still in the process of conducting a thorough analysis of the student portfolio as well as the focus group results. More quantitative and qualitative assessment data are expected to be available soon for a more comprehensive evaluation. The findings will be reported to NSF and be shared with colleagues in the near future.

![Result Analysis of Pre and Post Survey](image)

Figure 4. Comparison between Pre and Post survey results on knowledge related to digital logic design, simulation and synthesis (refer to Table 2 for knowledge sets).
Conclusion and Future Work

In this paper, we presented the current progress of the NSF sponsored CCLI project, entitled “Collaborative Project-based Learning to Enhance Freshman Design Experience in Digital Engineering”. Five in-class FPGA projects have been developed and implemented in EE244 class in Fall 2008. The projects not only reinforced the course concepts including number systems, K-map simplification and combinational/sequential circuit design, but also collectively fostered the student’s ability to conduct real-world design project. Preliminary assessment results shows that the impact of the course redesign on students’ learning outcomes is very promising. In our future work, more comprehensive assessment data will be collected and analyzed, and the findings will be used to further improve the course redesign.

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Reference


