Computer Architecture Design Project using Actual Air Traffic Control Specifications

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Abstract

Our computer architecture course includes the design of a system to solve a real world problem.

The system requirements and evaluation criteria are provided in a Request for Proposal (RFP). The class is divided into teams of four with equal numbers of Electrical Engineering and Computer Science majors. The problem chosen is to design a specialized, redundant computer to control individual messages sent to commercial aircraft via the radio frequency transponder link to the enroute aircraft in the United States.

Since the actual design involved a team of 175 engineers (managed by the author, when he was in the industry), it would be impractical for a team to do the detailed design. However, it is possible to do a top-level system design in response to a RFP. The RFP included specifications and costs for potential components such as computers, voting circuits, buses, and memory units. The teams are responsible for proposing a system block diagram, performing a reliability analysis, and calculating the projected cost.

The evaluation of the student proposals is similar to actual government evaluations of proposals - 40 % on cost, 50% on technical merit, and 10% on reliability achieved beyond the specified minimum.

The project provides training in the following areas:
- System Design
- Redundancy / Reliability Techniques
- Cost -Design tradeoffs
- Team Projects
- Oral and Written Presentation Skills

These areas are required for a high percentage of engineering positions, but often overlooked in many undergraduate engineering curricula.

Many of the student proposals submitted were very similar to the actual design. The benefits of a design problem based on an RFP response to an actual problem will be described.

Introduction

Since there is so much information to be taught in a computer architecture course, it is difficult to add a design element. The outline of the Boise State University course roughly follows the textbook by Hennessey & Patterson[1] with a design element added to the course. A design of a processor itself was rejected for two reasons. First, the level covered in a first course (parallel pipelining) is far from the complex super scalar designs being used in today's computers and second, the majority of students will be designing with computers as components as compared to designing the processor chips themselves.

Accordingly, we adapted an actual problem that a team of engineers had solved previously for the Federal Aviation Administration (FAA) - the Mode-Select (Mode-S) Enroute Air Traffic Control System. This problem was chosen for the following reasons:

- It could be solved in a number of different ways.
- It could be described by top-level blocks.
- It was a project previously managed and known in detail by the instructor.
- It required knowledge of redundancy and reliability to solve the problem.

Reliability is a key element in the design of a multiprocessor computer for critical applications. The normal way to achieve the high reliability is to use redundancy techniques. Therefore, in addition to introducing the basic elements of a computer, the fundamentals of redundancy are presented to the class.

The design project format selected was a request for proposal(RFP). The RFP is used for the following reasons:

- It is the most common way that programs or projects are awarded.
- The students become familiar with the RFP format & procedures.
- It allows for a competition between the teams and cooperation within the teams. Both are situations the student will commonly see in large projects.
- The format allows for costs to be a part of the criteria for winning the competition.

The criteria for the winning competition were was as follows:

- Technical Merit 50%
- Cost 40 %
- Exceeding reliability specifications 10%

A good technical approach to solving the problem was the primary consideration. The system had to work and could contain no critical flaws.

A common industry problem with many engineers is that they often do not consider cost a requirement as serious as a specification such as operating frequency or data rate. While this specification does not give cost as a requirement, it certainly introduces cost constraints to our

future engineers by giving cost a 40% weight. The cost weighting is high so that over-design solutions, for example, using massively redundant subsystems, would be penalized.

In addition, to spark innovation, extra points are awarded if the specified reliability could be exceeded, yet not cost a fortune.

This weighting scheme is similar to that used on most large competitive programs for government agencies. To make the competition as realistic as possible, we needed to have the winning team win big - something more than a few percentage points higher project grade. The solution – the winning proposal team is not required to take the final exam, and they receive the reward of an assumed better than average grade in the final.

System Description

Aircraft in the United States are controlled primarily by using a transponded radar signal. In such a system, a radar sends out a radio frequency pulse, the airplane receives it, amplifies it and returns it (transponds it) to the radar that sent it. In this way, the power of the radar pulses can be much smaller than that required for standard radar that returns a signal by reflecting a tiny fraction of the pulse energy. Before returning the pulse, the plane adds modulation to the pulse. The modulation information identifies the aircraft and its altitude. The air traffic controllers use these transponded signals to properly guide and separate the in-flight aircraft.

In 1984 the FAA issued an RFP requesting a major improvement to the guidance of aircraft in the USA. This improvement required the design of a system to a) send more information on the up-link to the plane by adding modulation to the ground radar pulse and b) add more information on the transponded pulse from the plane to the ground. The up-link modulation would be directed to the specific airplane and would contain information such as, turn left, use runway 270, or you are too close to the ground (just to make the reader feel better, this is accompanied by major audio warnings). The downlink information would contain the pilot's conformation of receipt of an up-link message, his altitude, the plane's identification code and other information such as current fuel reserves. This class of transponder operation is known as Mode-Select or Mode-S^2.

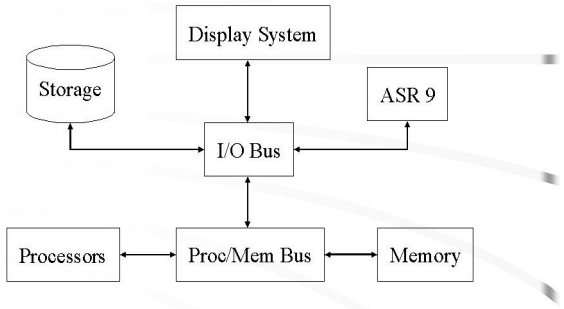

Figure 1 Mode-S System Overview

Figure 1 shows a diagram of the ground portion of the Mode -S system. The ASR 9 is the radar that encodes/decodes the digital information on to the radar pulses sent to the aircraft. The system design involves all the blocks except the ASR 9. The display system block represents the terminals that the air-traffic controllers use. The bus to the displays and the number of displays required are part of the design. A system for this critical function has to have extensive software development and a redundant, reliable computer. The portion of the program the author managed at Unisys was the development of the software, operating system, display systems and the computer hardware. Westinghouse developed the radar system. In the actual development at Unisys approximately 75 engineers worked on the hardware and 100 on the software. The team that responded to the RFP was composed of approximately 25 engineers.

This course uses a portion of the specification required to develop the redundant computer, and associated memory and interfaces. The size of the various modules of the software program is given as part of the specification. Originally the modules were items to be designed and developed. The student teams had to do a top-level design of a computer system with a very high mean time between failures (MTBF). The size of the computing requirements and the size of the processor module forced the actual system (and this class project design) into a multiprocessor solution. This was the approach taken in response to the government RFP in order to win the contract. The main topics in the RFP are shown in Table 1.

Section	Title
1	Scope
2	Quantity
3	Shipping (not used)
4.1	Software Specification
4.2	Hardware Specification
5	Basis of Award
6	Other (Rules for questions, bid submittal)
Appendix I	Component Specifications

Table 1 RFP Contents

The list of suggested components, reliability values, costs and specifications are given in Table 2 The restriction to use a given set of components is somewhat artificial, but it keeps the project focused on creative design rather than that of finding the latest components at a good price. The values used make the competing redundancy methods closer in cost, so many types of solutions are possible.

Component	**Specs**			3/12/99
Subsystem	Cost	Reliability	Specifications	Other
		Hours		
Memory	$4/ megabyte			
Processor	$1,000	40,000	300 Spec Marks	
Interconnect Bus	$100	80,000	100 MHz	
I/O Bus	$100	80,000	20 MHz	
Comparator Circuit	$10	1,000,000		Compares 2 inputs
Voting Circuit	$75	200000		Compares 3 inputs
Hard Disk	$100/Gbyte	60,000		
Display	$750	30,000		
Power Supply	$50	500,000	50 watts	
Power Supply	$200	300,000	200 watts	
Software	$20/ line of code		600,000 lines	
Software Testing	$75/ Hour		5,000 hours	
System Testing	$100/Hour		10,000 hours	

Table 2 Component Specifications, Costs, and Reliability

Course Content

The course outline follows closely the Patterson and Hennessy textbook.[1] By mid semester the students have been introduced to the following areas: Computer Performance, Instruction Sets, Arithmetic Hardware Units, Pipeline Processor Operation, and Memory Organization. At that time, basic reliability techniques are introduced in a module that includes the following:

- Reliability equation for long term operation.
- Redundancy without repair or replacement
- Redundancy with repair
- Methods to detect redundant units that have failed.
- Common redundancy techniques including Shadowed Memories, RAID Memories, Voting Circuits and Comparison Circuits.

The course then continues with Input/Output Processing and finishes with Multiprocessors including some of their corresponding interconnect schemes. A few examples of multiprocessor implementations are also included. With this background the student teams can make good progress and are predisposed to learn the upcoming multiprocessor information since it is rapidly becoming part of their project solution.

Design results

The student designs in the class were very good. The system block diagram showing the computers, memory and bus of the winning solution is shown in figures 2 and 3. The MTBF calculations and costs are shown for each segment. The SPEC Marks indicate the processing capacity of the computers and that they can handle the software programs.

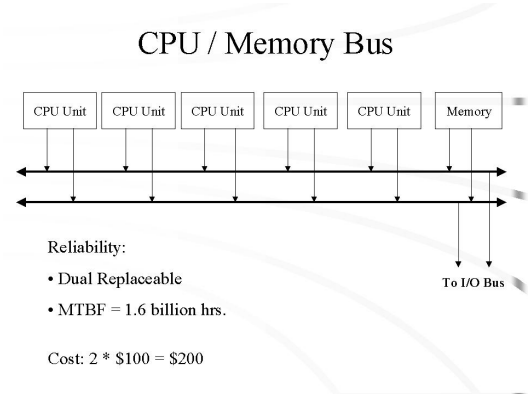

Figure 2 Five Processors on a Dual Bus

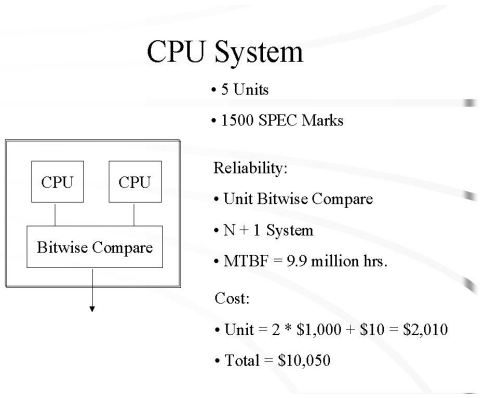

Figure 3 Shadowed Processor Pair

The solution uses a shadowed N+1 redundancy scheme. That is, if N computers are required to handle the processing load, then the extra one is used for redundancy. The problem is how do you tell if the N computers are operating properly? “Shadowed” implies that we take a pair of processors running the same software and compare the results. (The extra processor in each pair is the shadow processor.) If the results are identical, the data goes onto the bus; if not, that pair is considered a failure and the spare computer pair runs the software instead. This is, in fact, the solution used for the Mode-S systems that are in operation in the United States today.

Other student solutions used triply redundant circuitry and a voting circuit to determine the faulty processor. While this solution was valid, it is considerably more expensive and therefore did not win this competition. All the student team’s designs correctly eliminated any single points of failure that did not have an extremely high MTBF.

After calculating all the MTBF for the subsystems this team summarized the total system reliability and cost as shown in Figures 4 and 5.

System	Components	Qnt	Cost	Unit Totals
CPU/Mem Bus			**$200**	
	Interconnect Bus	2	$100	$200
CPU			**$10,050**	
	Processors	10	$1,000	$10,000
	Comparitor	5	$10	$50
Memory			**$1,040**	
	Memory (meg)	260	$4	$1,040
Mem-Option			**$68**	
	Memory (meg)	17	$4	$68
I/O Bus			**$1,000**	
	I/O Bus	2	$100	$200
	Bus Interface	8	$100	$800
Display			**$9,000**	
	Display	12	$750	$9,000
Storage			**$300**	
	Hard Drive	2	$100	$200
	Raid Controler	1	$100	$100
Power			**$300**	
	50 watt	6	$50	$300
Cost per system				**$21,890**
With ECC Option				$21,958

Figure 4 Costs

Reliability	lambda	MTBF	Lambda-S
CPUs			
Unit	5.0250E-05	19,900	
System	1.0100E-07	9,900,745	1.0100E-07
Memory	5.0000E-06	200,000	5.0000E-06
Mem-Option ~	5.0000E-06	400,000	2.5000E-06
Proc/Mem Bus	6.2500E-10	1,600,000,000	6.2500E-10
I/O Bus			
Unit	1.7778E-10	5,625,000,000	
System	1.3361E-09	748,440,748	1.3361E-09
Display	9.7778E-11	10,227,272,727	9.7778E-11
Storage	1.2611E-06	792,952	1.2611E-06
Power	2.4000E-10	4,166,666,667	2.4000E-10
	Total lambda		6.3642E-06
	Optional lambda		3.8644E-06
Total MTBF WithoutOption			157,130
Recommended System MTBF ~			**258,772**

Figure 5 System MTBF(hrs)

Educational Benefits

The RFP format and the award (no final) added a great amount of enthusiasm to the course. Without prompting by the faculty, the teams adopted business names and in most cases logos and slogans. An example from the winning presentation is shown in figure 6. This slide was done in PowerPoint in color, but reproduced here in black and white. The correlation between enthusiasm and educational value of a course is difficult to measure, but certainly positive. What is evident, is the time and effort that went into the designs.

Figure 6 Introduction slide by the **J²Q** team of **J**oe Hillard, **J**oe Coffland and **Q**uincy Holton

An objective of the project was to generate a real world experience. This was carried through by having the teams partially selected by management (the instructor) according to the suggestions of Felder and Brent[3]. This was performed to make sure there was an equal mix of electrical engineering and computer science majors on the 3 or 4 person teams. There were no adverse comments or complaints on the team mixtures.

The presentation and report training has been quite successful. All the presentations are made to the entire class as each team "pitches" their solutions. Every team member is required to participate. The written reports are evaluated according to the weighting discussed in the introduction.

As in a standard proposal after the initial dispersion of information, all questions on the project have to be in writing. The questions and answers then go to every team. This trains the engineers to be accurate in their questions and not to divulge a potential approach to the other teams.

The RFP method has a number of design training advantages. First, the very legitimate tradeoff of cost, reliability and technical design is forced by the RFP format. In other design classes there are no cost restrictions and the designs, while elegant, are often impractical. Out of nine teams only one had an overkill solution, the lack of overkill was attributed to the 40% evaluation on cost. Second, the design of a system is performed at a system level from sub-components. And third, the need to describe and clearly justify the technical approaches used is essential.

Summary

The RFP approach is very successful in including in a computer architecture course the following elements: Presentation skills, report preparation, teamwork, system design, cost tradeoffs, and reliability and redundancy. These skills are required on most large projects and are often not covered in detail in an engineering curriculum. This course also provides a fun, interactive way to introduce upper level students to skills needed in the workplace and to provide industry with well-trained graduates.

Bibliography

1. David A. Patterson and John L. Hennessy, "***Computer Organization and Design, the Hardware /Software Interface***", Morgan Kaufmann, San Francisco, CA, 1998.
2. Bruno Favennec and Yves Sagnier, "A Datalink that Meets the Requirements: Mode S***, Fourth European ATS Datalink Forum***, Nice, France, November 1996.
3. R. M. Felder, and R. Brent, ***National Effective Teaching Institute***, 2000.

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