

## **Demonstrating Motor Control using NMOS Exclusive H-Bridge Design**

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### Abstract

Delivering power to high voltage devices is a common requirement in an industrial setting. It is often required to be able to source current in two directions from the same supply. It is common to implement an H-bridge to supply power to these devices. An H-Bridge is a device with four switching elements that resembles a capital H. These devices are commonly configured with four transistors at the "tips" of the H and the load connected in the center of the horizontal "rung" of the "H." Depending on which of the four transistors is "on," current can be supplied to load in two different directions. This makes the H-Bridge a very useful tool in Industrial Settings.

In addition to being able to handle the high amount of current, ideally the H- Bridge transistors should have as little impedance as possible and as high a switching speed as possible. Based on these requirements N-type Metal Oxide Semiconductor Field Effect Transistor (NMOS) have a lower "on" resistance than P-type Metal Oxide Supplement Field Effect Transistors (PMOS) and thus are ideally suited for H-Bridge applications. Because NMOS devices require a voltage higher than that of the supply voltage, most H Bridge chips contain high side driver circuitry that is transparent to the user.

As an educational project the design of an NMOS exclusive H-Bridge was undertaken. This will implement simple circuitry and consist of common, easily obtainable components. This paper will demonstrate the design of the H Bridge and high side driver and will discuss, in depth, component choice, design considerations, and effectiveness of this particular circuit.

### 1. Introduction

Often in an industrial environment power must be delivered to high voltage devices. This may include as simple a task as turning on and shutting off power to the load, but may also require bi-directional control of power through the load. For this task an H-Bridge is often the desired solution. An H-Bridge is a circuit that contains four switches, in this case, transistors, which are arrange in the general shape of an "H" and can control current through the load. A basic H-Bridge circuit diagram is shown in Figure 1.

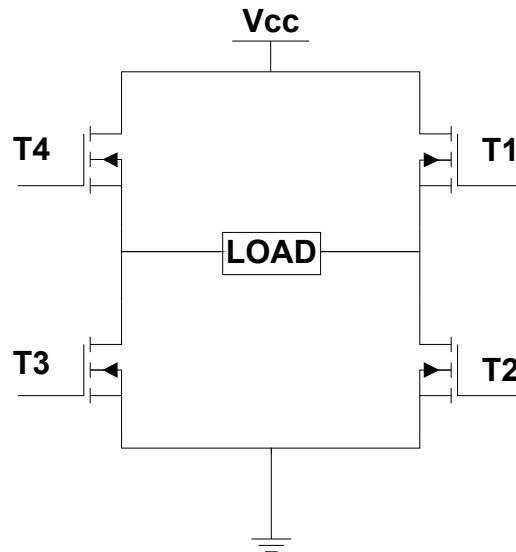


Figure 1. H-Bridge Circuit

The arrangement of the transistors in the circuit allows the H-Bridge to do any number of tasks including bi-directional current control, braking, and free-wheeling of a motor. This will be explained in further detail in the following sections.

Among the design considerations of an H-Bridge are the type of switches used. Since most industrial control is now done with microprocessors, MOSFET (Metal Oxide Semiconductor Field Effect Transistors) were chosen. NMOS (N-type MOSFETs) were chosen over PMOS transistors due to their higher efficiency. This necessitates the production of a high-side driver in order to drive the high-side transistors in the H-Bridge. These correspond to T1 and T4 in Figure 1.

Finally in order to avoid problems such as potential shorts between the supply and ground, there must be surrounding circuitry to protect the H-Bridge. The goal of this particular circuit is to implement a simple, cost-effective and robust design. This design will also be able to function fully when implementing pulse width modulation, PWM, in order to control the load. This will also be explained further in upcoming sections.

## 2. H-Bridge Fundamentals

The transistor arrangement on the H-Bridge allows for several modes of operation. As seen in Figure 1, an H-bridge has four transistors and four useful modes of operation based on which of the transistors is active and allowing current flow.

The two most common modes of operation allow current to flow from the source, through the load and to ground. Depending on the combination of active transistors on the high and low side, the motor will spin in both directions (T1 and T3 for one direction and T2 and T4 for the other). The current path is shown as the red line in Figure 2.

By switching all transistors off, the motor is said to be free-wheeling. In this state the motor will spin until all the energy in the system is dissipated due to shaft friction and windage. The current flow for this mode has exactly the same path as the first two modes, only opposite direction through the flyback diodes, which are not shown in Figure 2.

The final useful mode is the braking mode. This occurs when the two terminals of the motor are shorted together. In this mode the motor shaft slows down because the back EMF of the motor generates voltage across shorted terminals. While this mode is not considered for this application, future designs will implement a braking feature due to the necessity of this mode. Current flow in this mode is shown as the blue and purple lines in Figure 2, below.

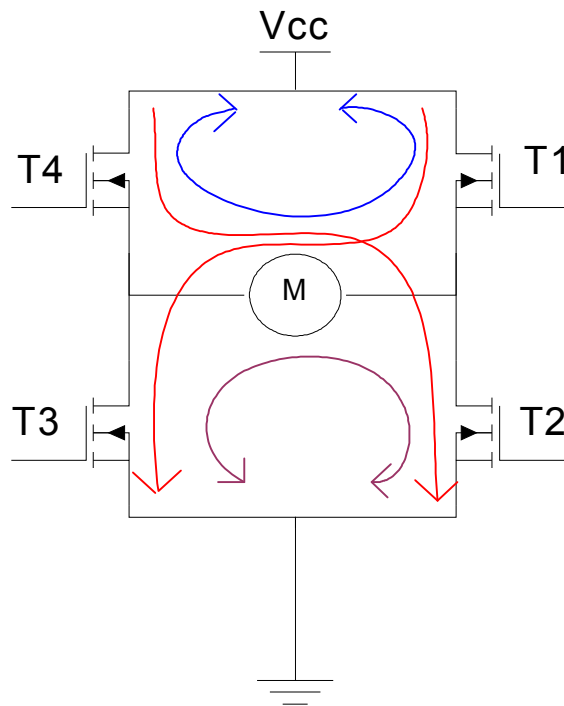


Figure 2. Current Paths in H-Bridge

### 3. Pulse Width Modulation

The speed of a DC motor is controlled by the voltage level that is applied to the motor's windings. For this reason, the motor can be controlled by simply varying the supply voltage with a variac or some other such device. This however wastes a great deal of energy through heat dissipation. This can be avoided by implementing pulse width modulation, or PWM.

PWM allows one to switch full power to the load a certain amount of the time. With an inductive load, such as a motor, this is ideal. The percentage of the cycle that power is being delivered to the load is known as the duty cycle.

With PWM, the only power losses are due to switching and are substantially less than regulating the DC power. This creates a far more efficient motor controller.

For this project we chose a switching (PWM) frequency that was greater than 30kHz, which would take it out of the audible range. Because the controller was to be controlled by a PIC chip, we chose 74kHz; a frequency easy to implement with the PIC chip..

#### 4. H-Bridge Design Considerations

The H-Bridge circuit must simply contain four switches that can be controlled as the user desires. The type of switch used is best determined by many factors including motor voltage rating, amperage rating, power supply, etc. In this case, the motor used was a linear DC motor with a max rating of 30 volts. A 15 volt, 3 Amp DC power supply was used. With minimal load at 15 volts, the motor consumed only 500mA of current.

In today's industrial setting, microprocessors control a great deal of equipment. Based on this fact, as well as the factors stated above, it was determined that the H-Bridge should be able to be operated easily by such a microprocessor, would include its own protection circuitry, and would be comprised of simple, economical and robust components.

These factors necessitated that the H-Bridge be able to be controlled with a TTL signal with a frequency of 74 kHz, as explained in Section 3. Since this signal was being produced by a microprocessor which are typically inadequate at sourcing current, voltage controlled FETs were used.

Due to the physical characteristics of NMOS devices, they dissipate less power than a PMOS device. By designing an NMOS exclusive H-Bridge, a more efficient circuit is created. However NMOS devices must have a gate to drain voltage,  $V_{GD}$  that is higher than its threshold voltage,  $V_T$  plus its gate to source voltage,  $V_{GS}$  in order to be fully active, a high side driver must be used to control transistors T1 and T4 in Figure 1.

Flyback diodes are placed into the circuit in order to allow current to flow when all the transistors are off. If these did not exist current would go to zero instantaneously, inducing a huge voltage in the motor that would destroy the transistors in the circuit.

In order to absorb the commonly occurring voltage spikes produced by switching the transistors, a high quality capacitor is placed on the input to the H-Bridge. This ensures that no voltage spikes are seen by the system and further protects the circuitry. This and the flyback diodes are shown in the full circuit schematic. See Appendix A.

#### 5. High Side Driver Circuitry

The high side driver must be able supply a voltage that it  $V_T$  volts greater than  $V_{GS}$ . In this

case the transistors used, National Semiconductor IRFZ14's, have a threshold voltage of 4 volts, worst case. This means that the high side driver must be able to maintain no less than 19 volts in order to switch the high side FETs.

A charge pump circuit was created to accomplish this. A charge pump can be compared to filling a bucket full of water. You use a small bucket and dump it into the larger bucket. As long as you dump the small bucket fast enough, the large bucket will stay full even if it is being emptied. The same applies to a charge pump, only instead of buckets, capacitors are used. This circuit is shown below.

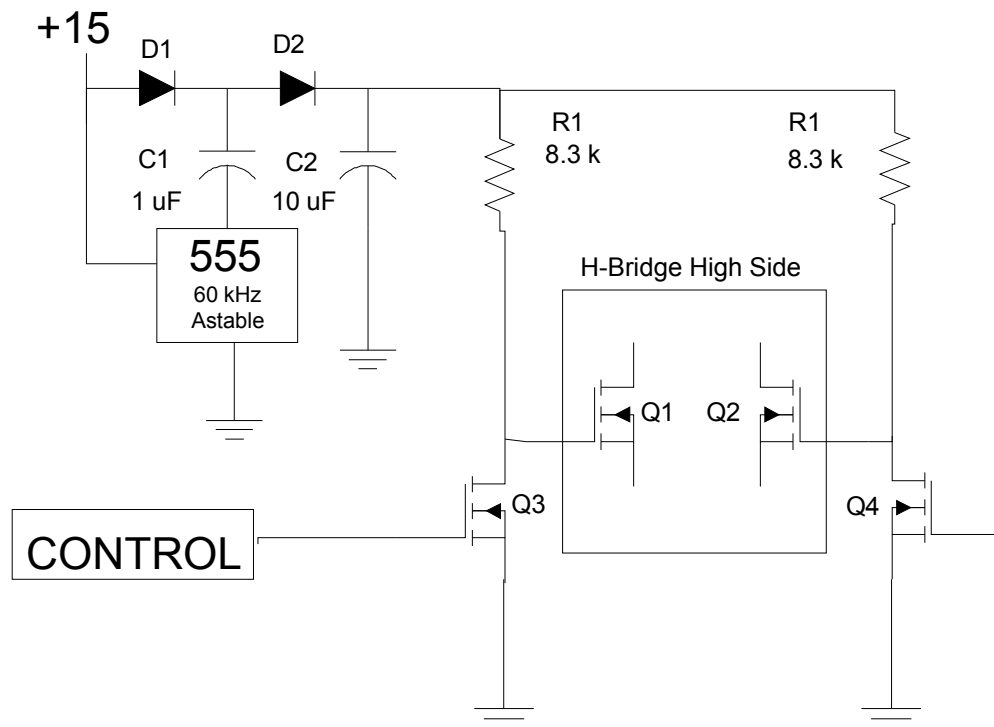


Figure 3. High Side Driver Circuit

The first stage of the charge pump circuit is a voltage doubler. For this, a National Semiconductor LM555 timer was operated in astable mode with 15 volt supply rails. This generated a 60 kHz, 15 volt peak square wave with nearly 50 percent duty cycle. This was used to drive a 1  $\mu$ F capacitor between 15 volts when the 555 signal is low, and 30 volts when high. This charge is then pumped through a switching diode into a 10  $\mu$ F capacitor. Both capacitors are tantalum due to their low loss characteristic. This will result in approximately 26 volts, due to diode drops, available to switch the high side FET's.

In order to ensure that the charge pump supply capacitor is not drained instantaneously through the FET when pulled low, a current limiting resistor is incorporated. However it is desirable to have as much current available as possible in order to overcome the gate capacitance in the highside MOSFET's. The IRFZ14 has an input capacitance of 300 pF.

A value of 3mA current drain is used. At 25 volts an 8.3 kΩ resistor is used to accomplish this.

Determining how much charge the charge pump is capable of producing, and also how much the remaining circuit will consume requires analyzing the circuit for charge rather than voltage or current.

First the amount of charge that is produced by the charge pump is calculated. Note this amount of charge is produced at a rate of 60k per sec.

$$\begin{aligned}q_1 &= C_1 v \\q_1 &= 1mF * 30V \\q_1 &= 30mC\end{aligned}$$

#### Charge Pump Analysis

Then the total amount of charge that can be stored in C2 is calculated. Note that the voltage on C2 is said to be 25 volts because of voltage drop across the diode.

$$\begin{aligned}q_2 &= C_2 v \\q_2 &= 10mF * 25V \\q_2 &= 250mC\end{aligned}$$

#### Storage of C2 Capacitor

In order for the high side driver to maintain the desired voltage of 20 volts, the amount of charge being produced must be at least equal to the amount of charge being drawn, and ideally the circuit should produce much more than is used.

The losses must now be calculated. Under steady state conditions the only charge being drawn will be due to the resistor in the current-sinking side of the drive.

$$\begin{aligned}q_{ss} &= \int i * dt \\q_{ss} &= \frac{25}{8300} * \frac{1}{60000} \\q_{ss} &= 50nC\end{aligned}$$

#### Steady State Charge Dissipation.

This calculation indicates that the charge dissipated by the resistor is 50nC while the charge being supplied by the charge pump is 30μC. This means that under steady state conditions, the circuit dissipates .17% of the charge produced.

Two other situations must be analyzed. When the circuit switches a high side transistor on, the gate of that transistor will consume charge. The total charge consumed in this case is the sum of the steady state charge consumption and the gate charge consumption. This is calculated below.

$$q_G = C_{G0}V$$

$$q_G = 300 \text{ pF} * 25V$$

$$q_G = 7.5 \text{ nC}$$

#### Gate Charge Dissipation

Now the total charged used is  $50 \text{ nC} + 7.5 \text{ nC}$  or  $57.5 \text{ nC}$ . This is still less than is being produced by the circuit.

Finally when the direction of the motor is changed, both high side transistors and brought low, which means the high-side driver supplies charge to each resistor. The total charge used in this case is simple two times the charge dissipated by one resistor, or  $.1 \mu\text{C}$ . Again this is much less than is supplied by the charge pump and thus has minimal effect on the circuit.

Next the speed of the gate charge is calculated. The gate voltage must go from zero to 20 volts to be “on.” The gate charging time is calculated on the following page.

$$V = V \left( 1 - e^{-\frac{t}{\tau}} \right)$$

$$20 = 25 \left( 1 - e^{-\frac{t}{8300 * 300 * 10^{-12}}} \right)$$

$$t = 4 \text{ mS}$$

#### Gate Charge Time Equation

A gate charging time of 4 microseconds is 29.6% of the 74 kHz PWM signal. This is an acceptable percentage of time since it takes at least one PWM cycle to switch states of the high side driver anyhow. Now 25 volts is available for switching the high side FET's in the circuit. These transistors must also be able to be shut off by applying a gate voltage of zero. In order to accomplish this, the transistors labeled Q3 and Q4 (Figure 15) are activated by the control circuitry to pull the high side transistor (Q1 or Q2) gate voltage to zero.

## 6. Control Circuitry

Certain conditions are undesirable in H-Bridge functionality. A dead short between supply and ground is extremely dangerous and is the primary concern of the drive circuitry. On a basic level the H-Bridge should use the direction bit to control which transistors turn off and on and should be able to turn them off and on based on the PWM signal. It was decided to design this circuit using 74 series digital logic devices because of their affordability, availability, and simplicity.

In order to simplify the operation of the H-Bridge, it makes sense that the high side transistor should stay active while the low side switches according to the PWM signal. This will simplify switching and reduce the amount of drive circuitry necessary for normal operation.

Also some consideration should be put into the fact that because the high side driver is operated with a NMOS which when active applies zero volts to the high side gates, thus shutting them off. This means that the logic controlling the high side drive must produce a logic low to turn on the high side gates.

The truth table for this circuit is shown in Table 1, below.

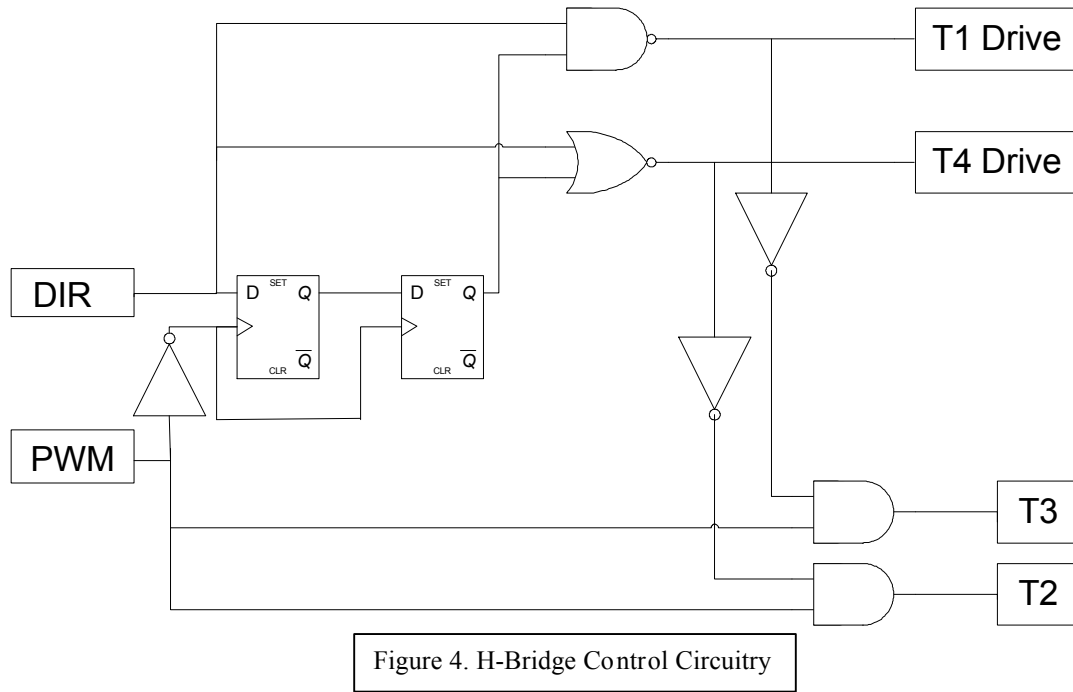
INPUTS		OUTPUTS			
PWM	DIR	T1	T2	T3	T4
0	0	1	0	0	0
0	1	0	0	0	1
1	0	1	0	1	0
1	1	0	1	0	1

As can be seen from the table, T1 is DIR inverted and T4 is DIR. T2 and T3 correspond to T4 and T1 respectively and are high with PWM. This is the desired characteristic. All that must be done now is to protect the circuit from shorting.

Because a direct short has devastating consequence to the circuit, the timing of switching must ensure no direct path from supply to ground. This is accomplished with a set of D flip-flops that will be clocked by the falling edge of the PWM signal. This feature ensures that on the first clock cycle that DIR changes, all the transistors are shut off, then on the following PWM cycle, the appropriate transistors are activated. The circuit's signal propagation time is far less than that of the clock, ensuring correct operation.



The final control circuitry is shown in Figure 4, below.



This design is further simplified by implementing NAND gates and inverters in order to create the digital logic shown in figure 4. This reduces the drive circuitry to two 74HC04 quad inverters, one 74HC00 quad NAND array, and one 74HC175 quad D flip flop array.

## 7. Conclusion

After connecting all the circuitry together and coupling it to the motor, the design was tested. The H-Bridge acted much like the similar one chip solution, National LMD18201. After extensive testing there was no sign of damage due to shorts and the transistors did not become hot at all. The design acted exactly as specified and incorporated low cost, readily accessible components.

The high side driver was able to maintain voltage enough to driver the H-Bridge even when switching. This is shown in Figure 5.

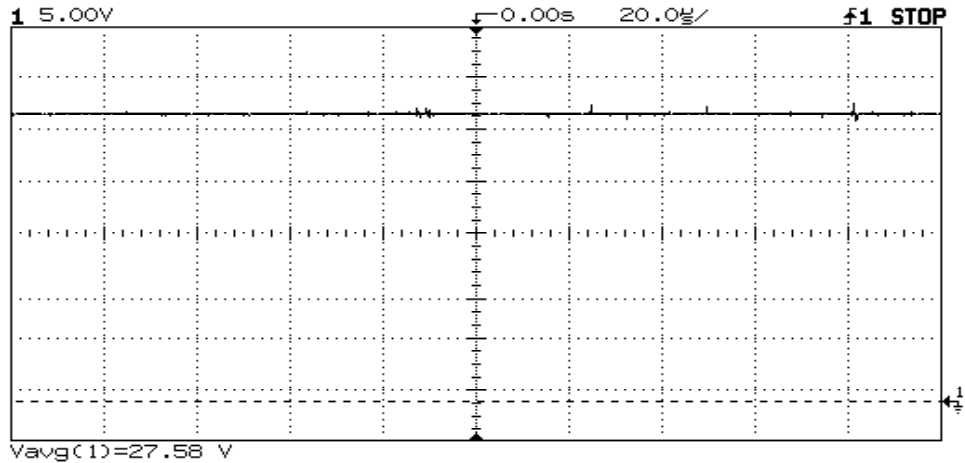


Figure 5. High Side Driver Output Voltage

Finally the operation of the H-Bridge control circuitry is shown in Figure 6. Note that there are no short conditions during the switching mode.

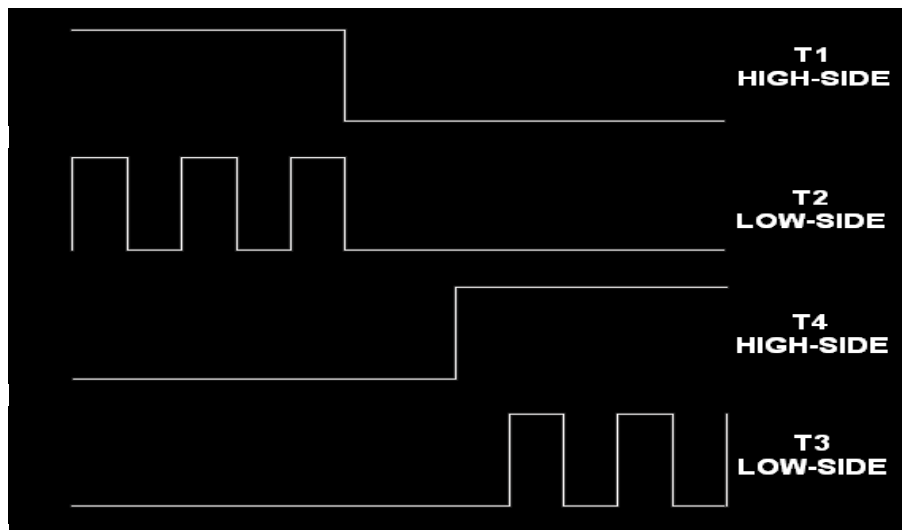


Figure 6. Control Circuitry Output

NMOS exclusive H-Bridge design has many benefits in a microcontroller based industrial setting including high speed, low heat dissipation and overall increased efficiency over BJT H-Bridges, PMOS H-Bridges and most other designs. The NMOS transistors are simply more efficient for this purpose.

The overall design of this particular H-Bridge is limited to no more than a 24 volt motor due to the limitation of the 555 to source 15 volts, maximum. In the automation industry many devices operate at a 24 volt DC level, making this design useful for those applications. The transistors are capable of handling 10 Amps of current and 60 volts with an “on” resistance of a mere 0.2 ohms. Redesigning the charge pump by replacing the 555

timer with a BJT and oscillator would allow larger voltages to be produced. This would allow for efficient and effective control of an even larger variety of industrial devices.

#### Product Data Sheet Reference

1. <http://www.irf.com/product-info/datasheets/data/irlz14s.pdf>
2. <http://www-s.ti.com/sc/ds/sn74f00.pdf>
3. <http://www-s.ti.com/sc/psheets/sdfs037a/sdfs037a.pdf>
4. <http://www-s.ti.com/sc/psheets/sdfs058b/sdfs058b.pdf>
5. <http://www.national.com/ds/LM/LMD18201.pdf>

#### BIOGRAPHY

##### MARCUS J. SOULE

Marcus J. Soule is a senior electrical engineering student at the University of Maine. He has worked as an Assistant System Administrator for the Electrical and Computer Engineering Department since September 1999. He has also acted as a Student Teacher for an introductory Electrical and Computer Engineering Class and is currently working for the Instrumentation Research Laboratory at the university.

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Bruce E. Segee is an Associate Professor of Electrical and Computer Engineering at the University of Maine. His research interests include Instrumentation, Automation, and Intelligent Systems. He is the Director of the Instrumentation Research Laboratory and a Member of the Intelligent Systems Group at the University of Maine. His work focuses on real-world deployable systems for use in manufacturing environments. Dr. Segee received his PhD from the Department of Electrical and Computer Engineering at University of New Hampshire in 1992.

# APPENDIX A

## Full Circuit Schematic

