

Demonstration of the Benefits of Asynchronous vs. Synchronous Circuits

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Abstract— Asynchronous circuits hold several advantages over synchronous designs. Currently, the asynchronous technology field is small, but it is expected to grow significantly over the coming years. Hence, it is important to show the advantages of asynchronous designs to help aid its growth. Asynchronous circuits display tolerance to temperature and supply voltage variation. A direct comparison of these attributes can be shown by having a synchronous and an asynchronous microprocessor play a song and then introduce various stresses. Under testing the asynchronous microprocessor sped up when introduced to cold and slowed down when heat was applied. Lowering the supply voltage caused the asynchronous microprocessor to slow down. The synchronous processor failed in all cases.

Keywords— asynchronous circuits; NULL Convention Logic (NCL); voltage scaling; temperature variation

I. INTRODUCTION

Asynchronous circuit design is currently a small, but growing field. The International Technology Roadmap for Semiconductors (ITRS) has documented the growth of asynchronous designs and expects continued growth in the future. Showcasing the advantages of asynchronous technology is important to its growth. This paper describes a simple experiment to demonstrate the robust and tolerant nature of asynchronous circuit designs.

The basic concept of the experiment is to compare the ability of two microprocessors, one asynchronous and one synchronous, to play a song while put under stresses. The song allows observers to detect the speed of the program execution and note when the microprocessor fails. This method provides an easily observed, direct response from the microprocessors as stress is introduced and gradually increased.

II. PREVIOUS WORK

A. Asynchronous Logic

For the last three decades the focus of digital design has been primarily on synchronous, clocked architectures. However, as clock rates have significantly increased while feature size has decreased, clock skew has become a major problem. High performance chips must dedicate increasingly larger portions of their area for clock drivers to achieve acceptable skew, causing these chips to dissipate increasingly higher power, especially at the clock edge, when switching is most prevalent. As these trends continue, the clock is becoming more and more difficult to manage, while clocked circuits' inherent power inefficiencies are emerging as the

dominant factor hindering increased performance. These issues have caused renewed interest in asynchronous digital design. Asynchronous, clockless circuits require less power, generate less noise, and produce less electro-magnetic interference (EMI), compared to their synchronous counterparts, without degrading performance. Furthermore, delay-insensitive (DI) asynchronous paradigms have a number of additional advantages, especially when designing complex circuits, like Systems-on-a-Chip (SoCs), including substantially reduced crosstalk between analog and digital circuits, ease of integrating multi-rate circuits, and facilitation of component reuse. Asynchronous circuits can even utilize a synchronous wrapper, such that the end user does not know that the internal circuitry is actually asynchronous in nature.

DI systems are very tolerant of power supply variations, allowing cheaper power supplies to be used and voltage to be dramatically reduced to meet desired performance while decreasing power consumption. Therefore, a very fast DI circuit can be run at a lower voltage to reduce power consumption when high performance is not required. Other DI advantages include tolerance of vast temperature differences, making these circuits well suited for operation in harsh environments, like outer space, and easing the difficulty of integrating designs with non-harmonically related clock frequencies. Their main disadvantage is increased area, which is approximately 1.5 – 2 times as much as an equivalent synchronous design when using static CMOS gates, but less for semi-static CMOS gates. However, for large designs, such as SoCs, the processor core(s) normally require(s) less than ½ of the chip's total area, while the rest of the chip area consists of flash, cache, RAM, peripherals, etc., which are the same in both DI and synchronous implementations. Therefore, the increased area for the DI implementation of the processor core(s) is less significant, especially considering the increased robustness and numerous other advantages [1].

B. NULL Convention Logic

NCL is a delay-insensitive (DI) asynchronous (i.e., clockless) paradigm, which means that NCL circuits will operate correctly regardless of when circuit inputs become available; therefore NCL circuits are said to be correct-by-construction (i.e., no timing analysis is necessary for correct operation). NCL circuits utilize dual-rail logic to achieve delay-insensitivity. A dual-rail signal, D , consists of two wires, D^0 and D^1 , which may assume any value from the set {DATA0, DATA1, NULL}. The DATA0 state ($D^0 = 1$, $D^1 = 0$) corresponds to a Boolean logic 0, the DATA1 state

($D^0 = 0, D^1 = 1$) corresponds to a Boolean logic 1, and the NULL state ($D^0 = 0, D^1 = 0$) corresponds to the empty set meaning that the value of D is not yet available. The two rails are mutually exclusive, such that both rails can never be asserted simultaneously; this state is defined as an illegal state. Dual-rail signals are space optimal 1-hot delay-insensitive codes, requiring two wires per bit [2].

III. EXPERIMENT DESIGN

A. Hardware Design

The microprocessors used are both from the 8051 microprocessor family. The commonly available 8051 is used for the synchronous processor. For the asynchronous processor, an 8031 design is used. The only major difference between the 8051 and 8031 is that the 8031 lacks the internal programmable read-only memory (PROM) of the 8051. The 8031 circuit contains an off-chip PROM. This factor causes the 8031 supporting circuitry to be slightly more complex than the 8051 circuitry.

The 8031 uses a parallel interface for external memory. The parallel PROM is connected to port 0 and port 2 of the 8031. Port 0 functions both as the lower address byte for the memory location as well as the data byte. This necessitates the use of a latch. The lower byte of the memory address is stored in the latch so that the data byte can be read or written using port 0 on the 8031. The PROM also requires the use of a Phase Locked Loop (PLL) Clock Multiplier since the PROM is not asynchronous. The PLL takes a sine wave from a crystal oscillator and transforms it into a square wave at a higher frequency.

The asynchronous processor is connected to a different voltage supply than the rest of the components. The independent power source allows the voltage to be scaled on the processor without affecting the operability of the rest of the devices in the system.

Both the synchronous and asynchronous circuits are both programmed to output a song as a square wave. This output is sent to a simple RC low pass filter and then fed into an operational amplifier. The filter removes some of the high frequency noises that are inherent in square waves. The amplifier takes the signal and boosts it to a voltage level that is capable of driving a small speaker. The processors do not supply enough power from their output pins to drive a speaker.

The 8051 circuit does not contain a PROM, latch, or PLL. This is because the 8051 has an internal PROM. Since the PROM is internal, the circuit instead contains a MAX232 chip. The MAX232 chip converts Transistor-Transistor Logic (TTL) voltage levels to RS-232 voltage levels. A computer's serial interface uses RS-232 voltage levels. The 8051 has a serial interface to allow the PROM to be programmed directly from a computer.

B. Software Design

The software works by outputting a square wave. The frequency of the square wave is changed to create different notes. The frequency and duration of a specific note are controlled by delay loops. Delay loops are created by changing the value of the output pin then having the processor perform

no operation (NOP) commands, which idle the processor for one clock cycle. This is used to create square waves of various frequencies to make notes and to control how long each note is played. The main function of the code calls different notes for different amounts of time creating the song. Since asynchronous circuits do not have a clock, the amount of time to complete a delay loop must be experimentally determined.

C. Experiment Execution

Three different stresses are applied to the microprocessors. The first stress is supply voltage variation; the second stress is excessive heat; and the third stress is excessive cooling. The possible outcomes include the processors not changing, slowing down, speeding up, or failing entirely. In the cases of slowing down or speeding up the pitch of the notes will also lower or raise, respectively.

The first test scenario is performed by connecting each processor to a variable voltage supply. The voltage is then lowered while the processor is playing its song. The second test is performed by taking a hot air gun and aiming it directly at a processor while it is playing its song, making sure to not heat up any of the other components near it. The final stress is introduced by pouring liquid nitrogen on the processor while it is playing its song, making sure the liquid nitrogen does not come into contact with the other components.

IV. RESULTS

For the supply voltage test, the nominal voltages are 5V for the 8051 and 3.3V for the 8031. Once the supply voltage is lowered to 4.1V the synchronous processor stops playing the song and resets when the voltage is again increased. The asynchronous processor's voltage can only be lowered to 2.4V. At 2.4V the supply voltage is being sourced from an internal node allowing the Vcc pin to be completely disconnected without stopping the song. The song plays continuously during the entire test, slowing as the voltage drops and returning to normal pitch as the voltage is restored to 3.3V.

The two different processors performed as expected during the temperature variation tests. The 8051 failed when it got too hot or too cold. The 8051 would reset as the temperature re-approached room temperature. The 8031 slowed down when heat was applied and sped up when it was cooled. As the 8031 returned to room temperature the song would return to normal speed and pitch.

V. CONCLUSIONS

The synchronous and asynchronous processors performed as expected. The synchronous processor failed under all the test conditions, while the asynchronous processor continued to function. The results show the robustness of asynchronous technology, demonstrated in a clear, easy to observe fashion.

VI. BIBLIOGRAPHIC INFORMATION

Justin Roark is a MS student in the Department of Computer Science and Computer Engineering at the University of Arkansas; he graduated with his BSEE from University of Arkansas in 2011.

Scott C. Smith is an Associate Professor of Electrical Engineering at the University of Arkansas. He received his PhD in Computer Engineering from University of Central Florida in 2001, a MSEE from University of Missouri – Columbia in 1998, and BSEE and BScPE degrees from University of Missouri – Columbia in 1996.

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Abstract

- Asynchronous Technology
 - Lower power, less noise, less electromagnetic interference
 - Eliminates need for a clock
- NULL Convention Logic
 - Delay-Insensitive
 - Tolerant to supply voltage, temperature, and fabrication process variation
- Compare Asynchronous vs. Synchronous Microprocessor
 - Clearly and simply demonstrate asynchronous advantages
 - Have both processors play a song
 - Heat, cool, and lower supply voltage to add stress
 - Variations in song speed and pitch indicate changes in processor performance
 - Asynchronous processor continues to function in each test case while synchronous version fails

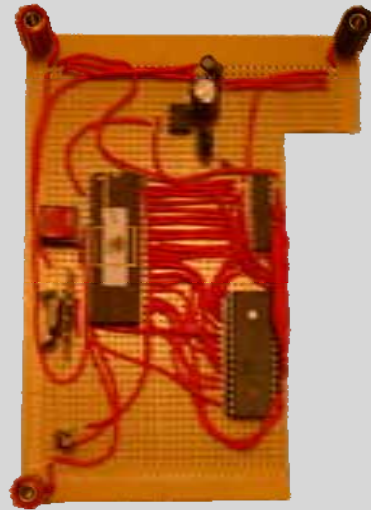
Experiment Design

- Each microprocessor plays a song
- Heat processors with a hot air gun
- Cool processors with liquid nitrogen
- Lower supply voltage with variable voltage supplies

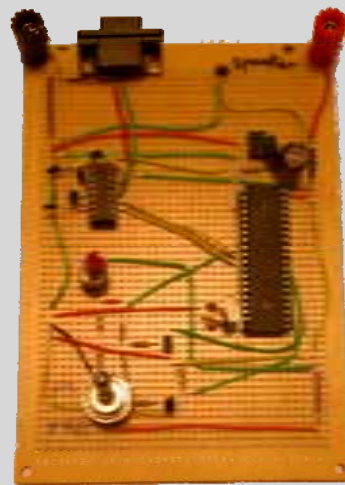
Software

- Outputs song as square wave
- Uses delay loops to create different notes
- Asynchronous delay loops are based on experimentally determined average case

Breadboard Layouts

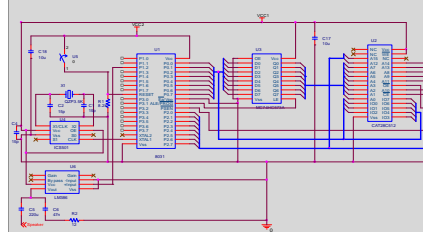


Asynchronous 8031 Microprocessor and Supporting Circuitry on Breadboard

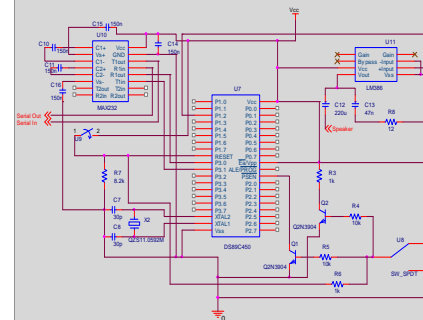


Synchronous 8051 Microprocessor and Supporting Circuitry on Breadboard

Schematics



Schematic for Asynchronous 8031 Microprocessor and Supporting Circuitry



Schematic for Synchronous 8051 Microprocessor and Supporting Circuitry

Hardware

- Asynchronous 8031 Microprocessor
 - Needs external PROM
 - Latch, PLL, and oscillator support the PROM
- Synchronous 8051 Microprocessor
 - MAX232 for serial connection to computer
 - Crystal Oscillator for internal clock
- Both
 - Op Amp to power speaker
 - Low Pass Filter

Conclusion

- Asynchronous microprocessor continued to function in all test cases, varying the speed of the song
- Synchronous microprocessor failed in each case causing the song to stop playing
- The tolerant nature of asynchronous technology is clearly displayed

References

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Results

	Heating	Cooling	Supply Voltage Drop
Asynchronous	Slowed Down	Sped Up	Slowed Down
Synchronous	Stopped	Stopped	Stopped

Effect on the Song by Various Stresses

Acknowledgements

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