Design, Simulation and Testing of MOSIS Fabricated CMOS Operational Amplifiers for Class Projects in an Analog I.C. Design Course

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Abstract

The paper describes use of MOSIS fabricated CMOS Operational Amplifiers as a real world design experience in senior level Analog Integrated Circuit Courses in Electrical Engineering. In the one-semester course on CMOS Analog I.C. Design offered at our department, design of a CMOS Operational Amplifier is required as a term project. Students are given a set of minimum specifications and are required to apply the learning they had into the design of a NMOS-input Operational Amplifier that can be implemented in an N-well CMOS process. The specifications include open loop gain, gain-bandwidth product, phase margin, common-mode rejection range, slew rate and output swing on a specified load including capacitive loading. The requirements are (1) to create a Mathematica file of their design calculations, (2) verify the design with appropriate SPICE simulations, (3) create a layout design that passes all design rules, and (4) write a report and do a Powerpoint presentation to the class at the end. Projects that pass the design specifications and layout rules can be sent out to be fabricated. However, typical turn-around times do not allow the graduating class to have a chance to test and verify their design, and get the satisfaction and the real world experience of testing. By using MOSIS fabricated designs of previous generations, this missing link was completed.

1. Introduction and Background

The paper describes how MOSIS fabricated CMOS Operational Amplifiers are used as a real world design experience in a senior level Analog Integrated Circuit Course in Electrical Engineering at the University of Southern Maine.

Design is an ABET requirement that every engineering student should experience before graduation. Although this experience can be left to the capstone project most engineering programs require, considering the diversity of electrical engineering disciplines, it is desirable that the design experience be incorporated into individual courses particularly those at the senior level. This ensures that the design experience and exposure is not limited to the narrow topic of the student's capstone project. Implementing it in the senior level courses makes it possible that a level of sophistication and depth can be demanded and achieved based on an accumulation of learning and experimentation from at least three years of prior engineering education.

"ELE444 Analog Integrated Circuits" is a senior level elective in our Electrical Engineering undergraduate program. Another title "CMOS Analog IC Design" is interchangeably used to highlight the fact that "design" is emphasized in this course. As a matter of fact the junior electronics courses (ELE342 and ELE343) constituting prerequisites for this course also emphasize design but at a smaller scale and using discrete BJT and off-the-shelf ICs rather than at the chip level using CMOS technology. This emphasis on "design" in our electronics sequence of courses has been implemented starting with an NSF grant to establish and develop a "Computer-Integrated-Electronics" Laboratory (C.I.E. Lab) in the early 1990's. The concept of "Computer-Integrated-Electronics Laboratory" simply brings computers into the electronics lab where designs implemented are tested for verification. Availability of PC-based

computational and graphics software along with inexpensive circuit simulation tools like "PSpice" has transformed the electronics lab into a design room where concepts and formulas can be turned into mathematical design calculations to determine component parameters, and where the circuit can be drawn and simulated in the same room to verify the design before building it on a proto-board and testing it. Furthermore, availability of GPIB interfaced test instruments and control and data acquisition software made fast, automated measurements and tests be performed for a quick turn around to check if the design met the design specs and, go back to the design calculations for corrections, modifications and iterative improvements on the spot. We achieve automated testing and measurements with software programs developed in our laboratory. Our "CIE-IV" program automates I-V measurement of device characteristics. I-V data gathered with automated measurements of the diodes, BJTs and FETs used in our laboratories help to extract their SPICE parameters for self-consistent simulation. CIE-IV program can also be adapted to measure Vout-Vin DC transfer characteristics of a circuit including DC coupled amplifiers and logic gates. Our "CIE-Bode" program automates frequency response measurements by stepping the frequency of a sine-wave generator over a specified range and employs oscilloscope readings to determine amplitudes and phase difference between the input and output of a circuit or amplifier at each frequency step. The data collected is used to generate Bode Magnitude and Bode Phase plots of the frequency response. More information about the C.I.E. Lab., the equipment and the software, automated Bode and I-V measurements and SPICE parameter extractions made with them can be found in the papers published earlier. [References 3-5]

For integrated circuit and MEMS layout design a PC-based "L-Edit" layout tool by Tanner is used. Availability of a student version, which comes in a textbook[2], makes this tool extremely convenient particularly for the commuting and part time students. Similar credit goes to MicroSim for making PC-based "PSpice" available to the public. Freely downloadable student versions of PSpice have become the indispensable tool of electronics education throughout the world. "Mathematica" is the default computational tool used in the Electronics courses mentioned above. As a matter of fact, thanks to another NSF grant received in mid 1990's it became integrated in our Electrical Engineering curriculum and it is used extensively in most of the courses we deliver. Having such a standard computational tool gives the student long enough a time to become a competent user and saves time from training particularly in the higher level courses where course-specific tools have to be introduced.

2. Description of the Course

The Analog Integrated Circuits (="CMOS Analog IC Design") course has the goal to introduce principles of operation, fabrication technology and design of analog integrated circuits to Electrical Engineering students at the senior level. VLSI fabrication is introduced with an emphasis on Silicon CMOS Technology. Starting with device physics and modeling of MOS devices, analysis of building blocks of analog integrated circuits such as differential, trans-conductance and high-gain inverting amplifier stages, current and voltage references and biasing circuits are completed to serve as a mathematical basis for engineering design of more complex circuits such as operational amplifiers, comparators, sensor interface and D/A converters. Concepts related with feedback, stability, phase- and gain-margins and frequency compensation techniques are discussed. CMOS layout design (L-Edit) and analog simulation tools (PSpice) are demonstrated and used extensively.

Two textbooks are used: Allen and Holberg's[1] serves as an excellent textbook with mathematical analysis and a reference book for the topics covered. Uyemura's[2] serves as a source for CMOS technology, layout design and design rules. Uyemura's book contains student version of L-Edit and it serves as a manual for the layout design software.

Grading is based on two exams, quizzes and homeworks, and a term project (design project).

Students are required do a design project, complete with mathematical calculations, SPICE verifications and design-rule-checked (DRC) layout, and present it to the class with a power point presentation at the end. The designs which are fully completed in time and satisfying all the specified design criteria (deemed "worth fabrication") are combined as a "multi-project chip" by the instructor for fabrication at a later time using the MOSIS fabrication services.

3. Design Project: Description and Specifications

The term project assigned is chosen to include as much of the topics covered as possible, while taking into accounts the time left in a semester and limitations of the student versions of the tools available. For this reason a CMOS OpAmp design using a 2 micron N-well CMOS process became the standard and default project over the years. Below is copy of a handout given to the students that gives details of project specifications and outcomes. It has been reformatted to comply with the paper's format.

CMOS Operational Amplifier Design

Design a CMOS Operational Amplifier that satisfies the specifications listed below.

Submit,
1. Mathematica Design File: A file including all steps of the design procedure used, i.e. starting from a set of design specifications, and using, in a logical sequence, design equations, assumptions, approximations and calculations leading to the choices made of all transistor and capacitor W/L ratios as well as their operating point values. MathCad is also acceptable. Students are free to choose the software tool they prefer to use as long as the instructor is notified of the choice (and the version) of the software at the beginning so that the instructor can read and run the file.
2. A set of MicroSim PSPICE schematics files (*.sch) and PROBE plots verifying the design specifications are met. (see 4 below)
3. LEDIT layout which passes DRC and generates a SPICE netlist that verifies consistency with the schematics and W and L values verified earlier with SPICE simulations. This step is crucial to determine if the design is ready (worth) to be sent out and fabricated on Silicon.
4. Report (document) file including "Discussions and Conclusions" and highligthing the results obtained, presenting them clearly and consicely using figures, charts and tables and describing and making comments on the successes/failures and suggested/implemented improvements. ". PROBE plots can be screen captured and pasted into this document. (For writing this document students are expected to use MS Word/Office which is available on C.I.E. Lab's computers but Mathematica or MathCad is also acceptable.)
The primary criterion for high achievement is the gain-bandwidth product (or the unity gain frequency) with maximum load while satisfying the stability and other specifications listed below.
Exceeding some of the specs marked on the list will be rewarded with extra "bonus" points.

Design Specifications

Process:	MORBN20 (2 um N-Well CMOS Process)
	(use the SPICE SCNA models given for this process)
Supply Voltage:	+/- 5 VDC dual supply
Supply Current:	≤ 300 uA Quiescent
Load:	$R_L \geq 50$ K, $C_L \leq 50$ pF
Output Voltage Swing :	≥ +/- 2.5 V
Stages:	≥ 3 (including a source follower output stage)

Compensation:	Internal Capacitance (students are free to choose any method/circuit)
Unity Gain-Bandwidth Freq:	≥ 0.5 MHz (Bonus for higher values)
Phase Margin:	≥ 45 degrees (Bonus for better values)
Differential Gain:	$\geq 10^4$ (preferably $\cong 10^5$)
Common Mode Range:	$\geq$ +/- 2.5 V (Bonus if one extends to the rail)
Slew Rate:	≥ 0.5 V/us overall with load capacitance
Layout :	Inputs on the left, Output on the right and Rails at the top and bottom
Area:	$\leq$ (500 um x 500 um)
Terminals:	Maximum six including an external bias (all labelled)
Bias:	External resistance or external current source delivering 10 uA to NMOS current mirror reference on the chip.

Include in the SPICE tests:
1. Output voltage versus differential input voltage dc transfer characteristics, both loaded and unloaded. Extract maximum gain, input offset voltage and output swing with minimum load resistance.
2. Output voltage versus common mode input voltage to determine the common mode range (unloaded).
3. Small signal ac response (open loop) with the offset voltage corrected. Extract the maximum gain, output resistance, GBW, phase margin, gain margin.
4. Transient response with a square wave signal large enough to drive the output to its maxima. Extract the slew rate and the maximum ac swing.
5. Submit the layout file and the DRC results.
6. You may check relative grading points assigned to these tests by downloading and reading
   "Project-Evaluation-44407.pdf" file.

4. Design Project: Samples of Design work and Spice Verifications

Figure 1 shows a typical NMOS-input CMOS Operational Amplifier circuit employed in the design projects. It is a 3-stage design comprising a differential input single-ended output differential amplifier, followed by a DC-coupled high-gain inverting amplifier, and the last stage, a source-follower unity gain buffer output stage for low output resistance and improved drive capacity to meet the slew rate and output swing requirements on the 50K // 50 pF load. Biasing is accomplished with a 1 Mohm external resistor which delivers 9 uA current to a four transistor current mirror (transistors M8, M5, M7 and M9) to control the bias currents supplied to three stages of the OpAmp.
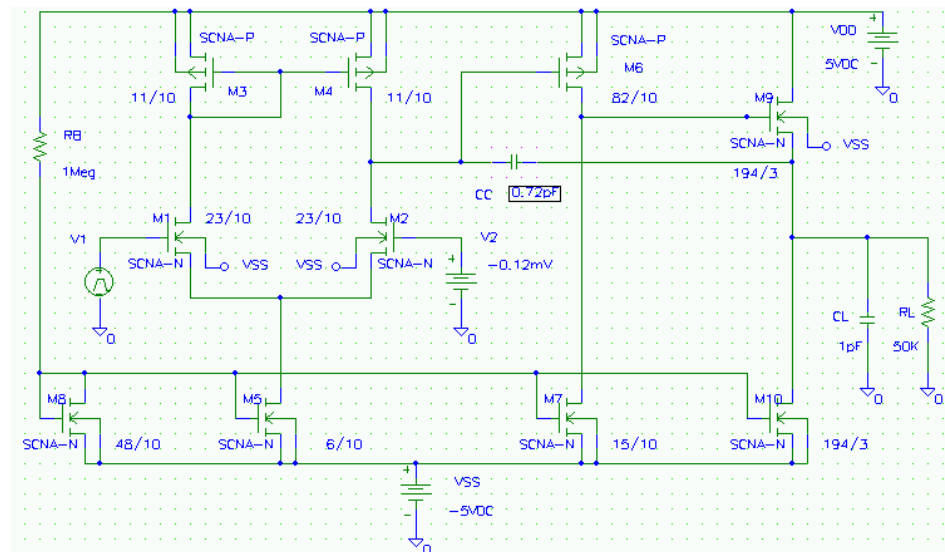

Figure 1. CMOS OpAmp

Figure 2 displays screen capture of a section of design calculation done in a student's submitted Mathematica file. Such a file contains design calculations based on equations derived, but also includes assumptions, estimates or final adjustments that have to be made to tune the design results to fit the specification windows. It also becomes a record of those. The design calculations lead to the specification of AR (Aspect Ratio) = Width/Length of all the MOSFETs in the circuit and the geometric dimensions of the compensation capacitance (Cc in the circuit) based on which chip layout design will be made. The compensation capacitance is calculated to achieve the required value of Phase Margin (> 45 degree) and Gain x Badwidth Product (> 0.5 MHz). Detailed guidance for these can be found in Allen and Holberg's text [1].

Layout and Bias Results Summarized:

Calculated: Actual Values Used/Obtained:

$AR_1 = 2.316$ W=23   L=10
$AR_3 = 1.077$ W=11   L=10
$AR_5 = 0.39$ W=6   L=10   (Compensated W by 6/4 to bring I5 up to .72uA)
$AR_2 = 2.316$ W=23   L=10
$AR_4 = 1.077$ W=11   L=10
$AR_8 = 4.815$ W=48   L=10
$AR_6 = 8.177$ W=82   L=10
$AR_9 = 97.379$ W=194 L=3   (Compensated L by 3/2 to bring I10 down to 180uA)
$Area_{Cc} = 8.714 \cdot 10^{-10}$
$AR_7 = 1.482$ W=15   L=10
$AR_{10} = 97.379$ W=194 L=3   (Compensated L by 3/2 to bring I10 down to 180uA)
$C_c = 7.216 \cdot 10^{-13}$ Cc=0.72pF
$I_1 = 3.608 \cdot 10^{-7}$ I1=0.397uA
$I_5 = 7.216 \cdot 10^{-7}$ I5=0.794uA
$I_6 = 2.739 \cdot 10^{-6}$ I6=2.62uA
$I_8 = 8.901 \cdot 10^{-6}$ I8=8.88uA
$I_9 = 1.8 \cdot 10^{-4}$ I9=176uA
$I_{TOTAL} = 1.924 \cdot 10^{-4}$ ITOTAL=188uA
$A_v = 1 \cdot 10^5$ Av=33.600 average (= 28.000 small signal at V1=0)
$A_{v1} = 497.181$
$A_{v2} = 201.134$

                                $R_B = 1 \cdot 10^6$ $R_L := 50 \cdot 10^3$ $C_{Lmax} := 100 \cdot 10^{-12}$

$V_{inMin} = -3.579$ VinMin = -3.9 V
$V_{inMax} = 5.096$ VinMax = +4.55 V
CMRange = 8.674   CMRange = 8.45 V
$\Delta V_{max} := 4.0$ VoutMax=3.6V. VoutMin=-4.8V
GBW = $1.257 \cdot 10^7$ rad/s   GBW = 1.3 MHz (= 8.2 x 10^6 rad/s)
$S_{min} := 1.0 \cdot 10^6$ S = 1 V/us (both rising and falling)
Offset Voltage: VOS1= 0.12 mV
Phase Margin=60   Phase Margin= 76

                        CMRR =   30,000 / 0.262 = 114,500   or   101 dBs

Term_Design_Opamp.nb

Input

Stage 3 Design

$I_{10} = S_{min} * C_{Lmax} + \frac{AV_{max}}{R_L}$ // EngineeringForm // N

$115. \times 10^{-6}$

$I_{10} = 180 \times 10^{-6};$

$I_9 = 400 \times 10^{-6}$ // N

0.0004

$Solve\left[I_9 == \frac{1}{2} * K_N * X * ((VDD - AV_{max}) + V_{TON})^2, X\right]$

$\{\{X \rightarrow 9.26333\}\}$

$AR_9 = 9.26;$

$W_{min} = L_{min} * AR_9$ // N

0.00002778

$C_{ox9} = L_{min} * W_{min} * C_{ox}$

6.90131×10^{-14}

$C_c = 0.22 * C_{ox9}$

1.51829×10^{-14}

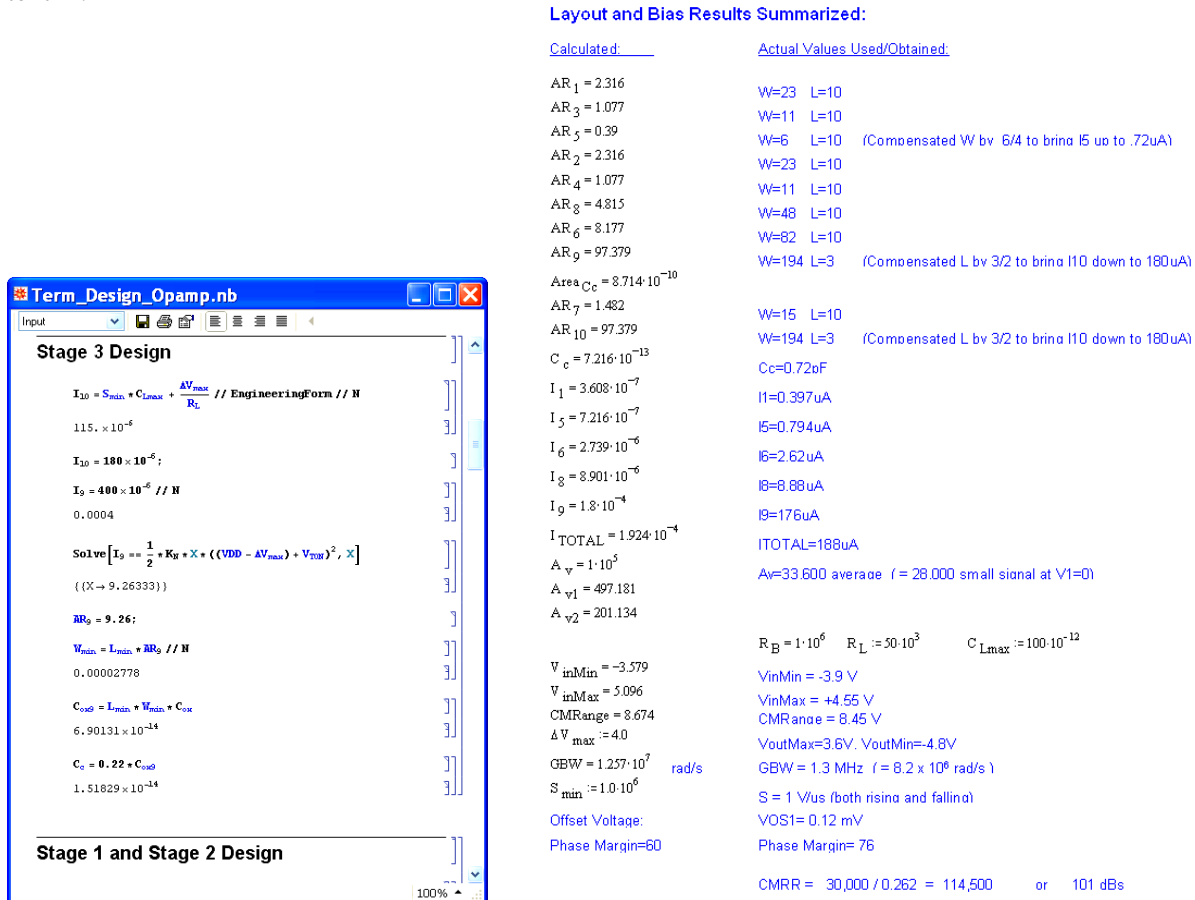**Stage 1 and Stage 2 Design**

100%

Figure 2. (a) Mathematica Design Calculations   (b) Transistor Sizes and Bias Currents Calculated

PSpice simulations are done starting with DC Vout-Vin transfer (Figure 3) which yields the input offset voltage, maximum and minimum output voltage levels. Slope of the DC transfer characteristics yields the low frequency open loop gain (Av = 33,466). Note that with zero input the input offset of even 0.2mV can easily push the output to its saturation. For the rest of the simulations and tests it has to be cancelled with an external bias. Otherwise the OpAmp operates its gain saturated region and the tests and simulations result in erroneous test results with very small open loop gain. The DC transfer characteristic shown in Figure 3 includes such a correction of -0.12 mV (included in the schematics in Figure 1).

The AC simulations of open loop gain reveal not only the gain but with the phase displayed the Bode plots obtained reveal unity gain frequency (Gain x Bandwidth product) and Phase Margin of this operational amplifier. (Figure 4) This design yielded Phase Margin of 76 degrees with GBW=1.3 MHz, better than the specs.
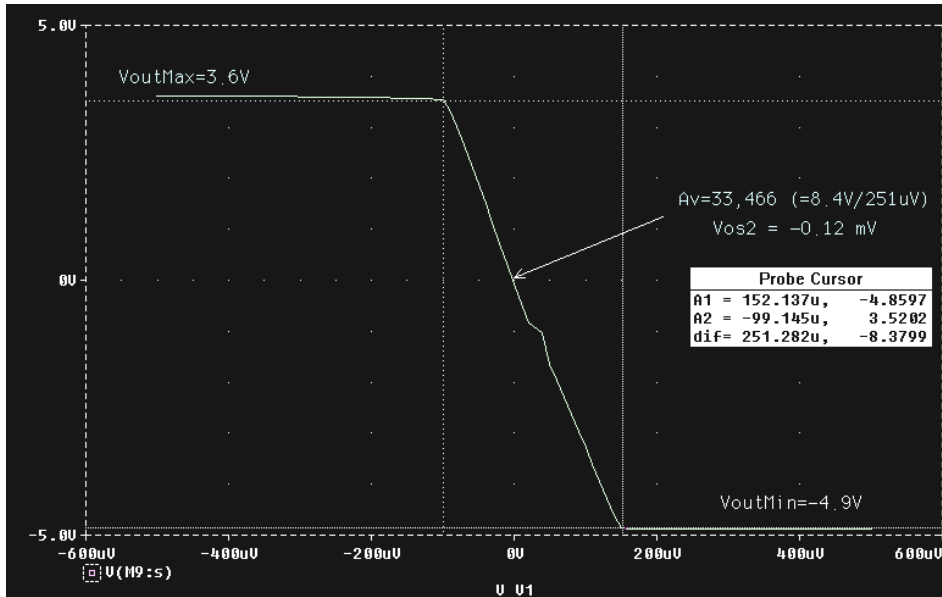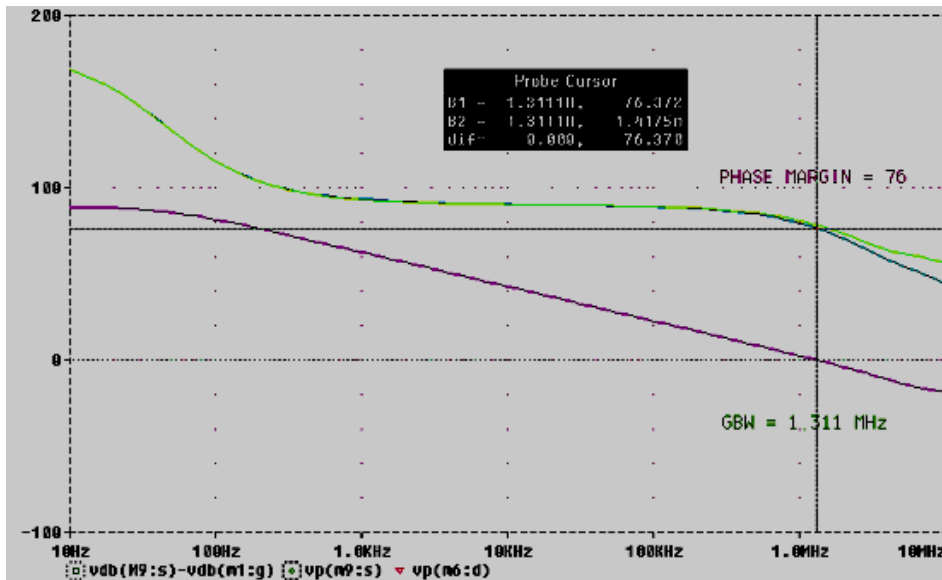
Figure 3.

Figure 4.

Figure 5 displays large signal transient response of the operational amplifier to a square wave input which has an amplitude large enough to drive the output to both of its maxima. Under these conditions the rise and fall times of the output are limited by the slew rate. Simulation results show the design yields slew rates of about 1 V/us twice as good as the specs.

Figure 6 displays DC transfer characteristics of the operational amplifier for a common-mode input. The slope of the curves measures the common-mode gain and the points where the slope suddenly increases indicates rejection limits have been exceeded. For this design useful common-mode range extends from (-3.9 V) to (+4.55 V) exceeding the specs of +/- 2.5V. Common-mode gain (the slope) is 0.365 which results in a CMMR (Common Mode Rejection Ratio) of 100,000 or 100dB.

Figure 7 shows a sample of student layout designs submitted. The small window clearly indicates that it passes DRC with zero design rule violations
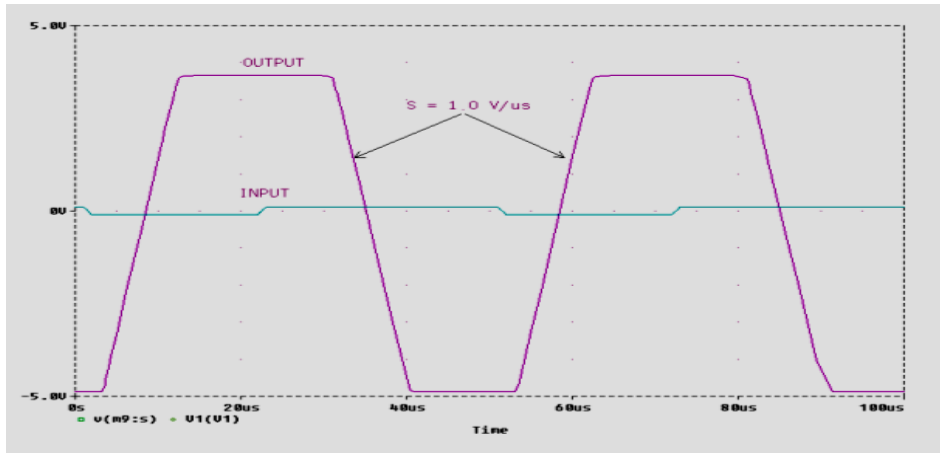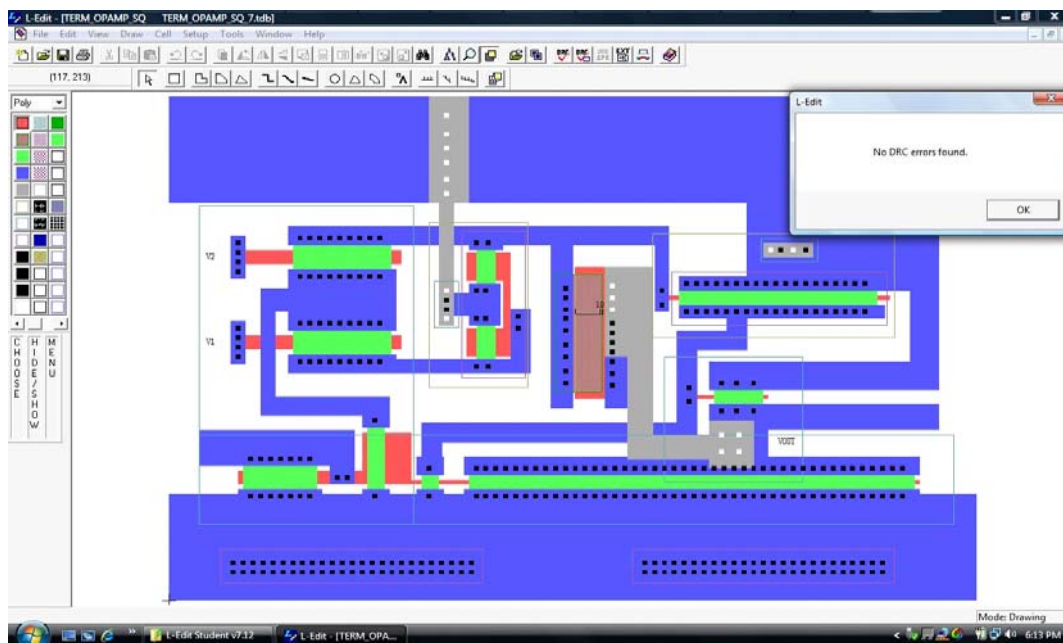
Figure 5.
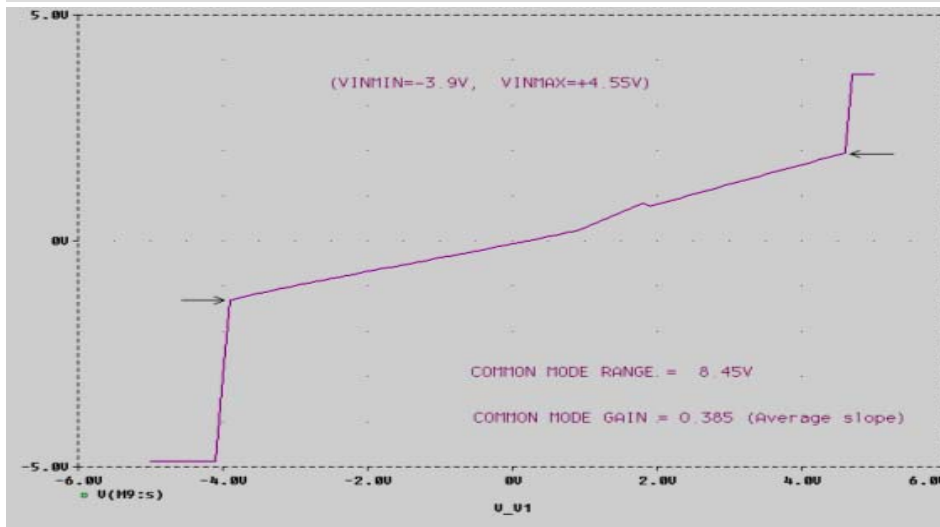
Figure 6.

Figure 7. A Sample of Student OpAmp Layout Designs (screen captured from L-Edit file submitted)

5. Design Project: Samples of Test Results on MOSIS Fabricated Designs

As stated before, it would be perfect to collect the Spice and Layout passing designs on a multi-project chip and have it fabricated, and give the experience and satisfaction of accomplishment as well as comparison between designed, simulated and the real device on silicon. However, this is impossible considering the time required to do that. However, if the projects assigned and specs chosen are similar in the consecutive annual offerings of the course, similar experience can be gained by testing the designs of previous years that have already been put on silicon and packaged, and ready to be tested. This is what was done with success.

Figure 8 displays a multi-project chip designed by the instructor. This is a combination of student projects which passed all the design requirements in Spice simulations and also passed DRC tests with no violation. It was later fabricated using MOSIS services, packaged and ready for testing, only after all of the designers graduated. It was put into use by the new designers.

Each student was assigned to test a different operational amplifier on that chip (there are eight different designs, four on each column). Pin diagrams were supplied. In the remaining pages samples from the results of tests are given.
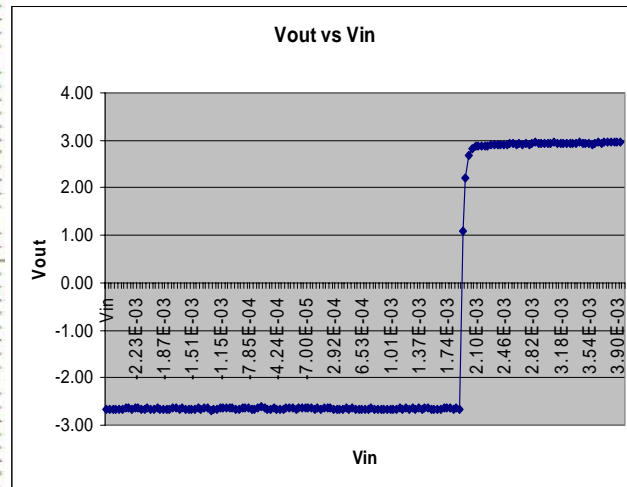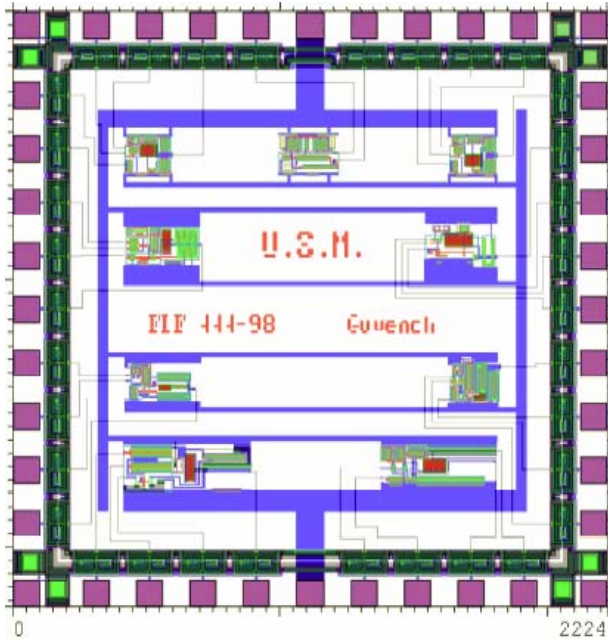

Figure 9. DC Transfer Chs measured with CIE-IV

Figure 8. Multi-project chip (left)

The DC transfer characteristics given in Figure 9 were measured using CIE-IV automated I-V measurement setup. It shows that the device output can swing more than +/- 2.5V spec, has a voltage gain greater than 10,000 (spec) and a DC offset of about 1.9mV.

The frequency response characteristics measured with CIE-Bode (Figure 10) indicate that the device has unity gain frequency greater than 1 MHz which is the upper limit of our set up. Phase plot also shows a value of 85 degrees even at 1MHz. It must be stated that open loop measurement of the frequency response of these high-gain amplifiers pose challenges with stray capacitances causing oscillations. For that reason, the operational amplifiers gain had to be reduced by negative feedback to about 100 (~40dB). In order to determine the unity gain frequency and phase margin a HP 4194A Gain-Phase Analyzer was employed which has a measurement range of 200 MHz. Figure 11 displays the result. Unity gain frequency of 1.938 MHz (about quadruple the spec) with a phase margin of 44 degrees is measured.

Figure 12 is the screen capture from an oscilloscope which shows the result of the slew-rate test. It measured approximately 8 V/us , significantly better than the specified value of 0.5 V/us.
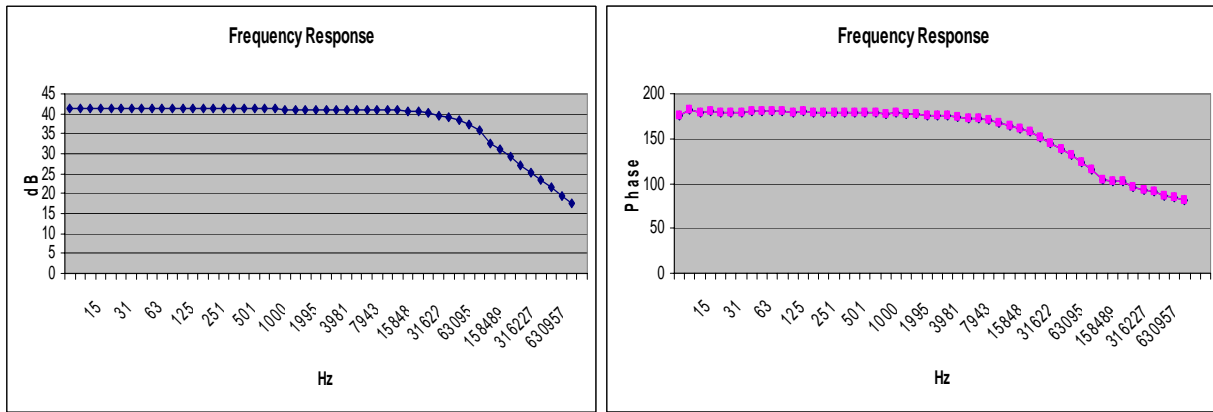

Figure 10. CIE-Bode Measured Frequency Response of an Operational Amplifier tested

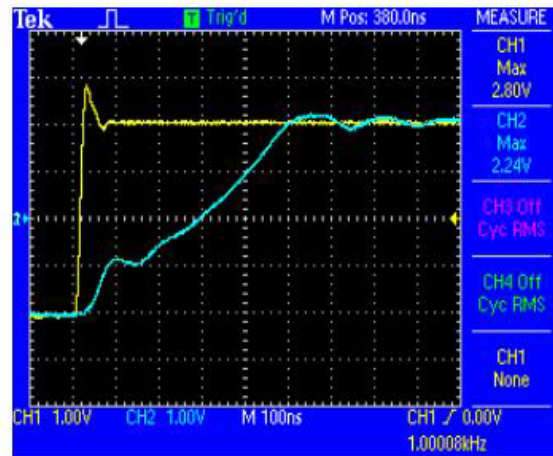Figure 11. Frequency Response and Phase Margin   Figure 12. Slew Rate Test

4. Conclusions

Design of CMOS operational amplifiers have been used as term projects in a senior level course on Analog Integrated Circuits in Electrical Engineering. With inexpensive tools using capabilities of a Computer-Integrated-Electronics laboratory successful designs have been completed starting from basic equations to create a Mathematica file for design. The designs were verified with Spice simulations to meet the specifications listed by the instructor. Students also completed layout design of their operational amplifiers, DRC checked and ready for fabrication. Lack of time before graduation to have their designs fabricated and for them to test to complete a real world engineering design experience was circumvented by using MOSIS fabricated designs of the previous classes. Use of similar technology and design specification in successful years made this experience possible.

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[8] L-Edit is a product of Tanner, Inc.