Developing VLSI Curricula in Electrical and Computer Engineering Department

Xingguo Xiong, Hassan Bajwa, Lawrence Hmurcik Department of Electrical Engineering, University of Bridgeport, Bridgeport, CT 06604

Abstract

VLSI technology has enabled the information technology revolution which greatly changed the life style of human society. The rapid technology innovation in VLSI industry has lead to new challenges to modern VLSI engineers. Students need to be trained systematically in the VLSI field to meet these challenges. In this paper, we share our experience in developing VLSI curricula in Electrical and Computer Engineering department. A series of VLSI courses have been developed, such as EE 458 - Analog VLSI Circuit Design, EE 548 - Low Power VLSI Circuit Design, EE 549 - VLSI Testing. We also developed EE 448 - Microelectronic Fabrication to cover the physical fabrication processes for modern VLSI circuits. In addition, modern VLSI is shifting from microelectronics to nanoelectronics due to the rapid development in nanotechnology. This will bring a new technology revolution to current VLSI industry. As a result, we also introduced the fabrication of future nanoelectronic circuits (such as quantum dot cellular automata, nanowire crossbar circuits, etc.). Students demonstrated intense interest in the VLSI field. Many students are also doing the VLSI graduate research and published papers and posters in the VLSI related journals and conferences.

1. Introduction

VLSI (Very Large Scale Integrated Circuits) has been one of the most important technologies developed in 20th century. During the last decade, the VLSI industry has made continuous efforts to keep shrinking the size of the transistors, so that more and more transistors can be built into a single VLSI chip to make it more and more powerful [1]. Moore's law has governed the trends in VLSI industry for the past decades [2]. The transistor size has been shrunk into deep submicron or even nanometer domain, so that more and more transistors can be integrated into the same chip area. Nowadays a state-of-the-art Intel Xeon Microprocessor MP X7460 based on 45nm technology contains more than one billion transistors [3]. Smaller transistor size results in lower cost, faster speed and lower power consumption. Nowadays, the minimum feature size of commercial VLSI technologies has been shrunk into deep submicron and nanometer domain. Furthermore, according to ITRS (International Roadmap [4], Technology for Semiconductors) 2009 summary MEMS (Microelectromechanical Systems) and Nanotechnology devices are being integrated with VLSI circuits into a System-on-Chip (SoC), as shown in Figure 1. Nanotechnology will bring new revolution to VLSI technology, which leads to brand new circuit architecture and fabrication strategy for future next-generation nanoelectronics. Nanoelectronics is expected to introduce revolutionary changes to current silicon-based CMOS VLSI technology, and maintain Moore's law in the following decades [5]. As more and more transistors are built into a single VLSI chip, this also bring tremendous challenges to the design, fabrication and testing of modern VLSI circuits. The early generation of small-scale ICs containing tens or hundreds of transistors could be manually designed by engineers in the physical level. However, nowadays a typical VLSI may contain millions of billions of transistors. The complexity can no longer be handled by individual engineers manually. Computer software (EDA tools) must be used in the design of complex VLSI system design. For the complex

VLSI digital system, a top-down instead of traditional bottom-up design strategy should be used. The testing of modern VLSI circuits can no longer be exhaustively tested due to extremely long test time. As a result, new test strategies must be developed to test the modern VLSI circuits efficiently. Students need to be trained with systematic knowledge and skills in various VLSI EDA tools in order to meet the challenges as VLSI engineers in modern VLSI industry.

Figure 1. Moore's law and more [4]

In this paper, the experience of developing systematic VLSI curricula at graduate level in Electrical and Computer Engineering department in University of Bridgeport is shared. A series of VLSI courses have been developed to cover various fields in VLSI technology. Some introductory course (e.g. CPE/EE 448D - Introduction to VLSI) has been developed to give students a comprehensive introduction about digital VLSI design. In this course, the fundamental knowledge in digital VLSI design is introduced, including CMOS transistors, layouts, combinational and sequential circuits, memory, design of arithmetic building blocks, timing analysis, clock distribution, etc. Students also get familiar with basic VLSI EDA (electronic design automation) tools such as OrCAD PSPICE, Mentor Graphics tools, ModelSim, Synopsys tools, etc. As portable electronics (e.g. laptops, cellp hones, PDAs, digital cameras) are becoming more and more popular, and energy conservation is receiving public awareness, low power VLSI circuit design is attracting more and more interests. We developed EE 548 - Low Power VLSI Circuit Design to introduce various low power techniques to reduce the power consumption of VLSI circuits. Nowadays the VLSI circuits can contain billions of transistors, the testing of such complex system becoming more and more challenging. We developed EE 549 - VLSI Testing to introduce various VLSI testing strategies for modern VLSI design. In addition, analog and mixed signal circuit design is becoming more and more important as MEMS (Microelectromechanical Systems) and Nano devices are integrated with VLSI into System-on-Chip (SoC) design. We developed EE 458 -Analog VLSI Circuit Design to introduce the analog and mixed signal VLSI design. Furthermore, we also developed EE 448 - Microelectronic Fabrication to introduce the physical fabrication process of modern VLSI circuits, so that students understand how a real VLSI circuit is fabricated in the VLSI industry. Furthermore, we also cover the nanofabrication of various next-generation nanoelectronic circuits. With such a series of VLSI related curricula, students have an opportunity to learn comprehensive knowledge in VLSI design, fabrication and testing of VLSI circuits. Students can also accumulate hands-on experience in various EDA tools such as PSPICE, Mentor Graphics tools (Design Architect for circuit design, IC Station for layout design, and Accusim for simulation), Synopsys tools, ModelSim for VHDL/Verilog design, etc. The curricula prepare students as VLSI engineers to meet the growing demands of VLSI industry.

2. Developing VLSI in Electrical and Computer Engineering Department

To prepare students in their VLSI career to meet the challenges of modern VLSI design, fabrication and testing, a series of VLSI courses have been developed to cover comprehensive fields in VLSI technology. These courses include but are not limited to: EE 549 - Low Power VLSI Circuit Design, EE 589 -VLSI testing, EE 458 - Analog VLSI, etc. Furthermore, EE 448 - Microelectronic Fabrication is also developed to cover the fabrication processes of modern VLSI circuits. The above series of VLSI curricula prepare students with solid knowledge background and hands-on design experience in the VLSI field. The details of the above VLSI courses are introduced as below.

1). EE 548 - Low Power VLSI Circuit Design

With the rapid development of mobile computing, as well as the energy conservation consideration, low power VLSI design has become a very important issue in the VLSI industry. In this course, VLSI power models are introduced so that students have an in-depth understanding about the power consumption of VLSI circuits, and how we can reduce the power dissipation. A variety of low-power design methods are employed to reduce power dissipation of VLSI chips. This course is designed to cover low-power design methodologies at various design levels (from system level to transistor level). The basic low-power design strategies are introduced. Students use the learned knowledge to design low-power VLSI circuits.

Upon completion of this course, students are expected to be able to analyze the power consumption of VLSI circuits, and design low-power VLSI circuits using various strategies at different design levels. The major target is to design VLSI chips used for battery-powered systems and high-performance circuits not exceeding power limits.

2). EE 549 - VLSI Testing

As VLSI continues to grow in its complexity, VLSI testing and design-for-testability are becoming more and more important issues. This course covers VLSI testing techniques such as such as VLSI fault modeling (stuck-at-fault), automatic test generation, memory testing, design for testability (DFT), etc. VLSI scan testing and built-in self-test (BIST) are also covered. Students learn various VLSI testing strategies and how to design a testable VLSI circuit.

The goal of this course is to help students get familiar with knowledge and skills in VLSI testing and validation. Students learn VLSI fault modeling, testing strategies for combinational/sequential circuits, memory, and analog circuits. Some important topics such as delay testing, design for testability (DFT), built-in self-test (BIST) and boundary scan standard are also discussed. Upon completion of this course, students are expected to be able to effectively test VLSI systems using existing test methodologies, tools and equipments.

3). EE 458 - Analog VLSI Circuit Design

Analog circuits are very important for the front and back ends to interface to the outside world. The system-on-chip (SoC) technology requires the implementation of both digital and analog modules on a single chip. The goal of this course is to introduce the modeling, design

and analysis of analog CMOS VLSI. The students design analog VLSI layouts, extract the netlists and simulate the circuit behavior. The transistor sizing in analog VLSI layouts is also discussed.

Upon the completion of this course, students are able to design and analyze basic analog and mixed-signal CMOS VLSI circuits. They get to know various analog/mixed-signal VLSI circuits such as current sources and sinks, amplifiers, S/H circuits, switching-capacitance circuits, analog-to-digital and digital-to-analog converters, etc. They are expected to be able to design analog VLSI layouts, decide transistor sizing, and simulate the designed VLSI circuits.

4). EE 448 - Microelectronic Fabrication

This course covers basic microelectronic fabrication processes for semiconductor and VLSI technologies, including photolithography, plasma and reactive ion etching, ion implantation, diffusion, oxidation, evaporation, vapor phase epitaxial growth, sputtering, and CVD. Advanced processing topics such as next generation lithography, MBE, and metal organic CVD are also introduced. The physics and chemistry of each process are introduced along with descriptions of the equipment used for the manufacture of integrated circuits. The integration of microfabrication process into CMOS, bipolar, MEMS and nanotechnologies is also discussed.

The purpose of this course is to provide students with technical background and knowledge in silicon microelectronic fabrication process. Fabrication processes on Microelectromechanical System (MEMS) and nanotechnology are also introduced. Upon finishing this course, students are expected to be familiar with the basic semiconductor and VLSI microfabrication processes. They can explain the physical and chemical mechanism for the fabrication process, and understand the basic procedures of the process. Furthermore, as VLSI industry is continuing shrinking the size of transistors, nowadays a state-of-the-art Intel CPU may contain billions of transistors. Traditional microelectronic fabrication is approaching the physical limit of transistor sizing induced by the wavelength of exposure light used in photolithography process. In order to overcome this bottleneck and maintain Moore's law for several decades, nanotechnology is the only hope. Nanotechnology introduces bottom-up molecular self-assembly fabrication strategy, which is totally different from the traditional top-down fabrication strategy. As a result, it can easily achieve resolution comparable to the size of individual atoms and molecules (~ astron), and extremely high efficiency. Nanotechnology also enables many new physical phenomena (e.g. quantum mechanics effect) and new devices for future nanoelectronic circuits. Many new architecture for future nanoelectronics have been suggested, such as nanowire cross-bar circuits [6], carbonnanotube (CNT) based transistors [7], single-electron transistors (SETs) [8], and nanoelectronics circuits based on quantum-dot cellular automata (QCA) [9], etc. In EE 448 -Microelectronic Fabrication, we also introduced the fabrication of nanoelectronic circuits to prepare students for the challenges of next-generation nanoelectronics.

3. Results and Discussions

VLSI courses generally involve heavy design projects for students to get familiar with the various EDA tools. As a result, the computer support is very essential for VLSI course curriculum. The School of Engineering in our university has 6 general computer laboratories which can be used for VLSI design and simulation. The computer labs totally have 135

desktop PCs and 20 Ultra25 Sun Microsystems workstations. The PCs are equipped with Windows XP and Redhat Linux dual operating systems. Various EDA tools are available to students. Some EDA tools are: Cadence PSPICE, Synopsys (Tetramax ATPG, Design Vision, DC Shell, etc.), Mentor Graphics tools (IC Station, Design Architect, Accusim), etc. All the computer labs are equipped with ceiling projectors with multimedia support, and network printers.

A Digital Design Laboratory is also available, which is equipped with 10 workstations. Each has a PC, programmable Altera boards, 2 power supplies, and oscilloscope, function generator, different kinds of TTL chips, Altera boards, Xilinx boards, multimeteters, and other related hardware. Furthermore, we have a Microprocessor Laboratory/Embedded Systems Laboratory. It has 10 stations. Each has a personal computer, function generator, oscilloscope and multimeter. It also has 15 Microchip boards used in the microprocessor class, 10 micro-controller, 2 EPROM programmers, 1 ultraviolet erasers, 2 development centers and more boards and many other hardware. It has Assembly emulators, Altera in full and student versions, etc. We also have a Circuits (I and II) Laboratory used to for basic electronics/digital applications. It has 10 workstations. Each one has: a PC, programmable Altera/Xilinx boards, 2 or more power supplies, oscilloscope, function generator, different kinds of TTL chips, multi-meters. The laboratory has many diverse/different chips, ICs and motors. These software and hardware support are very helpful for students in VLSI courses. Students can apply the knowledge they learned from the class into real VLSI experiments.

During the teaching, students are also encouraged to explore the most recent research frontiers in the VLSI field. Students are asked to do some background survey, search for most recent research papers in the field (e.g. low power VLSI, VLSI testing, etc.), and share their findings in the class. Through the discussion, they know the most recent research activities in the field. This also help them to find possible research issues in the VLSI field, and trigger their interest to further dig into the VLSI research. Many students eventually use the topics they find in their master project/thesis research, and achieved excellent results. They published some posters/papers in academic conferences/journals, and won the awards in the ASEE student poster competitions in the recent years. The layout design of the circuit with gated clock technique from a student poster is shown in Figure 2 [10]. The PSPICE schematic design of a 8-bit low power Wallace tree multiplier in PSPICE from another student paper is shown in Figure 3 [11].

Figure 2. Layout design of a sequential circuit with gated-clock technique [10]

Figure 3. Schematic design of 8-bit Wallace-tree multiplier [11]

Furthermore, in our VLSI curriculum, we also introduce to students about next generation nanoelectronic circuit design. For example, Quantum-dot Cellular Automata is a promising next-generation nanoelctronic technology due to their extremely low power consumption, fast speed and very high device density. In our VLSI courses, we assign a student project about the design and simulation of a QCA full adder. QCA Designer software (Version 2.0.3) [13] by University of British Colombia is used for this project. It is free software and students can download it and install it into their computers [13]. Students are also asked to read various research papers [14][15] to help them in their QCA circuit design. QCA circuit is totally different from traditional CMOS VLSI design. It utilizes the propagation of quantum dot cell polarization instead of voltage to transfer signals. Special clock scheme (four clock zones with each clock zone lagging a 90° phase difference from previous clock zone) is required for proper driving of signal flow in QCA circuit. Furthermore, the interference among neighboring QCA cells may even cause the QCA circuit to mal-function. All these are brand new concepts for students, and they are very excited about this new experience. An example 1-bit QCA full adder circuit in QCA Designer software interface from a student project is shown in Figure 3. Students are interested in QCA circuit design. Some of them are doing research in QCA circuit design of multiplier, memory, ALU and other VLSI circuits. This can help prepare students to meet the challenge of emerging next generation nanoelectronics technology.

4. Conclusions and Future Work

In this paper, the development of VLSI curricula in Electrical and Computer Engineering department is introduced. A series of VLSI courses have been developed. These courses include but are not limited to: EE 549 - Low Power VLSI Circuit Design, EE 589 - VLSI testing, EE 458 - Analog VLSI Circuit Design, etc. Furthermore, EE 448 - Microelectronic Fabrication is also developed to cover the fabrication processes of modern VLSI circuits. The course descriptions and the goals of these courses are discussed in details. The above series of VLSI curricula prepare students with knowledge and design experience in the VLSI field. The VLSI curricula have triggered intensive interests among students. The teaching of above courses has also triggered students' interest in active VLSI research. Based on their master projects/thesis research, students have posters/papers in academic conferences and journals.

Figure 4. A full adder circuit design with QCA (Quantum-dot Cellular Automata)

In the future, we plan to further develop some more VLSI courses. We are also planning to arrange a multi-semester project to cover both the VLSI design and testing. In the VLSI design course (e.g. EE 548 - Low Power VLSI), students are asked to design the physical layouts of VLSI circuits. Once the designs are completed, students will submit their designs to MOSIS [12] for fabrication. In the next semester, students will take the VLSI testing (EE 549) course. When the real fabricated chips are shipped back to students, they will utilize the knowledge they learned in VLSI testing class to thoroughly test the fabricated circuits. This will be very helpful for students to understand the full cycle of modern VLSI design, simulation, fabrication and testing.

References

^[1] T.H. Ning, "Silicon VLSI trends - what else besides scaling CMOS to its limit?", *Proceedings of the 10th International Symposium on the Physical and Failure Analysis of Integrated Circuits 2003 (IPFA'03)*, pp. 1-4, July 7-11, 2003.

^[2] R.R. Schaller, "Moore's law: past, present and future", *IEEE Spectrum*, Vol. 34, Issue 6, pp. 52-59, Jun. 1997.
[3] Microprocessor quick reference guide, URL: http://www.intel.com/pressroom/kits/quickreffam.htm.

^[4] ITRS (International Technology Roadmap for Semiconductors 2009 Summary. URL: http://www.itrs.net/Links/2009ITRS/Home2009.htm

^[5] M. Haselman, M.; S. Hauck, "The Future of Integrated Circuits: A Survey of Nanoelectronics", *Proceedings of the IEEE*, Vol. 98, Issue 1, pp. 11-38, Jan. 2010.

^[6] M. Dong, L. Zhong, "Nanowire Crossbar Logic and Standard Cell-Based Integration", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, Issue 8, Aug. 2009, pp. 997-1007.

[7] H.-S.P. Wong, Jie Deng, Arash, Hazeghi, T. Krishnamohan, G.C. Wan, "Carbon Nanotube Transistor Circuits - Models and Tools for Design and Performance Optimization", *Proceedings of IEEE/ACM International Conference onComputer-Aided Design (ICCAD'06)*, San Jose, CA, Nov. 5-9, 2006, pp. 651-654.

[8] K. Uchida, "Single-Electron Transistors and Circuits for Future Ubiquitous Computing Applications", *Proceedings of the 32nd European Solid-State Circuits Conference (ESSCIRC 2006)*, Montreux, Sept. 19-21, 2006, pp. 17-20.

[9] R. Tang, F. Zhang, Y-B. Kim, "QCA-based nano circuits design", *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, Vol. 3, May 23-26, 2005, pp. 2527-2530.

[10] Y. Yang, X. Xiong, "Gated Clock Technique for Low Power VLSI Design", 2009 Northeast ASEE (The American Society for Engineering Education) Conference, Bridgeport, CT, Apr. 3-4, 2009.

[11] Xiaoping Li, Xingguo Xiong, "Power Comparison of CMOS and Domino Full-adders", *ASEE Zone 1 Conference 2008*, United States Military Academy, West Point, NY, Mar. 28-29, 2008.

[12] MOSIS website, URL: http://www.mosis.org.

[13] QCADesigner software by the University of British Columbia, URL: <u>http://www.mina.ubc.ca/qcadesigner_downloads</u>

[14] A. Vetteth, K. Walus, V.S. Dimitrov, G.A. Jullien, "Quantum-dot Cellular Automata Carry-lookahead Adder and Barrel Shifter", *IEEE Transactions on Nanotechnology*, Vol. 6, No. 3, May 2007, pp. 374-383.

[15] R. Tang, F. Zhang, Y. Kim, "QCA-based nano circuits design [adder design example]", IEEE International Symposium on Circuits and Systems (ISCAS 2005), Vol. 3, 2005, pp. 2527-2530.