AC 2008-2677: EDUCATIONAL OPTICAL FIBER DATA COMMUNICATIONS TOOLKIT

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Educational Optical Fiber Data Communications Toolkit

Abstract

The use of optical fiber is certainly a significant recent technological advance that provides very high quality communications over great distances. Given the now common use of optical fiber in the industry and high-end consumer electronics, the use of optical fiber should be more widely taught. Certainly, the availability of low-cost plastic fiber, detectors, and data communications grade light emitting diodes (LEDs) makes suitable educational materials within financial reach.

Unfortunately, the use of optical fiber is still a curiosity in undergraduate data communications courses. Perhaps a missing element is the availability of practical examples that demonstrate complete data links. In addition to the actual fiber and optics, transmitter and receiver electronics are required, as well as devices to encode, decode, and retime digital data. With data rates over inexpensive plastic fiber reaching into the multi-megabit per second rate, traditional asynchronous communications methods are no longer appropriate. Synchronous techniques like that used with higher speed glass optical fiber data links are needed.

This research presents a toolkit that we intend to have students use to investigate the physical layer in an optical fiber based network. The required test gear includes a multimeter and an oscilloscope. Given our use of photo diodes, an optical power meter is entirely optional. At the core of the toolkit is the optical fiber toolkit adapter card which provides the transmitter and receiver electronics. The adapter board attaches to an off-the-shelf field programmable gate array (FPGA) development board, which provides the digital aspect of the data link.

The first audience we are addressing is undergraduate technology students. As such the design goal of the toolkit is to provide a system that clearly demonstrates functionality, allowing students to investigate all aspects of the system. The choice of using an FPGA provides a level of flexibility, allowing the toolkit to be used in other curriculum as well. Further, with a softcore processor, the toolkit can be used to implement a modest microprocessor system. It is our intent that the fiber optic toolkit will be useful in undergraduate classroom or laboratory settings, as well as in independent projects. The toolkit is being used with students during the spring 2008 semester. Preliminary results will be available for the 2008 ASEE convention and all documentation for the toolkit is freely available on the project website¹.

Introduction

Optical fiber technology provides very high quality data communications over great distances. With the growing and now common use of optical fiber in industry and high-end consumer electronics, the use of optical fiber should be more widely taught. For this purpose we are developing an educational optical fiber data communications toolkit that provides students with the means to investigate the physical layer in such a network. We first used the toolkit during the spring 2008 semester. The components and fiber are inexpensive and convenient to use. Despite modest performance in comparison to glass fiber, plastic fiber provides an inexpensive

and effective tool for introducing the most important principles of fiber optic data communications.

The first audience we address is our undergraduate technology students. In a technology program less emphasis is placed on *design* and more emphasis is placed on *analysis*, or what a circuit does. Such students are provided with extensive hands-on laboratory experience. As such our first goals are to clearly demonstrate commonly used principles and focus more on functionality rather than elegant circuitry. Appropriately, the design motto established for the toolkit is "*let me see the functionality*."

The kit is composed of a custom adapter card that provides transmitter and receiver electronics along with a small solderless breadboard area, an off-the-shelf FPGA development board, fiber optic light emitting diode (LED) devices, photo diodes, and plastic fiber. The solderless breadboard area enables students to investigate characteristics of the LED, photodiode, and optical fiber. The linearity of the LED and photodiode as well as attenuation of the fiber is examined using only resistors and a multimeter. The transmitter and receiver electronics provide the means to transmit and receive data. One design goal is to be able to provide a data rate of at least one million bits per second. The output of the first amplifier can be measured for rise and fall time directly using an oscilloscope.

It is possible for a data link to be limited in performance either by optical power considerations or by pulse spreading caused by optical dispersion. Students will consider the power budget for a data link and will measure the attenuation in fiber. Relative measures of optical power are made based on the near linearity present in the actual components, which is also demonstrated. Students also consider optical dispersion. Surprisingly, the performance of a plastic fiber data link driven by an LED is more likely to be limited by the electronic components themselves or attenuation, than optical dispersion.

A field programmable gate array (FPGA) generates the transmit data signal and also retimes received signals. A simple circuit drives an LED at the transmitter end. With respect to the receiver students learn about transimpedance amplifiers and data slicers. The topics of line coding and synchronous communications are introduced with Manchester encoding. A discrete time phase-lock loop configured into the FPGA retimes the received data. Other than the flexibility afforded by an FPGA, the development board is flexible in the discretion afforded to the instructor. In the extreme laboratory scenario, in some cases an instructor can prepare for an experiment by configuring the development boards so that when students arrive, actually performing an experiment can be a matter of turning the power *on*.

Apart from its first use in our technology program, the toolkit provides plenty of opportunities for engineering student projects and graduate student research. In particular, by means of a soft-core microprocessor, the FPGA can implement an optical fiber peripheral device for a larger computer or can be a modest microprocessor system with peripherals in its own right. Students can investigate various network topologies and protocols such as implementing a ring using a token passing protocol.

The Overall System

The fiber optic toolkit provides a low-cost means for students to examine a practical data link. Such a data link can be constrained in at least two ways. Performance can be limited by the optical power budget or by the available bandwidth. The power budget is basically the difference between the transmitter coupled power and receiver sensitivity. Bandwidth is related to pulse spreading which involves inter-symbol interference. Given the significant loss and modest bandwidth, plastic fiber is useful for students to investigate such design constraints.

In particular, the kit uses Eska brand one millimeter core step-index plastic fiber, manufactured by Mitsubishi². The LED and photo diodes use simple connectorless type optics. The optical fiber is cut to length simply with a sharp blade. The required test gear includes a multimeter and an oscilloscope. Given our use of photo diodes in the toolkit, an optical power meter is entirely optional.

The programmable logic device (PLD) provides students new opportunities to study data communications. PLDs range from simple logic array devices used for glue logic and the complex programmable logic device (CPLD) that replaces many small chips, to the high density field programmable gate arrays (FPGA) capable of implementing an entire system on just one chip. We selected the Spartan-3 series FPGA⁴ devices Given the availability of the Spartan-3 Starter board⁵ and the software development tools that are free or are available at little cost, this FPGA is particularly convenient.

Figure 1 is the fiber optic toolkit hardware. The Spartan-3 starter board is to the left and the custom adapter card is to the right. The captions indicate several of the most significant features. In particular, the JTAG cable is for configuring the FPGA. The LED and photo diode are inserted into a solderless breadboard. The Flash memory device to the left of the expansion connector provides standalone capability in configuring the FPGA. The starter board also has simple input and output devices to the left, a clock generator, and other features.



Figure 1: Fiber optics toolkit hardware

Attenuation and Power Budget

As discussed by Hecht⁶, the power budget is a useful tool for considering how optical power can be a constraining factor. In (1) the difference between the transmitter power P_{tx} and the minimum required power P_{rx} at the receiver is the amount of power available to the link, which comprises the sum of all the losses P_{loss} and margin P_m . Here the students consider simple losses associated with an optical fiber data link.

$$P_{\rm tx} - P_{\rm rx} = \sum P_{\rm loss} + P_{\rm m} \tag{1}$$

The definition of decibel units is well known to be the ratio of two relative power values (2). The advantage in using decibels is that equations become simpler. Given the squared relationship of the power dissipated by a resistor, with respect to voltage, (3) is true for resistors. In dealing with other types of components, such as diodes, refer back to the definition (2).

$$P_{\rm dB} = 10\log\left(\frac{P}{\rm P_{\rm Ref.}}\right) \tag{2}$$

$$P_{\text{RES-dB}} = 20 \log \left(\frac{V_1}{V_{\text{Ref.}}} \right)$$
(3)

In most cases in this paper, in comparing power values we assume decibels, as in (2). With optical fiber, it is sometimes useful to express power in dBm units, where the reference is one milli Watt. In those cases where we consider an actual power level, we use dBm units.

While the circuit in Figure 2 does not convey data, it is adequate for studying linearity and fiber optic cable attenuation. The LED load resistor is selected to adjust the LED current and the photo diode load resistor sets the sensitivity of the receiver. Given that the LED forward voltage is nearly constant, we expect to see a linear relationship between the transmitter and the receiver currents.



Figure 2: Linearity and attenuation test

Measurements are taken with an ordinary voltmeter. Figure 3 is an example response of the photo diode load resistor voltage with respect to the LED current. The LED is an IFE97⁷ with 660nm wavelength and the photo diode is an IFD91⁸ device. The fiber used for Figure 3 is one meter long. The fitted line did not consider the first three data points. This shows that for moderate current, the coupled power is approximately linear with respect to the LED current.

Likewise the photo diode current and load resistor voltage are also approximately linear with respect the received optical power.



We next use the circuit in Figure 2 to consider the optical fiber attenuation with respect to fiber length. An IFE91D⁹ device with 870nm wavelength is used to consider dependence on wavelength. The loss through a given length of fiber can be predicted with the approximation of decibels per meter. To examine this approximation, students use optical fiber cut to various lengths. In Figure 4, the attenuation in a one meter link is used as the reference, so that lengths longer than one meter have positive attenuation.



There are two observations for students to consider, first that attenuation is dependent on wavelength and second that attenuation is different for shorter than for longer lengths of fiber. The dependence on wavelength is a property of the plastic used. One reason for the second observation is that in coupling light to a fiber there are unstable modes that dissipate in the first few meters. Once the unstable modes dissipate, the attenuation becomes nearly constant.

In our own measurements, for 660nm wavelength the attenuation is approximately 0.75dB/m for 1m length and 0.20dB/m for 10m length. The data sheet for GH4001 Eska brand fiber² specifies a comparable worst case attenuation of 0.17dB/m at 650nm for kilometer lengths, which we can interpret to mean *very long* lengths of fiber. For 870nm wavelength, using linear approximation with the photo detector, attenuation was found to be about 2.7dB/m for 1m lengths and 1.8dB/m for 10m length. The published typical data³ indicate slightly higher loss which appears to be due to a pronounced peak at 900nm.

Considering Bandwidth

The overall response time and corresponding bandwidth causes pulse spreading which can degrade performance. Hecht⁶ describes how the overall response time T_o for a simple LED driven optical fiber data link is composed of the component response times below. The fiber response time in particular is approximately proportional to the fiber length *L*. Note that because of the root-square relation for any one term to dominate its value must be significantly larger than the others.

$$T_o = \sqrt{T_{\rm tx}^2 + T_{\rm f}^2 + T_{\rm rx}^2}$$
(4)

- T_o = Overall response time
- T_{tx} = Transmitter response time
- $T_{\rm f} = L \cdot \Delta t$ = Fiber spreading
- $T_{\rm rx}$ = Receiver response time

We next consider the actual fiber. According to Weinert¹⁰, optical dispersion is the spreading that occurs to a light pulse as it travels along an optical fiber, as in Figure 5. Here we consider dispersion due to the various optical modes that appear in a plastic fiber. The idea is that a light ray traveling straight down a fiber follows a shorter path and will arrive at the receiver sooner than a ray that reflects along inside the fiber. As outlined by Weinert, (5) is the measured spreading per unit length caused by the fiber and (6) predicts the spreading per unit length based on characteristics of the fiber, where NA is the numeric aperture, c_0 is the speed of light in a vacuum, and n_1 is the refractive index of the fiber core.



$$\Delta t = \frac{\mathrm{NA}^2}{2c_0 n_1} \tag{6}$$

(5)

The SigGen3 application produces a 100nsec pulse train with a 10usec period. The transmitter and receiver outlined in the next section were used to take measurements. Two lengths of optical fiber were considered. In using the values from the optical fiber data sheet² (NA = 0.5, n = 1.49), we estimate that the spreading is approximately 0.2796ns/m or 7ns for 25 meter of fiber, which is similar to the observed 4nsec.

- 1 meter fiber, measured 112nsec pulse width
- 25 meter fiber, measured 116nsec pulse width

Given the attenuation, it is fairly safe to predict that the longest plastic fiber optic data links are in the 100m range in length. It is more likely that a plastic fiber optic data link driven by an LED will be limited by attenuation or the electrical components themselves, rather than the bandwidth of the optical fiber. Consider that for a 100 Mbs data link the bit period of 10ns is approximately 35 times larger than the modal dispersion in one meter of this particular fiber.

Optical Fiber Transmitter and Receiver

Next consider the actual transmitter and receiver. The gen1 application produces a 'low'-'high' bit sequence resembling a square wave. Switches select a bit rate from either 10Mbs, 1Mbs, 100kbs, or 10kbs. The circuit in Figure 6 is the transmitter. The FPGA outputs V_{op} and V_{on} form a low voltage differential signal pair (LVDS^{11,12}). The corresponding standard for LVDS is TIA/EIA-644. The Resistors R1, R2, and R3 form a divider for driving the differential pair Q1 and Q2. The resistor R4 is adjustable to set the drive current to a value in the range from 5mA to 25mA and R5 allows observation of the drive current.



Figure 6: Example fiber optic transmitter

The receiver circuit in Figure 2 used earlier has conflicting requirements. First, to have adequate sensitivity the detector resistance must be fairly large. But this stands in contradiction as a large resistance reduces receiver bandwidth. Appendix-A outlines a useful relation between bandwidth and rise time. While our design goal is at least 1.0 Mbps, according to the data sheet the IF-D91 photo detector⁸ should be capable of data rates to 100 Mbps or for analog signals provide a bandwidth of at least 70MHz. But with a device capacitance less than 4pF, with a 100K detector resistor, the cutoff frequency is no smaller than 400 kHz which is not acceptable.

$$F_c = \frac{1}{2\pi RC} \tag{7}$$

Unfortunately, simply using a smaller value resistor to provide adequate bandwidth along with a gain amplifier is problematic as such a small resistance has significant noise current which degrades the receiver. Johnson–Nyquist noise¹³, also known as thermal noise is the electronic noise generated by thermal agitation of charge carriers inside a conductor. Thermal noise is approximately white meaning that the power spectral density is equal throughout the frequency spectrum. The RMS value of the noise current in (8) is I_n where k_B is Boltzmann's constant in Joules per Kelvin, T is the resistor's absolute temperature in Kelvins, Δf is the noise bandwidth, and R is the resistor has a thermal noise current of approximately 45.2nA.

$$I_n = \sqrt{\frac{4k_B T \Delta f}{R}} \tag{8}$$

Since we intend to use an amplifier anyways, a transimpedance amplifier allows us to better satisfy such conflicting requirements. As a case in point in applying our motto of *let me see the functionality*, we chose to not use the OPA380¹⁴ amplifier which is self biasing and is optimized for fiber optics. Clearly, the OPA380 provides an elegant solution. Rather, we chose to use the OPA657¹⁵ wideband operational amplifier in a trans-impedance configuration. This component more closely follows text book discussion, conceptually is simpler, and allows students to control the bias or operating point.

Figure 7 and Figure 8 are the non-inverting and inverting receiver configurations, as when the photo diode receives light the amplifier output is perturbed in either a positive or negative direction. A large resistance is selected to provide the required sensitivity. The amplifier uses negative feedback in such a way that from the photo detector the effective resistance appears very small, which allows the bandwidth and data rate to be large.



The reference voltage applied to the amplifier sets the nominal reverse voltage for the photo diode. Theory tells us that the photo diode current should be nearly independent of the applied voltage. In allowing a manual adjustment, students can investigate this phenomenon and consider practical limits for the operating point for each configuration.

The output of the transimpedance amplifier is very analog and will not comply with any given logic signal standard. This is especially true given the large dynamic range possible due to the attenuation in plastic fiber. The circuit in Figure 9 converts such a signal to digital values. Such action is called *slicing* the signal. A jumper setting allows a student to choose between a reference produced by an RC low-pass filter and a manual adjusted reference voltage. The RC low-pass filter produces the average value so that given a 50% on-time, the average will be in the center between the analog values corresponding to *low* and *high*.



Figure 9: Data slicing circuit

The manually adjusted reference allows students to investigate the effect of duty cycle distortion. An issue arises with such systems during the start of a message. Assuming that initially the fiber has been dark for awhile, time is required for the low-pass generated reference to settle. During this time the logic output will have a noticeable duty cycle distortion.

Manchester Encoding and Encapsulation

Synchronous serial communications is a widely used technique whereby the transmitter uses an encoding to convey the data and clock together. Students can use a digital storage oscilloscope to observe the transients that occur at the start of a message and likewise can observe how the

toolkit uses a discrete time phase-lock loop for retiming to recover the received data. To provide synchronous communications we selected the popular Manchester Code following the IEEE 802.3 standard¹⁶ in that a '1' bit is represented by the sequence 'low-high' and a '0' bit is represented by the sequence 'high-low' as in Figure 10. Here we refer to each such sequence as a *symbol*. The numbered vertical dash lines are the boundaries between *symbols*. Note that a transition always occurs at the center of each symbol.



Figure 10: IEEE 802.3 Manchester coded data

A transmitted *message* starts as shown in Figure 11. This format is similar to that in IEEE 802.3. Starting at the left, the message begins with a preamble which is a simple alternating '1', '0' pattern. While the preamble pattern is broadcast, transitions occur only at the center of each bit-cell. The preamble provides a means for the receiver to settle so that transients involving duty cycle distortion suitably decay. The preamble also provides a simple and reliable means for the retiming logic to obtain phase-lock. Once phase-lock is achieved, the receiver is directed to ignore transitions that occur at the boundary between symbols. The SFD nibble flag marks the beginning of the actual message.



Figure 11: Beginning of a message

Following the nibble flag is a so-called MAC frame, which is simply data, provided by the higher network system layers. Encapsulation is an important principle for students to understand. The physical layer provides no details regarding the content of the MAC frame. The MAC frame is essentially treated by the physical layer as cargo. In receiving a message, the preamble and nibble flag are stripped away and only the MAC frame is delivered to the higher level network layers.

Symbol Retiming

It is common practice to use a phase-lock loop to track a Manchester coded signal. The code 'timing1' uses the FPGA to produces only a preamble waveform and also provides a discrete time phase-lock loop for retiming. The following is paraphrased from Hill¹⁷. Future work will involve the logic for generating and disassembling actual messages and may also consider the use of a discrete phase-lock loop component. In Figure 12 a flip-flop and exclusive-OR gate detect a signal transition. The discrete time signal generator (DCO) produces a saw-tooth waveform. Once phase-lock is established the PreLock signal is forced *low*, instructing the register (Reg.) by means of the control logic (Cntl) to load only near the center of each symbol. Each symbol is sampled N_s times, to produce one estimate of the phase error between the local

clock and that corresponding to the received data. With a 50MHz system clock, to produce a 1Mbps symbol rate the signaling speed is actually 2Mbs. It is convenient to sample the input at 50MHz so that each symbol is sampled 50 times.



Figure 12: Discrete time phase-lock loop

Theoretical analysis of the phase-lock loop is outside the scope of our first audience presentation. The reader is referred to Appendix-B for a more complete theoretical discussion of the phase-lock loop. Students can draw diagrams to explain the behavior of the phase-lock loop in qualitative terms and can use an oscilloscope to observe how the phase-lock loop is able to obtain and maintain phase-lock.

Summary

In closing, optical fiber technology provides very high quality communications over great distances. Given the growing and now common use of optical fiber in the industry and high-end consumer electronics, it is hoped that this toolkit will inspire and motivate the teaching of optical fiber data communications. We are using the fiber optic toolkit during the spring 2008 semester and will soon have preliminary feedback. Plastic optical fiber provides an inexpensive and effective tool for introducing the most important principles of fiber optic data communications. Considerations are given to how a data link can be limited in performance either by optical power considerations or by pulse spreading caused by optical dispersion. A field programmable gate array (FPGA) is used to generate the transmit data signal and also retime received signals. An adapter card provides receiver and transmitter electronics. Other than the flexibility already afforded by an FPGA, the accompanying development board should be particularly flexible in the discretion afforded to the instructor.

Appendix A – First Order Low Pass Filter Model

The first order low-pass filter model is particularly helpful. Here we consider a low-pass filter with time constant τ and D.C. gain K. The filter cutoff frequency is F_c and the step response is h(t). A relationship between rise time and bandwidth is particularly useful. In considering the time to rise from 10% to 90% of the final value, we solve (9) and (10) to produce the familiar approximation in (11).

$$H(s) = \frac{K}{1 + \tau s}; \text{ where } F_c = \frac{1}{2\pi\tau}$$
(9)

$$h(t) = K\left(1 - e^{-t/\tau}\right) \tag{10}$$

$$t_r = \frac{-\ln(0.1) + \ln(0.9)}{2\pi F_c} \approx \frac{0.35}{F_c} \sec$$
(11)

Appendix B – PLL Analysis

Analysis of the phase-lock loop used to recover received data falls along the lines of classic theory and is of particular interest to students familiar with discrete time signal theory. Freeman¹⁸ is a useful reference. The key here is that each received symbol is sampled N_s times, essentially scanned to produce one down-sample estimate of the phase error. In the following, the stability is considered and an optimal loop gain is selected to minimize the pull-in time. The model in Figure 13 assumes one estimate of the phase error per symbol. The values θ and ϕ as well as the corresponding values Θ and Φ are the received and local phase, respectively.



The down-sample delay in the phase comparison block models how an entire scan produces one sample estimate of the phase error. While steady state phase error can be eliminated by including an integrator in the loop filter, actually doing so increases the system order by one and also complicates the pull-in process. Given that a modest phase error can be tolerated, the loop filter L(z) is a simple scaling factor K_{λ} . With the loop filter being a scaling factor, the phase lock loop is modeled neatly as a second order system. The DCO is modeled as a phase accumulator, with sensitivity K_d .

$$\frac{\Phi(z)}{G(z)} = \frac{K_d}{z-1} \tag{12}$$

The system function from input θ to output g is as follows. The terms K_f and K are the forward gain and the overall loop gain, respectively.

$$\frac{G(z)}{\Theta(z)} = \frac{K_f (z-1)}{z^2 - z + K}$$
where: $K_f = K_e K_\lambda$
 $K = K_d K_f$
(13)

To select a value for the loop gain and consider the stability of the system we inspect the denominator of (13) to identify regions for which the poles are contained by the unit circle. The Schur-Cohn stability criterion described by Freeman formally identifies the region of stability. Inspecting the denominator produces the ranges that we consider.

- 0 < K < 0.25 unique real poles
- K = 0.25 poles repeat at z = 0.5
- 0.25 < K < 1.0 complex poles, decreasing dampening
- K = 0 or $K \ge 1.0$ non-responsive or unstable system

The root locus in Figure 14 is the trajectory of the system poles with respect to K. In considering that each pole contributes to the system response, the furthest pole is closest to the origin, implying the greatest damping, when K = 0.25. With K = 0.25, the phase error step response is in (14). Given an initial phase error of one-half symbol, the model suggests that without noise, after 10 symbol onential response, we c



$$(\theta - \phi)_{step} = \frac{-n}{2^n}; n > 0$$
(14)

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