
AC 2011-1060: ELECTRICAL ENGINEERING STUDENT SENIOR CAPSTONE PROJECT: A MOSIS FAST FOURIER TRANSFORM PROCESSOR CHIP-SET

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Electrical Engineering Student Senior Capstone Project: A MOSIS Fast Fourier Transform Processor Chip-Set

The purpose of this paper is to describe an undergraduate electrical engineering senior capstone design project “*success story*” from the University of Portland. This project incorporated the University of Southern California’s (USC) MOSIS¹ Educational Program (MEP) for the fabrication and packaging of a CMOS chip-set which successfully implemented a 4-bit, 8-sample Fast Fourier Transform (FFT) function.

MOSIS is an acronym for “Metal Oxide Semiconductor Implementation Service” and is run out of USC. The MOSIS Educational Program provides free CMOS integrated circuit fabrication services for participating universities in the form of a Multi-Project Wafer (MPW) using the N-Well 0.5um CMOS process from ON Semiconductor, Inc². The goal of the MEP program is to provide undergraduate electrical engineering students experience in integrated circuit design, fabrication, packaging, and test. At the University of Portland, senior EE student teams design their own digital circuit (which is part of their senior design capstone project) using a standard digital simulation tool (e.g., B²Logic from Beige Bag Software³). Then they layout their CMOS integrated circuit using a standard layout tool (e.g., L-Edit from Tanner Research, Inc.⁴). Finally, a standard layout file (e.g., CIF file) is produced and sent to MOSIS for mask-making, CMOS fabrication, and packaging.

The University of Portland’s Department of Electrical Engineering has been participating in the MOSIS MEP program since 1997. Approximately 50 EE student senior capstone design projects have successfully incorporated a MOSIS CMOS integrated circuit. It has been our observation that the use of the MEP program to implement interesting digital functions as part of an overall EE senior design project is an effective pedagogical experience for our students and faculty. Additionally, the MEP program plays a crucial role in “leveraging” EE student projects to higher functionality, higher project success rates, and higher achievement satisfaction in capstone design projects.

This paper describes a recent and particularly interesting EE senior design capstone project completed at the University of Portland which was implemented using two MOSIS chips (or chip-set). This particular project was the most sophisticated and complex among all MOSIS projects done at the University of Portland. Each chip contained over 2000 gates. (Typically, student-designed MOSIS chips contain approximately 500 to 1000 digital gates.) For their EE Senior Design Capstone Project, a team of three senior EE students from the University of Portland (Neil Tuttle, Ziyuan Zhang, and Sandra Pellecer), along with their two faculty advisors (Dr. Peter Osterberg and Dr. Aziz Inan) successfully designed and simulated a digital 4-bit, 8-sample Fast Fourier Transform Processor circuit and then implemented it as a CMOS chip-set and submitted their layout to the MOSIS Educational Program (MEP) for fabrication and packaging. After receiving the chip-set back, the students successfully built and tested a functioning Fast Fourier Transform prototype system which was presented and demonstrated to the EE community at the University of Portland. This use of the MEP Program to implement a sophisticated digital function such as the FFT was an extremely effective pedagogical experience for the students and the faculty.

FFT Circuit Description

The design of the FFT processor begins with the algorithm to be implemented. The FFT algorithm is a “divide-and-conquer” approach which reduces the number of required calculations from $O(n^2)$ to $O(n \cdot \log n)$, where n is the number of samples. Figure 1 shows the flow of data for an $n=8$ FFT.

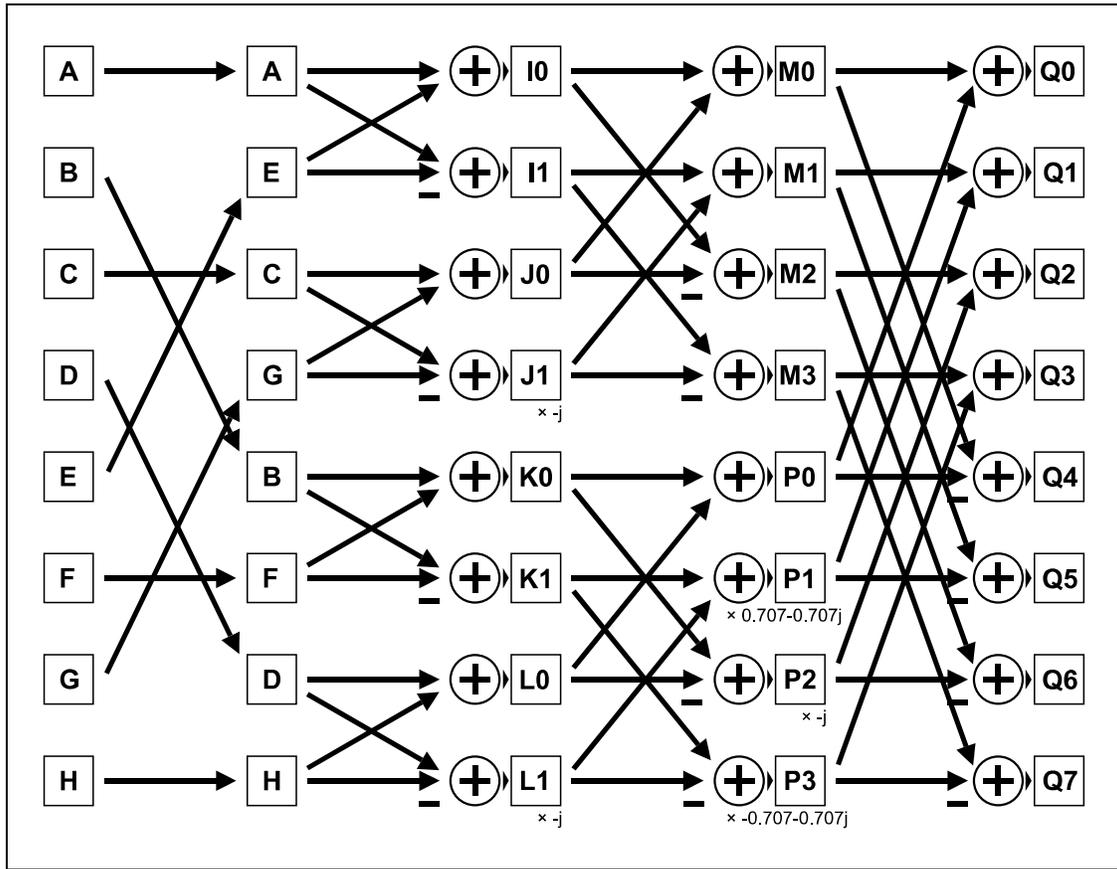


Fig. 1. Dataflow diagram of $n=8$ FFT

The students implemented the above FFT algorithm in digital logic using the B²Logic digital simulation tool from Beige Bag Software. The algorithm is split into a two CMOS MOSIS integrated circuit chip-set (CHIP1 and CHIP2). CHIP1 is responsible for receiving input and executing part of the FFT calculations. The data produced by CHIP1 is then transferred to CHIP2, where the final part of the FFT calculations is executed and the results obtained are buffered for output. Figure 2 shows the high-level block diagrams of MOSIS CHIP1 and CHIP2, along with the breakdown of calculations and communication between them. Figure 3 and Figure 4 show the CMOS integrated circuit layouts for CHIP1 and CHIP2, respectively. The layouts were created using L-Edit from Tanner Research, Inc.

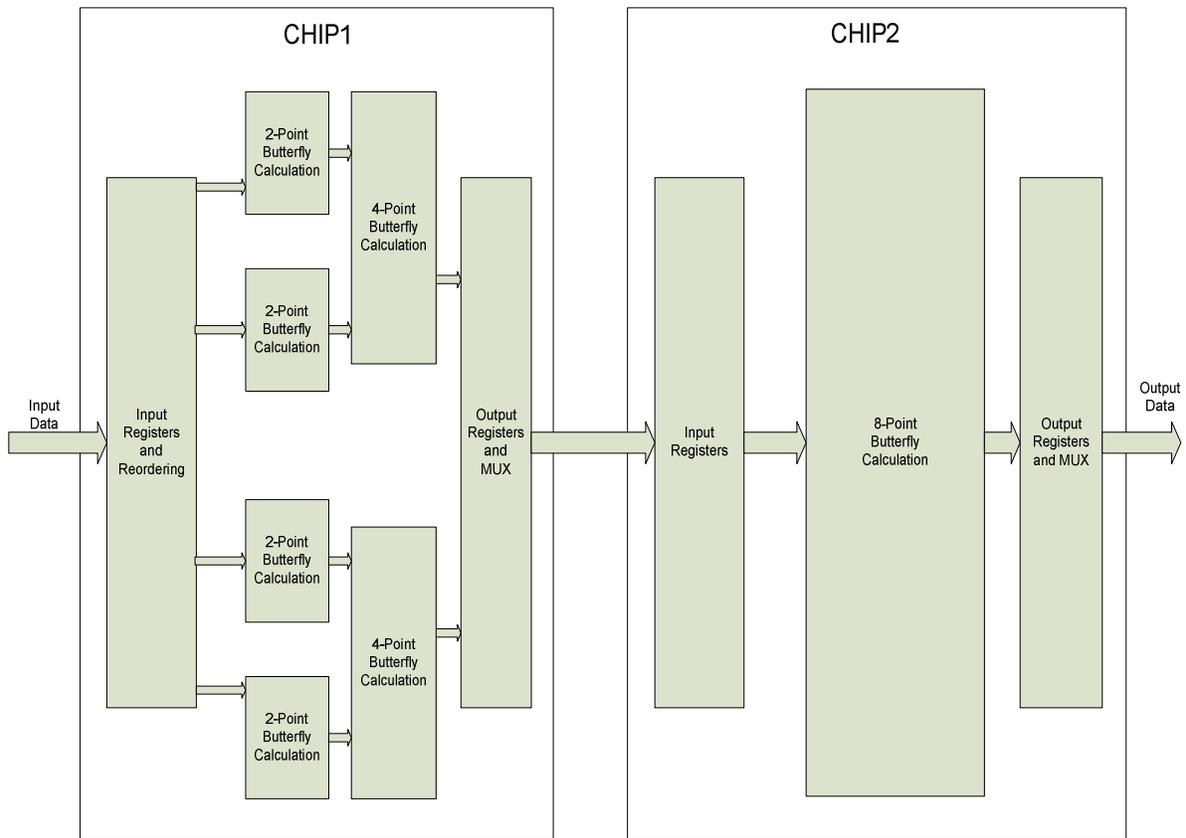


Fig. 2. High-level block diagrams of MOSIS CHIP1 and CHIP2

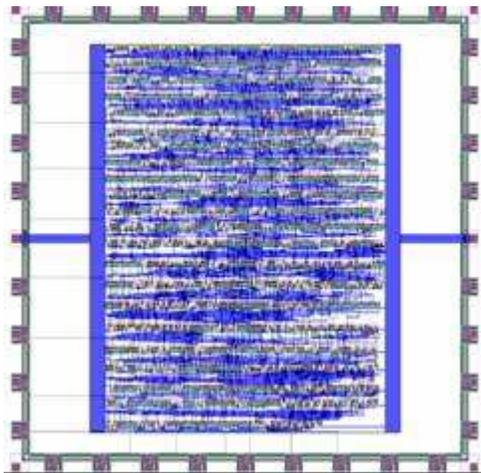


Fig. 3. L-Edit layout of CHIP1

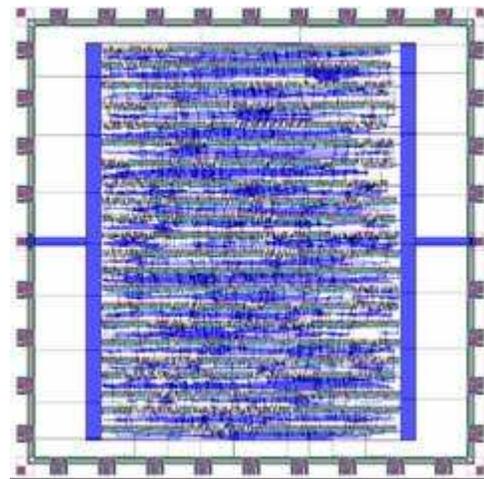


Fig. 4. L-Edit layout of CHIP2

Brief description of MOSIS CHIP1

The detailed block diagram of MOSIS CHIP1 is shown in Figure 5. To keep the initial design simple, the input is limited to eight four-bit signed samples in the 2's complement format. In order to avoid overflow, the final output consists of eight complex pairs of nine-bit signed fixed-point numbers. Each fixed-point number contains seven bits for its integer part and two bits for its fractional part. The range of the output data is greater than the range of the input data in order to prevent overflow.

The state machine in each of the chips is a five-bit binary counter with a decoder which controls the flip-flop storage elements. The asynchronous reset signal synchronizes the counters in CHIP1 and CHIP2 to the initial state. During the first eight clock cycles, CHIP1 reads the four-bit input data and stores it in an appropriate register. CHIP1 clocks in data on the falling edge. This step serves both to store and reorder the data. On the ninth clock cycle, CHIP1 performs four $n=2$ butterfly calculations simultaneously. An intermediate set of registers stores the result. Note that since the inputs must be real, the logic gates that would be responsible for handling complex numbers have been omitted wherever complex values are impossible. On the tenth clock cycle, CHIP1 performs two $n=4$ butterfly calculations simultaneously and stores the output data in a set of registers to prepare the data for output. At the rising edges of the 11th through 23rd clock cycles, CHIP1 clocks out the data from the output buffer using a multiplexer. Since CHIP1 contains the complex multiplication logic, it outputs eight-bit numbers to avoid overflow.

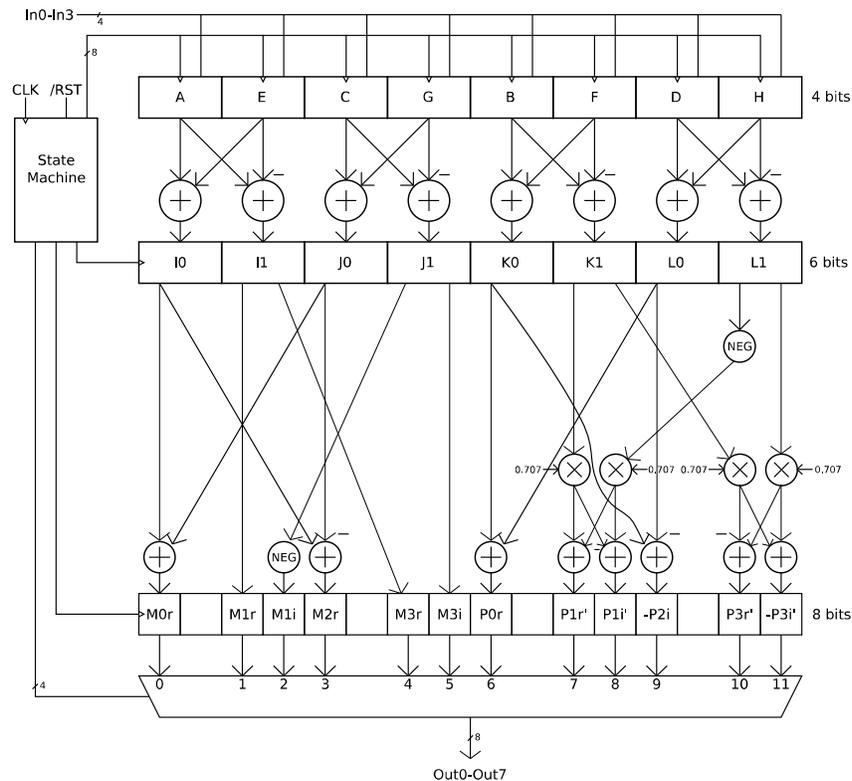


Fig. 5. Detailed block diagram of MOSIS CHIP1

Brief description of MOSIS CHIP2

The detailed block diagram of CHIP2 is shown in Figure 6. CHIP2 waits for the 11th clock cycle before it starts reading data from CHIP1. CHIP2 clocks in the data on the falling edge of each clock. On the 24th clock cycle, CHIP2 performs the $n=8$ butterfly calculation to complete the FFT algorithm. CHIP2 stores the result in a set of nine-bit fixed-point output registers. CHIP2 clocks out the data from the output registers on the rising edges of the 25th through 33rd clock cycles. After the 33rd clock cycle, the state counter wraps back to the initial state so that CHIP1 will be ready to receive new data on the next clock cycle. The outputs from CHIP2 are complex numbers in rectangular form. There are nine output pins for the real part and nine output pins for the imaginary part.

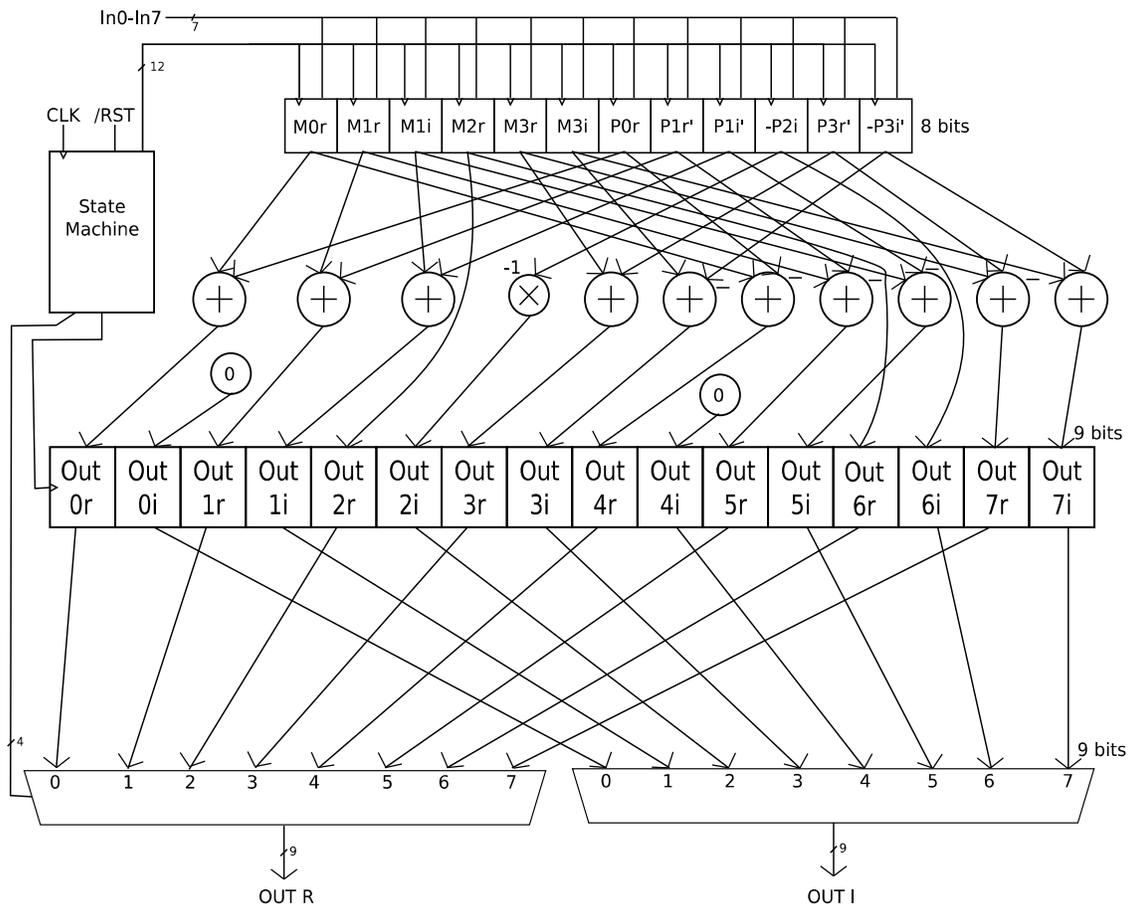


Fig. 6. Detailed block diagram of MOSIS CHIP2

The timing diagram in Figure 7 summarizes the interaction between CHIP1, CHIP2, and the enclosing system.

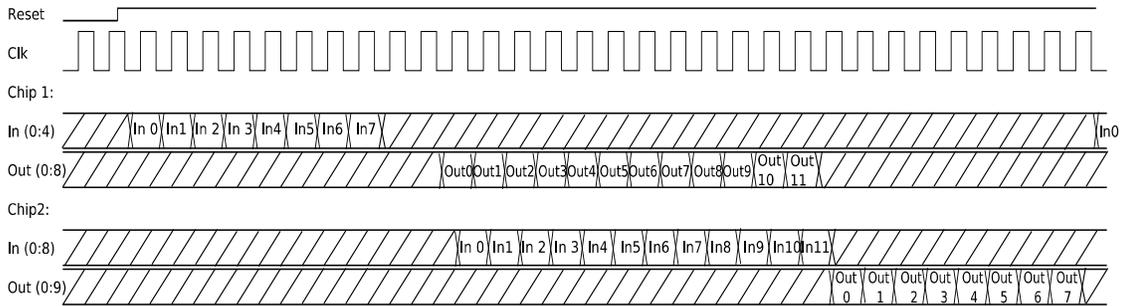


Fig. 7. FFT timing diagram

Test System

The final FFT project was assembled into a test system for debug and demonstration. The overall block diagram of this FFT test system, including the MOSIS chip-set (CHIP1 and CHIP2) is shown in Figure 8. The test system features a PIC microcontroller (PIC1) connected to a Personal Computer (PC), Liquid Crystal Display (LCD), and a secondary microcontroller (PIC2) which acts as an I/O extender.

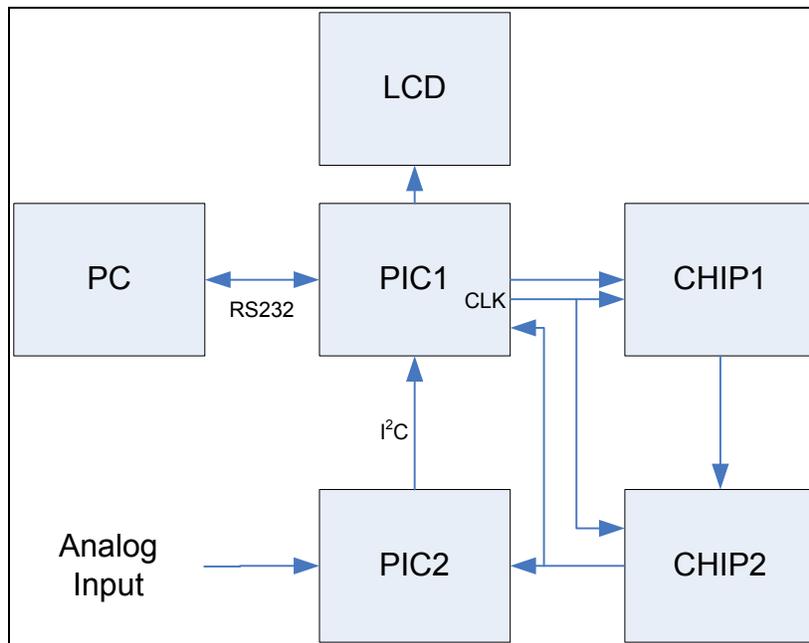


Fig. 8. FFT test system block diagram

PIC1 can receive data over the RS-232 protocol from a PC or over the Inter-Integrated Circuit protocol (I²C) from PIC2's internal A/D converter. The A/D converter samples analog input data from an external function generator at 10 kHz, so the maximum frequency on the input is 5 kHz. Next, PIC1 applies a clock signal to CHIP1 and CHIP2 and sends the data to CHIP1. PIC1 continues to clock CHIP1 and CHIP2 until the output data from CHIP2 is ready. PIC1 and PIC2 receive this result data from CHIP2. PIC2 sends its part of the data to PIC1 via the I²C bus. PIC1 formats and displays the data on the LCD and sends the data to the PC. The PC is used for testing and debugging and is not needed for normal operation.

A photograph of the final FFT test system is shown in Figure 9. The left side of the LCD displays the input samples and the right side displays the magnitude of each frequency component. Figure 9 shows the test system in action with input from a function generator (not shown).

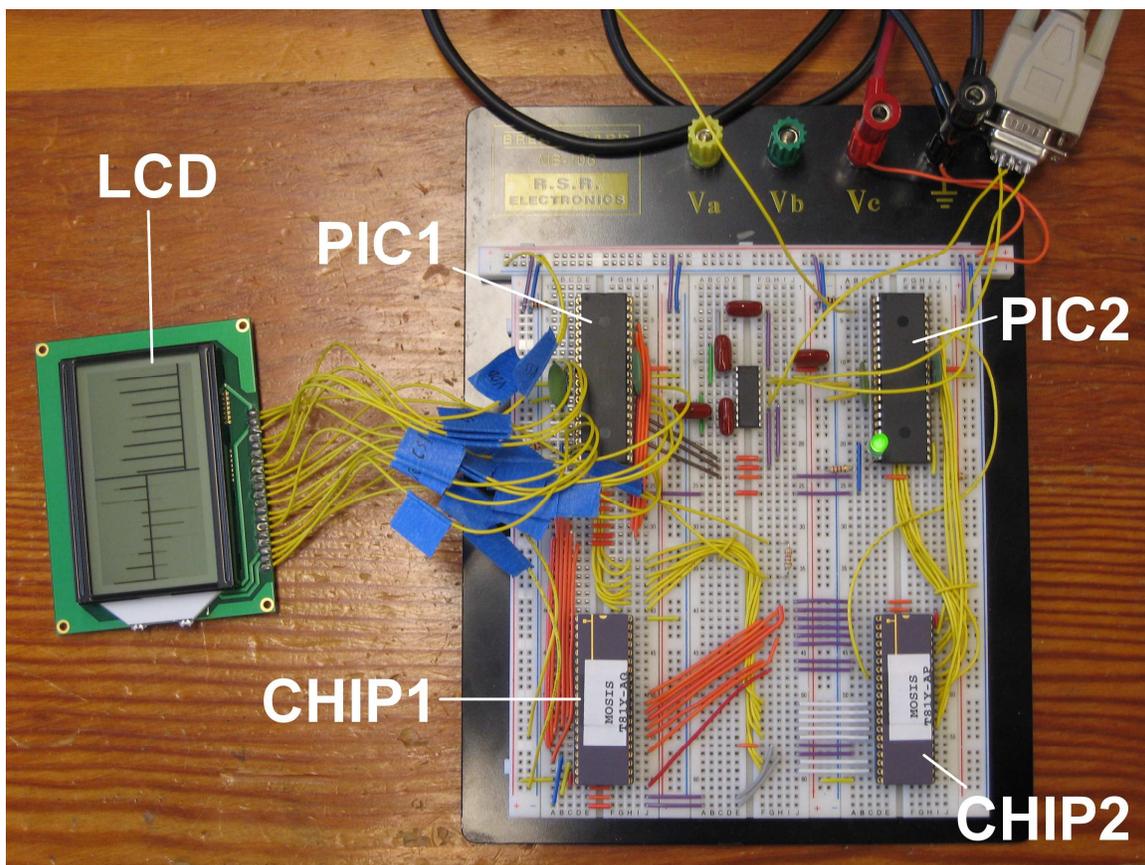


Fig. 9. Final FFT test system

Test Results

In order to test the CHIP1/CHIP2 Mosis chip-set, PIC1 has a set of test vectors and expected results in its ROM. When the system powers up, PIC1 runs the test vectors and automatically compares the actual outputs to the expected outputs. After PIC1 runs all the test

vectors, it reports to the PC whether the test has passed or failed. The LCD shows the input samples on the left and the amplitude of each frequency component on the right.

The chip set functioned as expected. Figure 10 shows a successful demonstration with a 3.6 kHz sine wave as the input and an $n=8$ FFT as the output. The MATLAB⁵ simulation results on the left agree with the actual test results on the LCD.

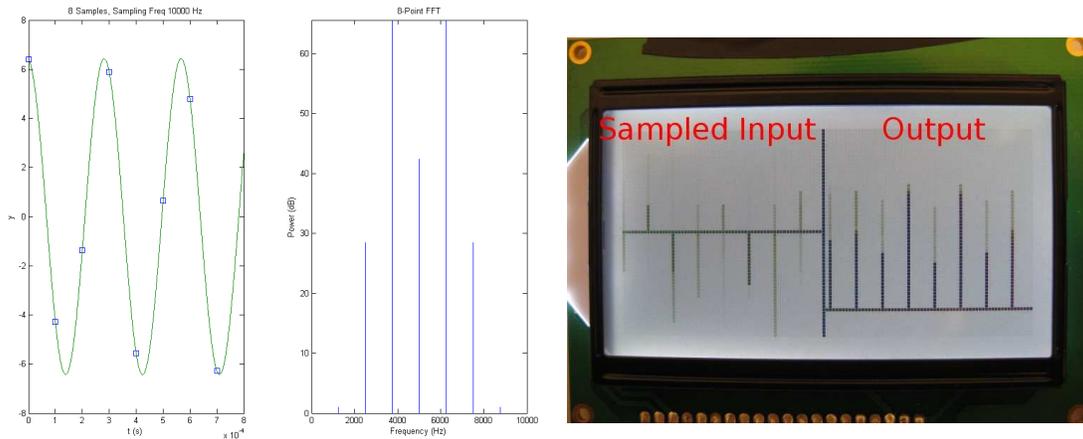


Fig.10. MATLAB simulation I/O (left) agrees with actual test I/O (right)

Conclusion

In conclusion, the 4-bit, 8-sample FFT chip-set is an effective use of the MOSIS Educational Program (MEP) to implement the Fast Fourier Transform function. It is an example of an extensive application at the undergraduate level. The MEP Program served as a vehicle to help the students implement a sophisticated digital function such as the FFT and provided them a pedagogical approach to achieve it. This project was an excellent example of how the MEP program plays a crucial role in “leveraging” EE student projects. This was the first time a design of this scale had been successfully attempted and completed at the University of Portland, and it achieved “first-silicon” success.

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