AC 2007-1139: ELECTRONS, HOLES, AND THE HALL EFFECT

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Electrons, Holes, and the Hall Effect

Abstract

Many students studying semiconductor theory have a difficult time grasping the concept of a hole as a real particle. From their experience in chemistry, physics, and electrical circuits classes, they have a firm grasp of the electron as a particle. However, the concept of an electron vacancy in the valance energy band of a semiconductor crystal behaving as a positive charge with mass seems metaphysical to them. In order to demonstrate that the theory is based on observations, an undergraduate student built a Hall effect device to measure the Hall effect voltage for doped semiconductor material. The Hall device will be used in future electronics classes as a demonstration of the electron-hole theory of semiconductor material. The project has two main results: the research student learned the laboratory procedures for making Hall effect devices using photolithography and thin film diffusion processes on silicon wafers and the electronics class now has a laboratory demonstration for reinforcing the electron-hole theory of semiconductors.

Our paper will present the difficulties encountered during construction of the Hall effect devices. The primary difficulties in building the devices are finding the correct balance of three factors: the magnetic flux density of the magnetic field, the current flowing through the doped semiconductor, and the sensitivity of our measuring instruments. Stronger magnetic fields and larger currents flowing through the Hall effect device cause the Hall effect voltage to be larger. However, we must balance this against the safety issues of strong magnetic fields and damaging the semiconductor material with too large of a current density. Finally, the paper will present a description of how the Hall effect devices will be used in the classroom to reinforce electron-hole current flow theory.

Introduction

The purpose of this research project is to build a Hall Effect device to demonstrate different charge carriers of the electrical current flow in p-type and n-type semiconductor materials. The demonstration is to be used in an undergraduate electronics course to prove the existence of hole current flow and electron current flow in semiconductor materials.

Eventually, the demonstration will consist of two Hall Effect devices: one with a p-channel conductor and the other with an n-channel conductor. However, we currently have constructed only the n-channel device. We started with the n-channel device because our laboratory has been doping n-type channels and regions for several years. It is only within the last year that we have obtained equipment to do p-type doping and we expect to create a p-channel Hall Effect device in early 2007.

Background

To briefly explain the concept of this project, consider the atomic levels of semiconductors: elemental semiconductors have four electrons in the outer shell. At absolute zero (0 K) the

electrons of the semiconductor atoms drop to the lowest shell (the valence energy band). Each shell is completely filled so that the electrons can not move. Hence, electrical current can not flow and the material is an insulator. At any non-zero temperature, however, some electrons can jump from the valence band to the conduction band (a higher energy band) and move about freely and electricity can flow. For every electron that jumps to the conduction band, there will be a vacancy (or hole) in the valence band. A hole moves as an adjacent electron (in the valence band) moves to fill the hole. As the electron fills the hole, it creates a new hole at the old location of the electron. As electrons move sequentially to fill holes, the holes travel through the material. For pure semiconductor material, there will be equal numbers of electrons and holes.[1]

Consider taking a semiconductor and doping it with a material that has "extra electrons." n-type donor materials have five electrons (e.g. "extra electrons") in the outer shell. Doping semiconductors with donor materials fills the valence band and forces the extra electrons to the conduction band. These electrons freely move through the conduction band and carry the majority of the charge when electric current flows in the n-type material. On the other hand, doping a semiconductor with p-type acceptor material (which has only three electrons in the outer shell) results in holes in the valence band. Because there are more holes in the valence band than there are electrons in the conduction band, the majority charge carriers of p-type material are holes.[1]

When current flows through these semiconductors in a magnetic field the charged particles tend to push to one side of the conductor or the other. The resulting voltage difference can be measured perpendicular to the current flow. The transverse voltage across a semiconductor is called the Hall Effect.[2] See Figure 1.

The primary difficulty in building this demonstration was the need to accurately measure very small voltages (on the order of micro-volts). In any given laboratory there are electrical noise sources that generate voltages that are induced into our experimental circuit. The measured noise voltages in the testing laboratories are approximately 10 mV unless proper grounding and shielding techniques are followed.

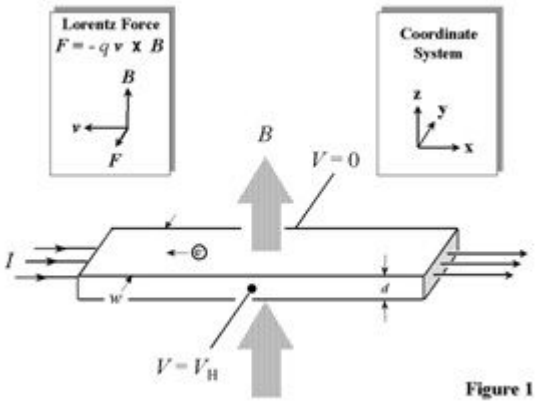

Figure 1: The Hall Effect[3]

Processing

The Hall Effect devices will be fabricated on 4-inch p-type silicon wafers, using planar processing techniques. The first step in the process is the growth of a thick silicon oxide (SiO_2) layer on the surface of the wafer, using wet oxidation. In this process, high purity oxygen gas is bubbled through boiling deionized (DI) water in order to couple steam into a high temperature furnace. The oxidation parameters (time and temperature) are determined by the minimum oxide thickness necessary for a subsequent doping process, as described later. The thickness of the oxide layer is measured and verified to be adequate for future processing.

Next, using standard photolithography techniques, small windows are etched in the oxide layer in order to expose regions of the silicon wafer that are to be doped and converted from p-type to n-type. The doping process is based on a conventional two-step diffusion profile, involving predeposition and drive-in. During predeposition, dopant sources containing phosphorous (an n-type dopant material) are placed in close proximity to the wafers in a high temperature furnace. This deposits a thin layer on the surface of the wafers that exhibits a high concentration of phosphorous. Using the natural process of diffusion, the phosphorus in this layer is then "driven-into" the wafer using yet another high temperature process. The diffusing phosphorous then converts the wafer from p-type to n-type. However, due to the oxide layer grown earlier, the conversion from p-type to n-type only takes place within the windows where the oxide has been removed by photolithography. Elsewhere, the oxide is thick enough to block the diffusion of phosphorous into the silicon. As a result, wells of n-type silicon are created within an otherwise p-type silicon wafer. The doping parameters (time and temperature) dictate the oxidation parameters outlined above – the higher the drive-in time and temperature, the thicker the oxide must be in order to serve as an effective block to the phosphorous diffusion.

Following the doping process, a thin layer of silicon oxide is grown over the entire wafer surface, using dry oxidation. In this step, high purity oxygen gas, instead of steam, is pumped directly into a high temperature furnace. A second photolithography step is then used to open very small (contact) windows in this thin oxide layer, exposing the underlying doped silicon where electrical contacts will be made.

In order to form the electrical contacts, a thin layer of aluminum is deposited over the entire wafer surface (as well as inside the contact windows) through physical vapor deposition. The aluminum contacts are then defined using a final photolithography process in which all of the aluminum is removed expect for the contact pads over the contact windows. The devices are then ready for testing.

Testing

From the beginning it was expected that testing these devices would present the greatest challenge. Testing required us to overcome three major challenges: create a low noise environment, create the strong B-field required to generate the Hall Voltage, and increase the current flow through the Hall Effect device.

The first challenge was creating a low noise working environment. A considerable amount of time was dedicated to trying to identify the sources of noise and interference within the room. Whenever possible, equipment not in use was turned off. During some of our earliest experiments, we also turned off the fluorescent lights in the room because they were causing variations in our measurements as our shadow covered the silicon wafer under test. Eventually as we created stronger B-fields, higher currents, and more mechanically robust contacts, the Hall Voltage became large enough where fewer precautions were required.

The second challenge was creating the necessary B-Field that generates the Hall Voltage. We used permanent magnets as the source of our B-field because they were cheap and we would not have to worry about another power supply adding electrical noise to our environment. We originally borrowed some small permanent magnets from another department to do some preliminary experiments. These early experiments failed to produce any measurable Hall Voltage. From calculations based on the resistance of the channel of the Hall Effect device and the B-field strength, we determined we needed a much stronger magnet. We obtained two neodymium rare earth magnets (2.0 in. in diameter and 1.0 in. thick) with a surface flux density of 0.7 T and mounted them on a C-Clamp with one magnet on each of the jaws of the clamp. See Figure 2. The magnets were held in place by 3 inch diameter aluminum stock. Two identical sections were cut, and bored out so that one magnet could fit within each. The aluminum stock was bolted to the clamp and the magnets placed in the aluminum stock. Once the stock was bolted closed, encasing the magnets, the magnets were more easily handled.

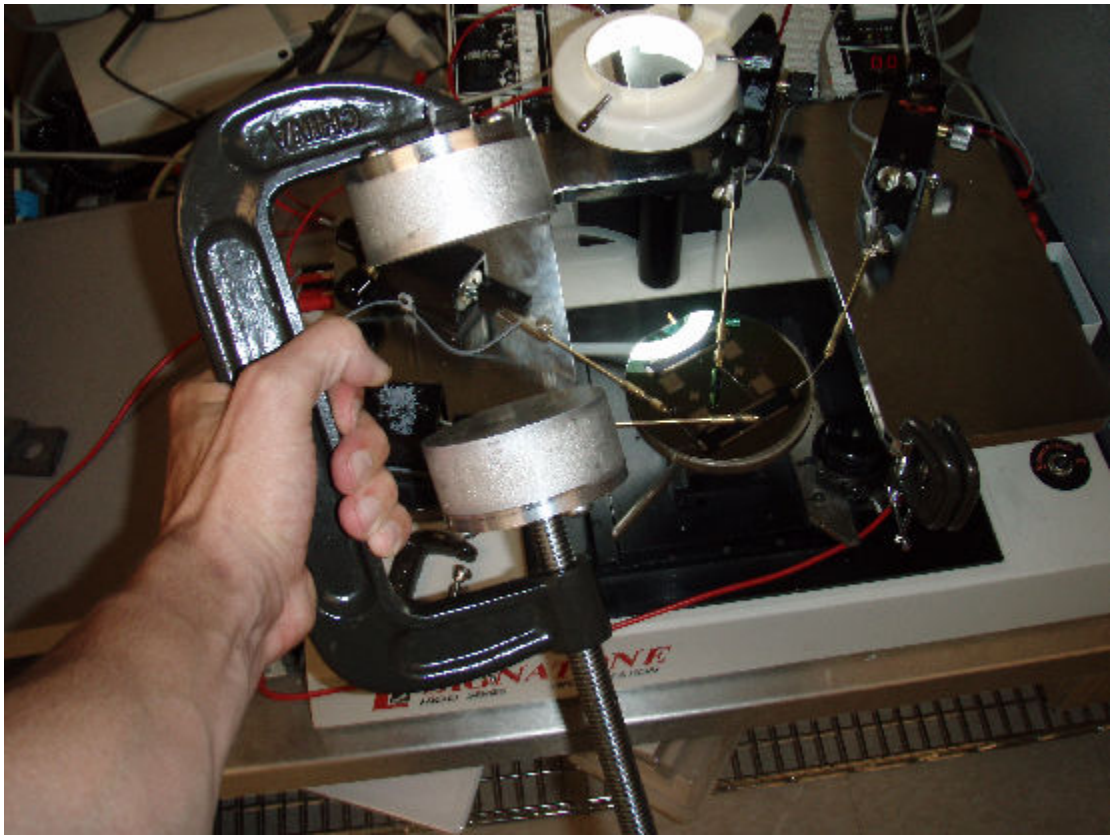

Figure 2: C-clamp with magnets

The final challenge was to increase the current flow through the Hall Effect device. Our first attempt at creating Hall Effect devices had several small devices on one wafer. After simple experiments did not yield any measurable Hall Voltage, we designed a new Hall Effect device with a wider and longer channel. The formula for the Hall Voltage predicted that the total current flow and the magnetic flux density were the important factors. So we used a larger channel so we could increase the total current flow without damaging the wafer by heat dissipation from the larger current flowing through the channel of the Hall Effect device. We also reduced the amount of doping because the formula for the Hall Voltage indicated that a larger sheet resistance would increase the Hall Voltage. Reducing the doping also increases the mobility and further increases the Hall Voltage. However, if the doping is too low, there will be nearly equal amounts of electron flow and hole flow: reducing the Hall Voltage.

With the improved Hall Effect device, we tried to increase the current from 100 mA to 1 A. However, our electrical contact was a steel needle touching aluminum deposited on the wafer. The higher current resulted in very high current densities near the contact point. The high current densities cause the aluminum to melt and electrical contact was lost. Our first attempt to improve the contact was to order special solder and flux to solder a wire to the aluminum contact. Unfortunately, the liquid solder dissolved the deposited aluminum and destroyed the contact pads. The final solution to obtain better contacts was to use conductive epoxy to attach a connector header to the conductor pad of the wafer. With the improved contact, we were able to achieve stable electric current flow of 0.3 A.

With the new Hall Effect device, we set the current to approximately 300 mA and measured the transverse voltage without any applied magnetic field. We measured a non-zero value because the channel has a voltage drop along the channel and if the transverse contact points are not precisely placed, the measured voltage will contain both a component caused by the voltage dropped along a portion of the channel and a portion caused by the Hall Effect. We also measured the transverse voltage with a magnetic field applied and recorded the difference as the Hall voltage. We applied the power supply so that conventional current flowed from left to right from the observer's point of view. We measured the transverse voltage with the positive terminal behind the channel (the channel was between the observer and the positive test point on the wafer). The negative terminal of the voltmeter was in front of the channel (the negative test point was between the channel and the observer). Finally we set the magnet so that the north pole of the field was on top and the south pole was on the bottom. Analysis of this configuration using the right hand rule shows that hole flow will produce a positive Hall Voltage while electron flow will produce a negative Hall Voltage.

Results

Consistent, repeatable Hall Effect voltages between 0.3 and 0.4 mV were observed. In addition, the polarity of the Hall Voltage was correct for the n-type material under test. We switched the polarity of the applied magnetic field and observed the sign change in the voltage. The maximum Hall Voltage for this device, based on theoretical calculations, is approximately 7 mV. This however, assumes a magnetic field density equal to the specified surface flux density of the magnet. Since we were moving the C-clamp with the magnets to apply and remove the magnetic

field, the gap between the north pole and the south pole had to be large enough to not touch the headers of the contacts (about 3 cm of gap). Taking into consideration the additional gap created by the aluminum stock holding the magnets, the applied magnetic field is considerably weaker than 0.7 T. As shown in the equation below, the Hall Voltage is also dependent on the mobility and sheet resistance of the device.

$$\left|V_H\right| = IB\mu R_s$$

Semiconductor device characterization techniques, including four-point probe analysis, provide only estimations of these terms, adding more uncertainty to attempts to calculate an accurate expected Hall Voltage. Nevertheless, despite the difficulties in predicting the magnitude of the Hall Voltage, the Hall Effect is clearly observed and the device will sufficiently serve as a class demonstration tool. Our next version of the Hall Effect device will move the contact locations out of the way so that the gap between the poles of the magnet can be reduced, thus strengthening the B-field. After that, we will experiment with making a p-channel Hall Effect device.

Expected Uses in the Classroom

As stated in the introduction, the purpose of this research project is to build a Hall Effect device to demonstrate different charge carriers of the electrical current flow in p-type and n-type semiconductor materials. All of the effort so far has been toward creating the n-type device. However, the solutions to the problems encountered with the magnetic flux density, the current density, and the doping levels are expected to be directly applicable to the p-type device. Hence, we expect only minor problems creating the p-type device. We are expecting some problems creating the p-type device because we have no experience doping silicon with p-type material with our laboratory equipment.

Eventually, the demonstration will consist of three Hall Effect devices: one with an intrinsic silicon channel, one with a p-channel conductor, and the final one with an n-channel conductor. Students will connect a power supply to the conductive channel of one of the wafers and use a voltmeter to measure the transverse voltage. A magnetic field from permanent magnets will be applied with a known north/south polarity and the students will observe the change in the transverse voltage caused by the magnetic field. The change in the voltage caused by the magnetic field is the Hall voltage. The students will use the right hand rule to determine the expected polarity of the Hall voltage and determine the type of semiconductor the conductive channel is made from (either intrinsic, p-type, or n-type). The students will repeat the experiment for each of the silicon wafers.

With the students observing that the polarity of the Hall voltage is determined by whether electrons or holes are the majority carrier in the semiconductor, it is hoped they will better understand the concepts of electron flow and hole flow. Once all of the Hall effect devices are built, pedagogical studies will be used to test the efficacy of the laboratory exercise.

Conclusions

It is feasible to build a Hall Effect device to determine the majority carrier of a doped channel of silicon material. Currently, we can consistently measure a Hall Voltage of about 0.3 mV, but we expect to improve on that by moving the contacts out of the way and reducing the gap between the poles of the magnet. Even if this does not affect the answer, we already have a design for the device that works well enough for a demonstration. Once we have perfected the Hall Effect devices, we will use them as a demonstration of semiconductor physics in an electronics course.

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