

Engaging Community College Students in Research using Summer Internship on Analysis of Performance Degradation of Integrated Circuits Due to Transistor Aging Effects in Nano-Scale

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Abstract

Integrated Circuits, or ICs, work behind the scenes to make people's lives better from common appliances, such as refrigerators and dish-washers, to the most sophisticated computers. IC performance has dramatically improved since their first creation. However, with scaling of ICs to Nano-scale, an ideal integrated circuit delivering reliable performance over its lifetime is almost impossible. All ICs experience degradation over time due to the aging of underlying transistors. Working on latest technology issues is typically an opportunity available only to graduate level students working on related research projects. To address this gap, using a NASA Curriculum Improvements Partnership Award for the Integration of Research (CIPAIR) grant, we have created a summer internship program that engages community college students in research projects on the latest challenges of circuit design in nano-scale semiconductor technology. Through this program, four community college students were mentored by two graduate students in a research project to analyze performance degradation of integrated circuits due to transistor aging effects in nano-scale. In this research, analysis of transistor breakdown is performed through computer simulations using the Custom Designer SE tool to understand effects on circuit power and performance. To simulate the effect of transistor breakdown, a ring oscillator circuit is utilized. This breakdown is modeled by resistors placed between the transistor terminals. The values of the resistors represent the severity of breakdown; large resistors represent fresh transistors, whereas low resistors represent a fully broken transistor. In addition to computer simulations, real ICs are studied by taking power measurements. This research aims to offer better insight into the impact of transistor breakdown and to improve IC design in Nano-scale.

I. INTRODUCTION

It is difficult to imagine life without integrated circuits because many aspects of civilization have become dependent upon them. The supercomputers, high-tech machines, and cutting-edge technology of today would not be possible without a simple switch known as the transistor. It is unbelievable how much IC technology improved in such a short time; the first IC had two transistors, but today's computers typically exceed a billion transistors. However,

designing more reliable, energy efficient, and high performing ICs in nanotechnology presents many difficulties. As transistor channels continue to shrink for better performance, problems such as transistor breakdown and instability arise and challenge today's computer scientists and engineers. It is important to study and prevent IC breakdown in order to continue technological growth.

Transistors have two main attributes: a high speed switch and an amplifier. The most simple model of a transistor is a faucet which can be turned on or off by a valve. In the case of digital circuits, transistors are either on or off with a delay in between the switching. As the size of transistors decreases, this delay decreases due to the time to activate.

Circuit designers and testers commonly use a circuit called a ring oscillator (RO), as shown in Fig. 1, to test new technology and reliability. ROs are created using an odd number of Complimentary Metal-Oxide Semiconductor (CMOS) Inverters because an even number of inverters will not allow the signal to oscillate. The output signal of the last inverter or stage is connected to the input signal of the first inverter forming a "ring".

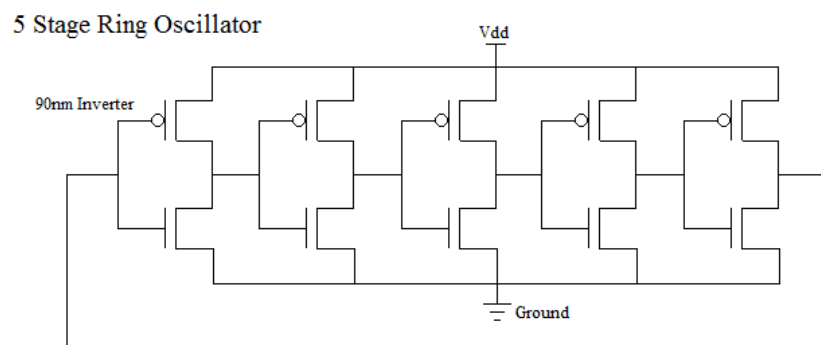


Figure 1. Schematic for 5 Stage Ring Oscillator

Each inverter is composed of two Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETS), which act as capacitors [1]. The inverter is the most fundamental construct of digital circuits. Its job is to take an incoming pulse and convert it to either high voltage or zero. This means that if a pulse has amplitude of 1.2V, the output of the inverter will be zero, or if the pulse has amplitude of zero, the output will be 1.2V.

When the RO is started with alternating potentials of high and zero volts at nodes between inverters, the signal starts to oscillate. The signal frequency is dependent on the transistor technology but most notably on the number of stages. Frequency and the number of stages are inversely proportional, so as the number of stages increases, the frequency of oscillation decreases.

All integrated circuits will experience degradation which can come in many forms. Soft Oxide Breakdown (SBD) is a type of degradation that involves the formation of traps in the gate oxide layer of the transistor. These traps, which are defects in the SiO_2 gate oxide, form conduction paths and develop leakage current from the polysilicon gate to the silicon substrate, as shown in Fig. 2. The leakage current affects the power consumption of the circuit even during its off state. There is debate about the formation of traps which includes: fabrication issues, hole creation, proton release, irradiation, and thermal damage [2].

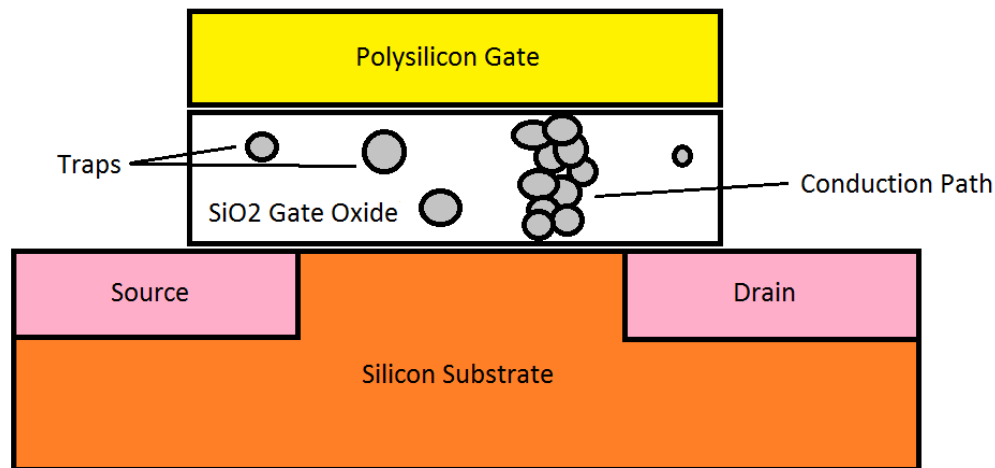


Figure 2. Cross Section of NMOS transistor showing traps and conduction path in the gate oxide region

Oxide breakdown has been investigated for various purposes, ranging from early-life failure (ELF), to the effect that breakdown has on performance of circuits [3 4]. Nan et al. analyzed the delay caused by SBD on a single gate of an inverter [4]. They used 32nm transistor technology, with a 0.9V supply voltage, and a constant resistance value of 100k Ω to model SBD. However, their work did not include a wider range of resistance values to better understand the effects of SBD on the performance of the circuit. As such, they were unable to see the decrease in performance up until the point that hard breakdown (HBD) occurs.

Working on latest technology issues is typically an opportunity available only to graduate level students working on related research projects. To address this education gap, using a NASA Curriculum Improvements Partnership Award for the Integration of Research (CIPAIR) grant,

we created a summer internship program to engage community college students in research projects on the latest challenges of circuit design in nano-scale semiconductor technology. Through this program, four community college students were mentored by two graduate students in a research project to analyze performance degradation of integrated circuits due to transistor aging effects in nano-scale. This paper presents the research conducted by these students on establish how SBD affects the performance of a circuit, specifically the delay variation and power consumption, in relation to location of the breakdown, and its severity.

II. APPROACH

The effects of leakage current through the transistors of integrated circuits are simulated by inserting a resistor into the RO circuit. Failures in the inverter can occur at four different locations, as shown in Fig. 3: NMOS/PMOS gate to source and NMOS/PMOS gate-to-drain. These failures are modeled by placing resistors at these locations one at a time. The values of the resistors determine the severity of the circuit degradation. It is expected that as this value decreases, the performance degrades proportionally.

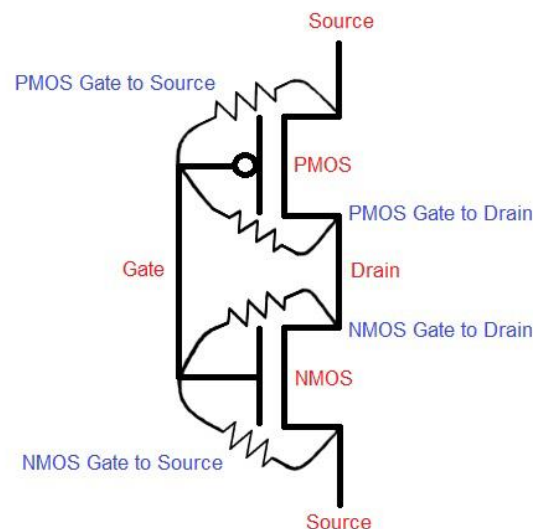


Figure 3. Locations of Leakage Resistors in the Ring Oscillator

SBD in logic circuits can be modeled by replacing multiple different logic gates in a specific path with a ring oscillator. This ring oscillator contains one inverter that contains a resistor at one of the four locations whose value varies from $1\text{M}\Omega$ down to $1\text{k}\Omega$. Three, five and seven stage ring oscillators are used to see if the effect of the inverter with SBD diminishes with

length. All of these circuits were created in Synopsys Galaxy Custom Designer and simulated using HSPICE.

Data on frequency, period, delay and average current were collected using measurement tools inside the WaveView software. Delay values were calculated by averaging the rise and the fall delays at 50% of maximum voltage as shown in Fig. 4. These delay values were only taken for the inverter that has SBD to compare to a fresh inverter. Each one of the variables had multiple values recorded and averaged to form the final tables and graphs.

An actual IC is analyzed using Cascade B11000 Probe Station and Agilent B1500A Device Parameter Analyzer. The Cascade B11000 probes the ICs and the Agilent B1500A records and analyzes data.

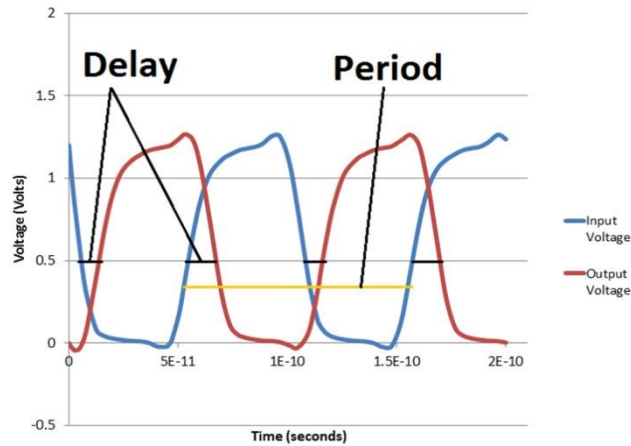


Figure 4. Delay, period, and frequency measurements

III. RELATIONSHIP BETWEEN LEAKAGE RESISTANCE AND TIME

Although the study provides valuable insight as to how ICs will break down, it does not indicate when breakdown will occur. It is important to understand when ICs will cease to work properly in order to improve the ways they are designed and manufactured. According to Afzal et al. [5], the relationship between Soft Breakdown Resistance R_{SBD} and time can be modeled by

$$R_{SBD} = \frac{V_{dd}}{I_0} \exp(-tGR) \quad (1)$$

where V_{dd} is the supply voltage, I_0 is the Initial leakage or defect current, and GR is the defect current growth rate. GR can be computed using the equation

$$GR = K_1 \exp(\theta_1 V_g - \theta_2 T_{ox}), \quad (2)$$

where V_g is gate stress voltage, T_{ox} is gate oxide thickness, and θ_1 , θ_2 , and K_1 are constants from experimental data.

Different values for GR are used: 1.6 , 3.2 , and $6.4 \times 10^{-8} \text{s}^{-1}$. These constant values are used because no industrial data are available for GR [5]. There are many proposed methods to calculate the initial defect current, I_0 . A voltage source was attached to an NMOS transistor, and it was observed the current that flows through the power source, which is also I_0 , as shown in Fig. 5.

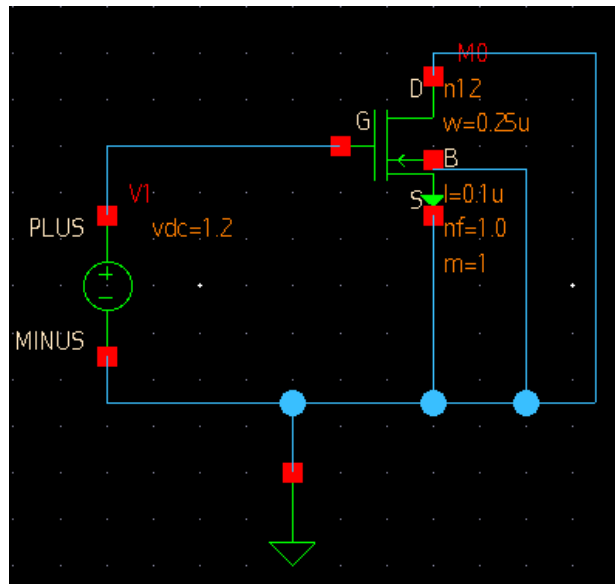


Figure 5. Set-up used to determine I_0

The current coming from the power supply behaves in an oscillating fashion. We use its average as our initial defect current, which is found to be 2.76 nA . Using the average defect current and 1.2V for V_{dd} , we are able to use Eq. 1 to create a plot that relates resistance and time, which is shown in Fig. 6. The value GR is an inherent characteristic of the circuit; hence, the lowest GR value represents a circuit with a very short life span, and the highest GR value represents a very durable circuit. It is also observed that the leakage resistance does not decrease linearly over time. Rather, it experiences exponential decay.

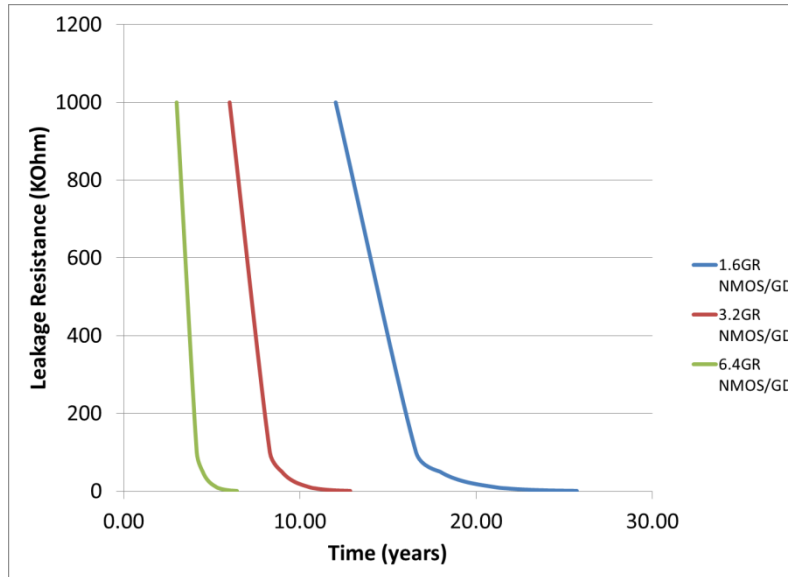


Figure 6. Leakage Resistance vs. Time for various GR values

IV. DELAY RESULTS AND ANALYSIS

A. NMOS/PMOS Gate-to-Source

The results shown in Fig. 7, from the three ring oscillator circuits with NMOS Gate to Source breakdown, show no perceptible difference in delay up to the 10 k Ω average life limit. The measurements show an average change of 1-2 ps in period which is an insignificant change in performance. This difference is not enough to cause the calculation to be completed after the clock cycle because it falls within a minimum clock error of 10 ps.

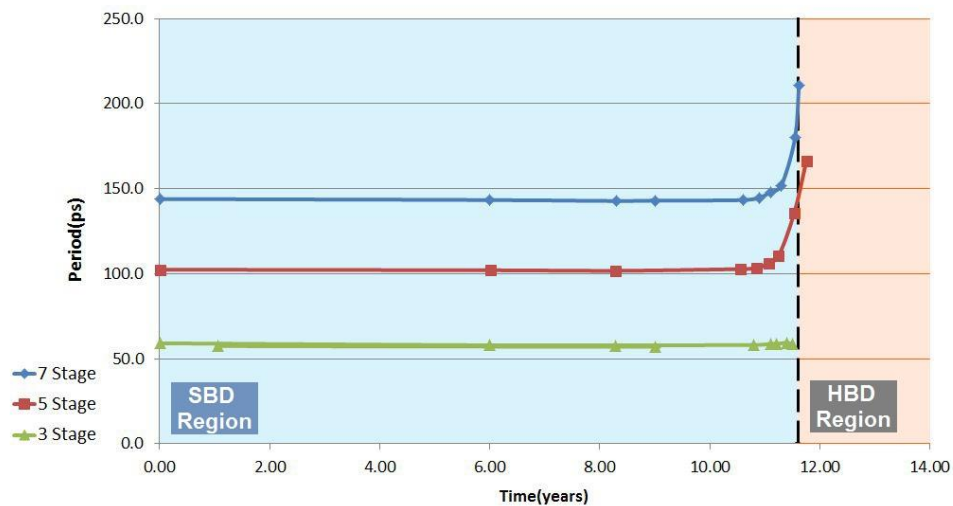


Figure 7. NMOS Gate-to-Source Period vs. Time

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Significant differences occur when the inverter is close to HBD at about 3-4 k Ω , which causes the circuit to fail completely. These failures correspond to about 11-12 years of use, which is more than double the time a typical consumer will use a device.

Delay at the level of the single inverter has increased significantly, but as the number of stages increase, the effect diminishes quickly as shown in Fig. 8. The increase may be critical when a circuit has aged evenly where all transistors have had breakdown. If a main path in a logic circuit were to undergo even SBD, the cumulative effects would be significant enough to cause problems with calculations falling outside of the clock error. Further study is required to see how overall delay or period increases with the addition of more inverters with breakdown.

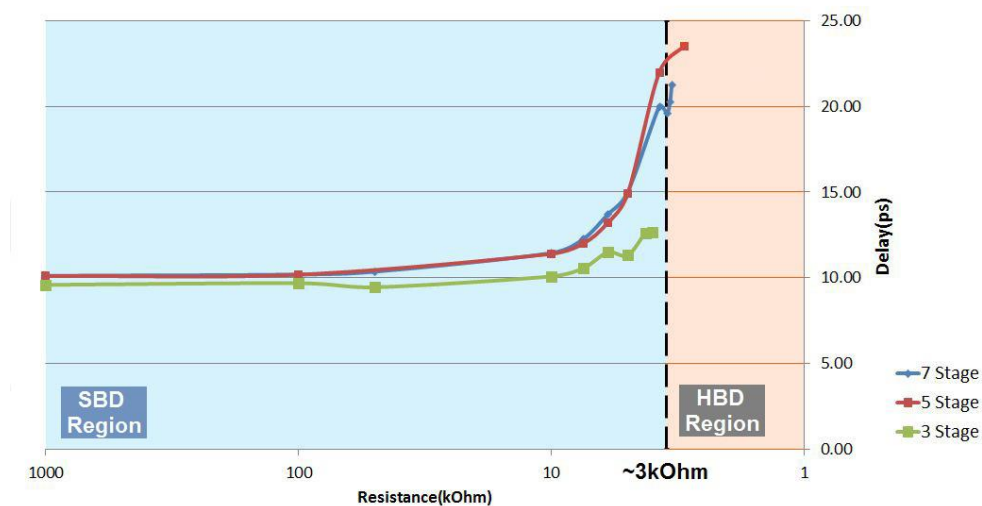


Figure 8. NMOS Gate-to-Source Delay vs. Resistance

According to Choudhury et al. [6], PMOS breakdowns are less likely to be seen because the time to breakdown is one order of magnitude greater than that of the NMOS. The delays, frequencies, and power are very similar to the NMOS as shown in Figs. 7 and 8, so it is believed that further study should be focused on the NMOS failure.

NMOS/PMOS gate to source results can be explained with an analog circuit shown in Fig 9. As the pulse train enters the inverter, shown as current source, some of the current flows to the capacitor but some also flows through the resistor to ground. This causes an increased delay in the charging of the capacitor, which means the rise and fall delays of the waveforms increase. In short, as the resistance decreases the delay increases so the frequency decreases proportionally.

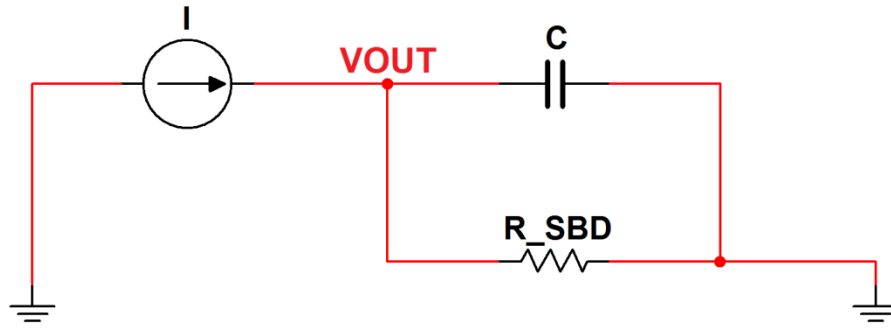


Figure 9. NMOS/PMOS gate-to-source model

B. NMOS/PMOS Gate-to-Drain

Since PMOS and NMOS gate-to-drain yielded identical results due to resistors being connected to same nodes, data for both cases were combined. The three simulations show that an increase in performance is possible when a gate-to-drain breakdown occurs as Table 1. It shows the period on average decreases by 8%. This most likely should not be the focus of future research because it does not negatively affect the circuit.

90nm Ring Oscillator – NMOS/PMOS Gate-to-Drain				
Type	Period(No SBD)	Period(10k Ohm)	Difference	% Difference
3 Stage	59	52	7	11.9
5 Stage	102	97	5	4.90
7 Stage	144	132	12	8.33

Table 1. NMOS/PMOS difference between fresh oscillator and one with single breakdown

Delay of the single affected inverter shown in Fig. 10 does show increase in performance because of the decrease in delay. The change in delay is similar to gate to source, but it seems to have a larger effect on the overall circuit as shown by the period.

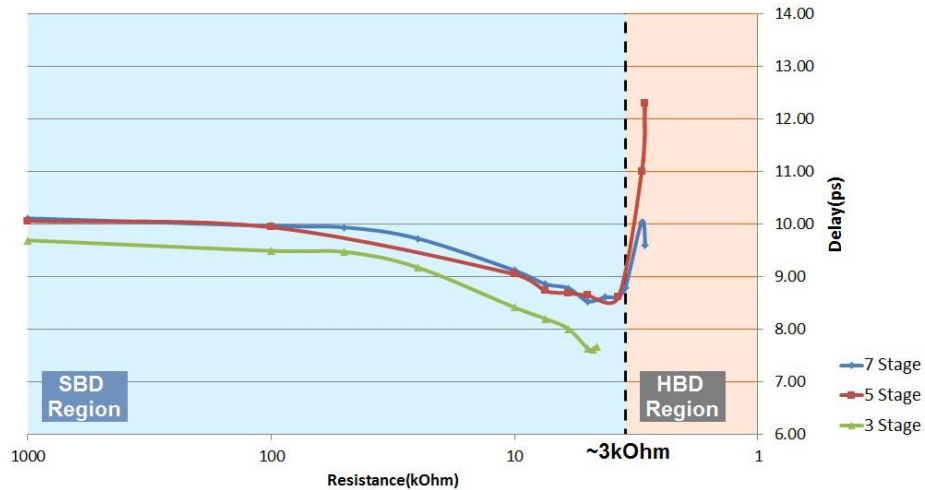


Figure 10. NMOS/PMOS Gate-to-Drain Delay vs. Resistance

The data for the gate-to-drain simulations can be explained with a simpler analog circuit shown in Fig 11. Initially the inverter is turned on, thus a current I_P flows through the resistor helping to charge the capacitor, so $I_C = I + I_P$. I_P switches direction when the inverter switches which slows the charging of the capacitor, thus $I_C = I - I_P$. Large values of R_{SBD} show that the first case is stronger than the second because the delay decreases. As the value decreases close to 5 k Ω , the second case overtakes the first so delay increases rapidly.

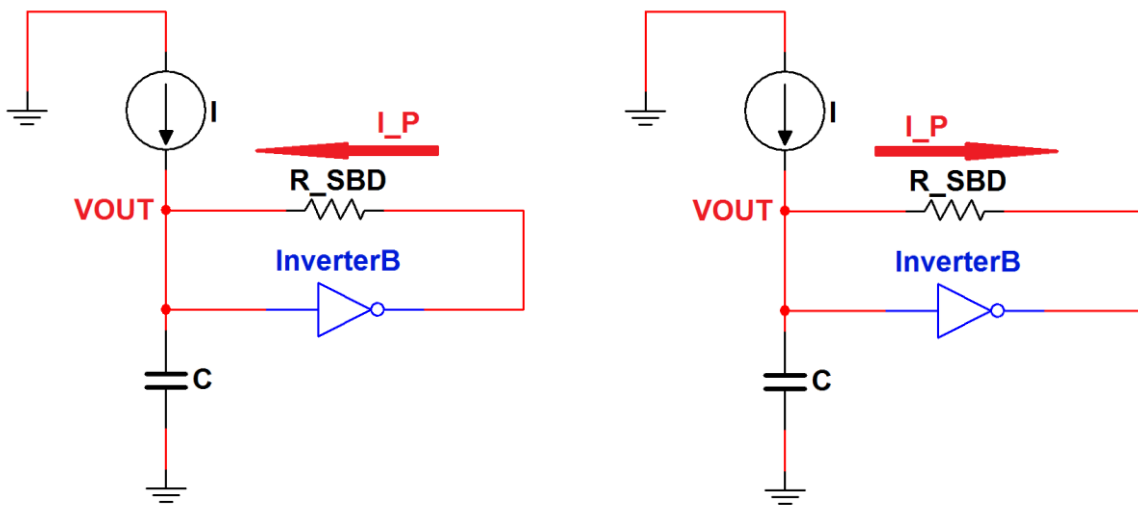


Figure 11. NMOS/PMOS gate-to-drain model, current helping charge (left), resistor taking current (right)

C. Unexpected Results

The three stage results for all of the resistor positions show some unexpected results. The waveforms appear to be damped because they oscillate until their amplitudes reach zero after a short period of time of about 0.5 ns. The frequency and period data remain relatively flat until the breakdown point, which was unexpected because it was believed that the shorter ring oscillator would accentuate the delay differences. We were expecting to still see the rise or drop of frequency, period, and delay that was seen with the seven and five stage ROs.

An interesting difference between the three ring oscillator results seems to be the time when hard breakdown occurs. The exponential increase in period appears to come sooner when the number of inverters increases, such as from five to seven stages. Further study may be needed to see if this is true for circuits longer than seven stages.

V. POWER RESULTS AND ANALYSIS

A. Gate-to-Source

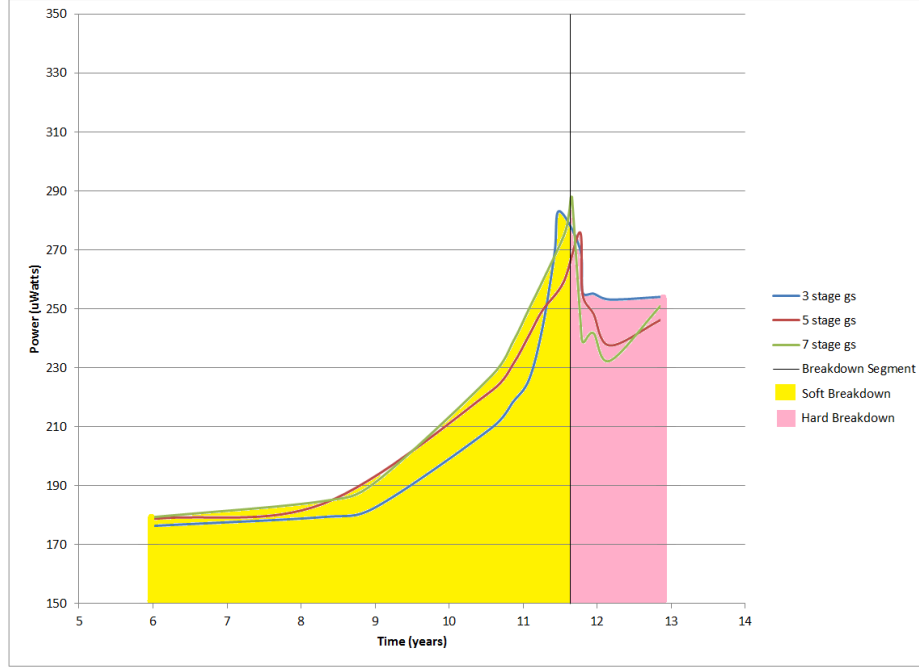


Figure 12. Power vs. Time for Gate-to-Source Breakdown

$$P_{total} = P_{sw} + P_{leakage} \quad (3)$$

The total power consumption for breakdown that occurs in the Gate-to-Source (GS) region can be modeled by Eq. 3. The switching power P_{sw} is the power consumed by the inverter as it switches signals. The transistors in the inverter act as capacitors, so there is a finite time for them to be fully charged and invert the input signal. This charging sequence is one of the reasons for the dissipation of power.

$$P_{sw} = f * C * V_{dd}^2 \quad (4)$$

$$P_{leakage} = V_{dd} * I_{leakage} = V_{dd}^2 / R_{sbd} \quad (5)$$

To understand leakage power $P_{leakage}$, it must be noted that there is no such thing as a perfect IC. Due to breakdown, there is current leaking from the gate to other regions, such as the source region. This leakage current increases as circuit degradation gets worse.

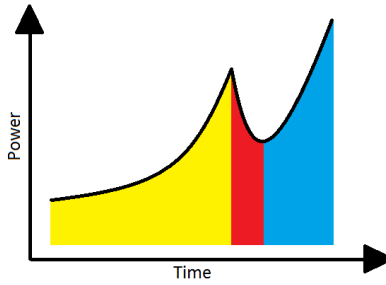


Figure 13. Power Consumption behavior for Gate-to-Source Breakdown

The data collected from the simulations of ring oscillators with various stages show a curve that predicts power consumption over time, as shown in Fig 12 (actual data) and Fig 13 (pictorial representation). The yellow region shows a non-linear increase in total power. This region is the SBD region, where the switching power is constant and the leakage power rises as R_{sbd} decreases. HBD begins in the red region, where the period of the IC rises dramatically until it reaches infinity. Since period is the reciprocal of frequency, the switching power goes to zero, and the power consumption drops significantly. R_{sbd} is still decreasing, which means the leakage power continues to increase. Even though the switching power no longer contributes to total power consumption, leakage power is still growing, hence the rising curve in the blue region.

B. Gate-to-Drain

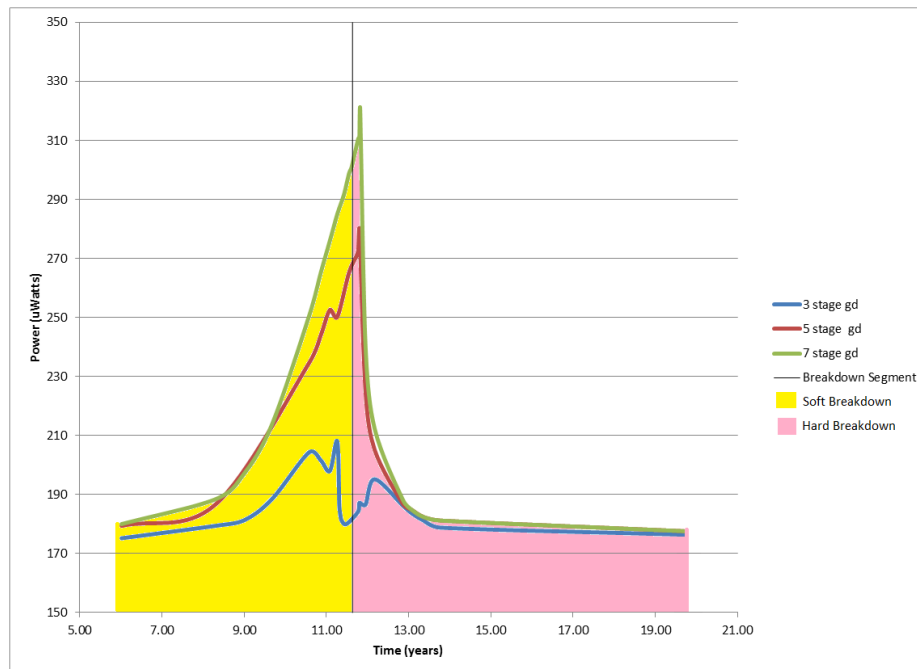


Figure 14. Power vs. Time for Gate-to-Source Breakdown

In contrast to the GS graph, the Gate-to-Drain (GD) breakdown shows interesting behavior in the HBD region. From the data gathered, a Power-Time pattern is created, as shown in Fig 14 (actual data) and Fig 15 (pictorial representation).

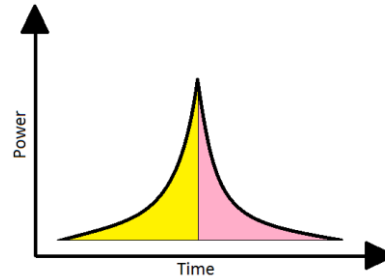


Figure 15. Power Consumption behavior for Gate-to-Drain Breakdown

The yellow region in Fig. 15 represents the SBD region. Similar to GS breakdown, as the value of R_{sbd} decreases, the leakage current increases, thus overall power consumption rises. When HBD begins, total power consumption decreases until it reaches a steady state, as shown in the pink region.

C. Different Power Behavior for Severe HBD

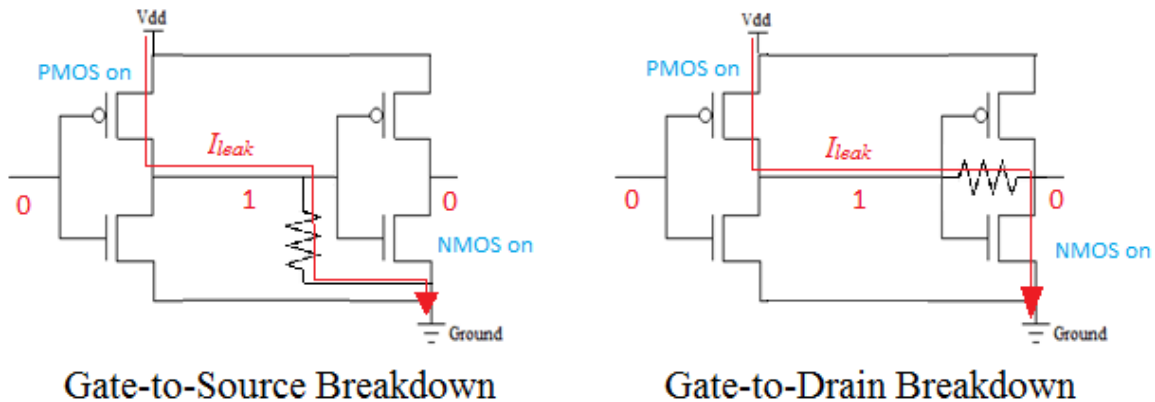


Figure 16. Leakage current paths for GS and GD breakdown

In Figs. 12 and 14, the significant increase in power in GS breakdown that is not present in GD breakdown can be attributed to the different pathways of the leakage current. In GS breakdown, the leakage current flows across the leakage resistor and PMOS transistor that acts as a resistor in its on-stage. Although there is increased resistance due to the PMOS transistor, the leakage current is still able to flow from V_{dd} to ground. Hence, total power consumption for GS breakdown increases again, as shown by the blue region in Fig. 13.

In GD breakdown, the leakage current I_{leak} flows across the PMOS transistor, leakage resistor, and NMOS transistor. It is more difficult for the current to flow compared to GS breakdown. The leakage power for GD breakdown becomes,

$$P_{leakage} = V_{dd}^2 / (R_{sbd} + R_{PMOS} + R_{NMOS}) \quad (6)$$

The high resistance reduces the leakage current significantly so that its effect on total power consumption can be neglected.

After HBD, further decrease in leakage resistance no longer affects the circuit, and total power consumption is simply given by

$$P_{total} = f * C * V_{dd}^2 + V_{dd}^2 / (R_{PMOS} + R_{NMOS}) \quad (7)$$

Because total power is independent of leakage resistance, all of the ring oscillator curves converge to some constant power value, regardless of the number of stages in the IC.

D. Initial Leakage Current Effect on Power

For both GS and GD breakdown, it is observed that as the number of inverters in the ring oscillator increases, the area under the Power curve gets larger. To explain this behavior, the effects of initial leakage current must be considered.

The initial leakage current I_0 is an inherent characteristic, which is caused by imperfections in the IC. Also, as IC design gets better, the Gate Oxide region gets smaller, which contributes to the increase in current tunneling. It is not the same as leakage current caused by breakdown. Total leakage current is the sum of breakdown current and initial leakage current. Each inverter in the ring oscillator has its own initial leakage current; therefore, total leakage current is,

$$I_{leakage} = I_{bd} + n * I_0 \quad (8)$$

In Eqn. 8, I_{bd} is the breakdown current and n is the number of inverters in the ring oscillator. Incorporating this initial leakage current effect, Leakage Power becomes,

$$P_{leakage} = V_{dd} * I_{leakage} = V_{dd} * (I_{bd} + n * I_0)$$

$$P_{leakage} = (V_{dd}^2/R_{sbd}) + (n*V_{dd}*I_0) \quad (9)$$

Total power consumption is dependent on the number of inverters in the ring oscillator, which explains why the seven stage ring oscillator consumed the most power and had the largest area under its power curve among the ring oscillators that were tested.

VI. EXPERIMENTAL RESULTS

This portion investigates the validity of the simulations conducted on the computer program. Using the Cascade B11000 Probe Station and Agilent B1500A Device Parameter Analyzer, the test chip was probed at its voltage and ground nodes while applying 1.8V at 20°C provided by the Source Monitor Unit (SMU), and produce the I-V graph for the fresh test chip. The chip is then stressed with the Semi-Conducting Pulse Generator (SPGU) at 3.5 V at 140°C for approximately one hour at 90% duty cycle with 1ms period to accelerate the process of SBD. After stress, the chip was probed to original quantities and its I-V graph was made. The same process was performed except at 100°C and a graph was created. Fig. 17 represents the defect current of the chip due to the breakdown.

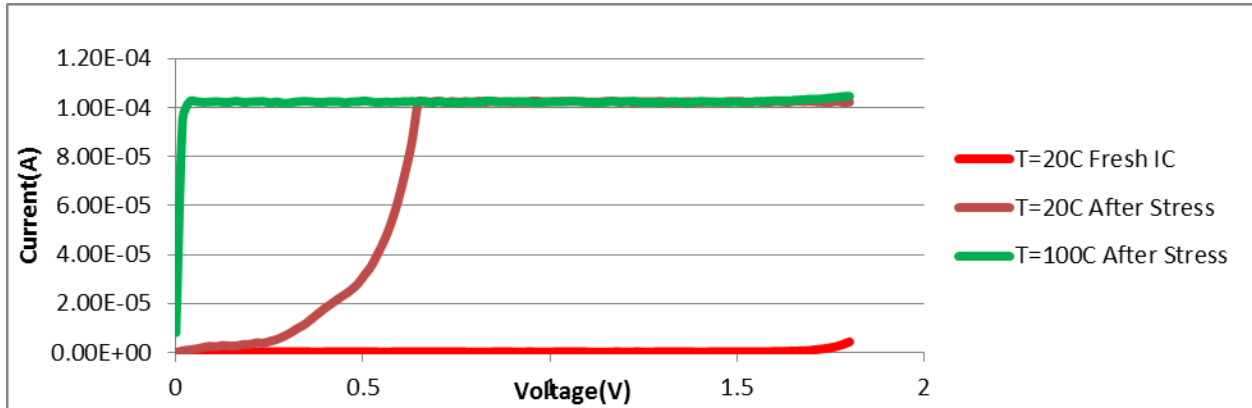


Figure 17. I-V characteristic of fresh IC and IC after stress



Figure 18. Power supply section of chip under test

VII. STUDENT SURVEYS

Table 2 summarizes the results of post-program student survey designed to measure perception of over-all usefulness of the research internship program. Results show that the research internship program was successful in its achieving its goals of helping students prepare for transfer, solidify their choice of major, increase their confidence in applying for other internships, and enhance their interest in pursuing graduate degrees. Overall, students were satisfied with the program, and would recommend it to a friend.

The internship program was successful in achieving its goals of developing students' skills needed for academic success. Table 3 shows a summary of student perception of how much they have learned from participating in the internship program, as determined from a post-program survey. Note that for each of the categories, the average response is between "Quite a bit" and "A lot."

Table 2. Summary of student responses to the post-program survey measuring the perceived benefit of participating in the research internship program.

Question: Tell us how much you agree with each of the following statements. Response Scale: 1 – Strongly Disagree; 2 – Disagree; 3 – Neutral; 4 – Agree; 5 – Strongly Agree.	
	Average Rating
The internship program was useful.	4.9
I believe that I have the academic background and skills needed for the project.	4.1

The program has helped me prepare for transfer.	4.5
The program has helped me solidify my choice of major.	4.3
As a result of the program, I am more likely to consider graduate school.	4.6
As a result of the program, I am more likely to apply for other internships.	4.8
I am satisfied with the NASA CIPAIR Internship Program.	4.8
I would recommend this internship program to a friend.	4.8

Table 3. Summary of student satisfaction with the summer research internship program.

Question: How much did you learn about each of the following? Response Scale: 1 – Nothing; 2 – A little; 3 – Some; 4 – Quite a bit; 5 – A lot.	
	Average Rating
Performing research	4.8
Designing/performing an experiment	4.9
Creating a work plan	4.8
Working as a part of a team	4.8
Writing a technical report	4.8
Creating a poster presentation	4.7
Making an oral presentation	4.6
Performing research	4.8

VII. CONCLUSION

Adding resistors to the IC produces reliable approximations to the effects of SBD. The equation relating leakage resistance to time allows our circuit model to behave like a typical integrated circuit.

The results of the gate to source individual delay and the total period of the three, five and seven stage ring oscillators show no perceptible difference up to the hard breakdown point.

The gate-to-drain data shows a much larger change of about 8%, which is shown as an increase in performance rather than a decrease. We conclude that delayed multisampling is not possible due to the small differences in delay and period.

This research confirms that power consumption increases due to the growing leakage current from SBD. It has been observed that there is a point, called Hard Breakdown Point, where power consumption actually starts to decrease. Experimental results support our observations by simulations.

Our research goes beyond the scope of prior research by analyzing the circuit behavior as the SBD progresses to HBD. The HBD behavior is different for GS and GD breakdowns. In the BD region the delay continues to increase until the circuit fails. The power shows an irregular behavior depending on the location of the breakdown.

VIII. BIBLIOGRAPHY

- [1] B. Van Zeghbroeck. "The MOSFET – Introduction." Internet: <http://ecee.colorado.edu/~bart/book/mosintro.htm>, 1997 [July 11, 2012]
- [2] N. Azizi. "Gate Oxide Breakdown". December 2, 2003.
- [3] T. Chen, Y. Kim, K. Kim, Y. Kameda, M. Mizuno, S. Mitra. "Experimental study of gate oxide early-life failures," IEEE International, Reliability Physics Symposium, 2009.
- [4] H. Nan, L. Li, K. Choi. "TDDDB-Based Performance Variation of Combinational logic in Deeply Scaled CMOS Technology," 13th International Symposium, Quality Electronic design (ISQED), 2012.
- [5] B. Afzal, B. Ebrahimi, A. Afzali-Husha, H. Mahmoodi. "Modeling read SNM considering both soft oxide breakdown and negative bias temperature instability"
- [6] M. Choudhury, V. Chandra, K. Mohanram, R. Aitken, "Analytical model for TDDDB-based performance degradation in combinational logic", Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 423-428, 2010.