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From Theory to Implementation: Meeting Industry Needs through University & Community College Collaboration in Digital Logic Design Progress Report

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Abstract

Hardware Description Language and Field Programmable Gate Array (FPGA) have revolutionized the way Digital Logic Design is taught and implemented. Traditional ways of teaching logic design using discrete components (TTL: Transistor-Transistor Logic and CMOS: Complementary Metal Oxide Semiconductors) have been replaced by Programmable Logic Devices (CPLD: Complex Programmable Logic Devices and FPGA) [1, 2, 3]. Today, a more standard development process is widely used in industry. The process uses Hardware Description Languages as a design entry to describe the digital systems. The two most widely used Hardware Description Languages in industry are VHDL (Very High Speed Integrated Circuit Hardware Description Language) and Verilog (Verifying Logic). Although most traditional electrical and computer engineering programs have updated their curriculum to include topics in hardware description language and programmable logic design (FPGA/CPLD), two-year and four-year electrical engineering technology programs have fallen behind and are moving slowly in updating their curriculum. A survey of 107 two-year electrical engineering technology programs and 52 four-year electrical engineering technology programs showed that only 16.5% of two-year and only 19.5 % of four-year programs in electrical and computer engineering technology at US academic institutions currently have a curriculum component in hardware description language and programmable logic design [5]. Clearly, electrical engineering technology programs are far behind in teaching the skills that represent current and future industry needs. The School of Technology at Michigan Technological University in partnership with College of Lake County is stepping up to this challenge by developing and introducing curriculum in hardware description languages and programmable logic design. This paper will discuss the curriculum development and course assessment results at Michigan Technological University Electrical Engineering Technology Program and The partner Community College. The paper also addresses project activities including the two-day Faculty Professional Development workshop on VHDL and FPGA design implemented in December 2012, assessment results and lessons learned, and finally, the undergraduate research experience at Michigan Technological University.

I. Introduction

Programmable Logic Devices in general and FPGA-based re-programmable logic design became more attractive as a design media during the last decade, and as a result, industrial use of FPGA in digital logic design is increasing rapidly. Considering the following technology trend in industry, the need for highly qualified logic designers with FPGA expertise is increasing rapidly. According to the United States Department of Labor, the job outlook is on the rise and will continue to expand for at least the short- to medium-term future [9]. To respond to the industry needs for FPGA design skills, universities are updating their curriculum with courses in hardware description languages and programmable logic design. Although most traditional electrical and computer engineering programs have updated their curriculum to include topics in hardware description language and programmable logic design (FPGA/CPLD), only 19.5 % of 4-

year and 16.5 % of 2-year electrical and computer engineering technology programs at US academic institutions currently have a curriculum component in hardware description language and programmable logic design [5]. To effectively meet the next generation's workforce needs, the electrical and computer engineering technology curriculum must be current, relevant, and teach technology that is widely used in industry. To meet this goal, we propose a curriculum development in the electrical engineering technology program digital logic design series. This curriculum revision incorporates the addition of two new courses that added to the current course (Digital Electronics). As a result, the EET program introduced two new courses (Digital Design Using VHDL and Topics in Programmable Logic). Each of these courses is three credit hours (2 class, 3 lab). Faculty involved in developing and teaching the new curriculum must be well-informed of advances in technology currently used in industry. Likewise, industry wants to have qualified and well-educated employees coming out of academia who are ready to implement their knowledge on day one of their employment. As a result, while academia needs to be fully aware of the current state-of-the-art knowledge requirements, industry must be driving the curriculum development. Therefore, in this curriculum development, a strong link between academia and industry must be established. This partnership is a "two-way street" and advantageous for both parties. The Electrical Engineering Technology (EET) program in the School of Technology at Michigan Tech University is collaborating with Altera University program in which the involved faculty members attend a set of Altera training workshops. These workshops are targeted toward professional individuals and college faculty seeking knowledge and expertise in programmable logic design. Faculty members having the opportunity to attend these workshops gain the knowledge and expertise to teach both VHDL digital Design and Programmable Logic (FPGA) design courses. The exposure to industry-taught courses will help the faculty members to impact the learning experience of his/her undergraduate students by providing them with skills that are highly marketable and appreciated by industry.

II. Curriculum Development at Michigan Technological University

Figure 1 shows the current and proposed digital design logic sequence which incorporates the addition of two new courses that will be added to the current course (Digital Electronics). The EET program will introduce two new courses (Digital Design Using VHDL and Topics in Programmable Logic). Each of these courses is three credit hours (2 class, 3 lab). The descriptions of the two new courses are provided below. We are able to add the two new courses without impacting the overall degree plan. The current EET program has a shortage of courses in digital logic design; only one course (Digital Electronics) is currently offered. The EET program will still be structured as a 127 credit hour program with sixty-eight (68) credits of technical courses in Electrical Engineering Technology. This is in line with ABET requirements [10]. ABET Criterion **5. Curriculum: "**Baccalaureate programs must consist of a minimum of 124 semester hours … and the technical content is limited to no more than 2/3 the total credit hours for the program" [10].

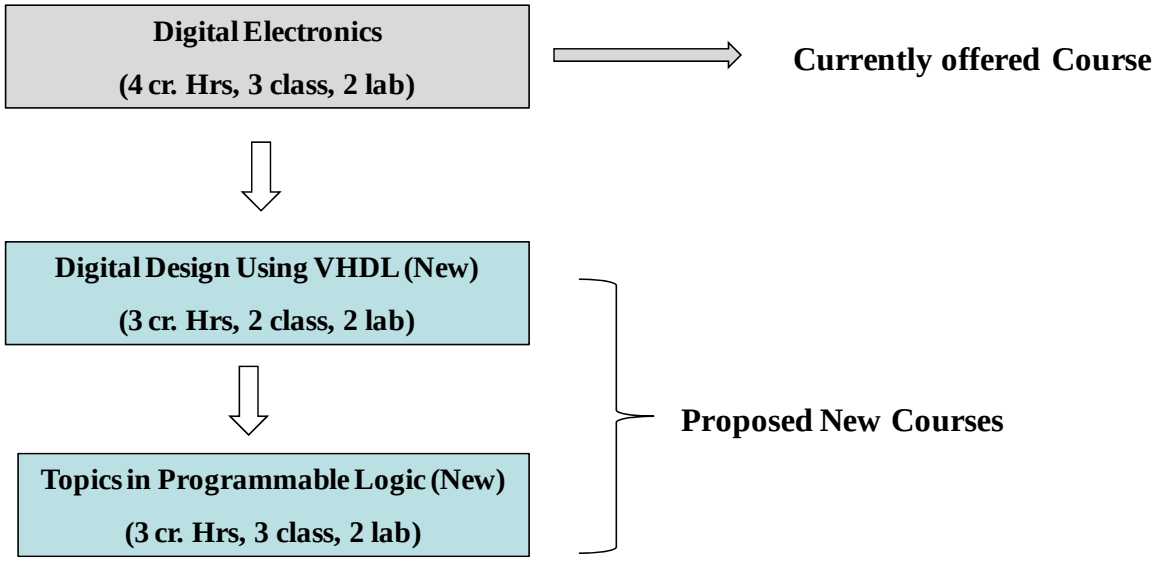

Figure 1: Proposed Digital Logic Design Courses Sequence

<u>New Course 1: Digital Design Using VHDL</u> (3 Cr hrs, Class 2 hrs, Lab 3 hrs)

Course Objectives

The course places an emphasis on the language concepts of digital systems design using Hardware Description Language (VHDL). The course will focus on good digital design practices and writing testbenches for design verification. Low-level gate modeling techniques with varying timing details will be presented, as well as structural level of abstraction for wiring predefined gates and other predefined components. The information gained can be applied to any digital design by using a top-down design approach. Students will gain valuable hands-on experience in writing efficient hardware designs using VHDL and performing high-level HDL simulations.

The academic objectives of the "Digital Design using VHDL" course are to provide students with skills and experience that will help them to be attractive in the job market and as employees with high-value skills in the workplace. The students will learn the design of major components of digital systems, such as arithmetic logic units (ALUs), floating points, memory, and controller using hardware description language (VHDL). In addition, the students will learn FPGA design flow starting from HDL design entry and circuit simulation to verify the correctness of the intended design, writing testbenches. To accomplish this in a one-semester course, the intent of lectures and labs is to have the students:

1. Gain the knowledge on programmable logic devices (PLD) and their design methodologies
2. Learn fundamental concepts of hardware description language
3. Learn how to use HDL for modeling basic building blocks of digital system
4. Learn about different design entry methods
5. Learn how to model digital circuits in hardware description languages
6. Learn how to use VHDL editors, debug designs and perform logic simulation
7. Learn how to use Altera's Quartus® II development software[4]
8. Learn how to perform timing analysis and verification

Course Structure
The course "Digital Design using VHDL" is three credit hours with two hours per week of recitation and three hours per week in the lab. The course will be open for sophomore or higher students and the pre-requisite is "Circuits I" and "Programming Languages". The course will integrate Altera's Quartus® II development software, and the lab will use Altera's DE2 FPGA evaluation board [1, 2, 3, 4].

The second class offering of Digital Design using VHDL was conducted in spring 2012 with a total of twelve enrolled students, continuous improvement actions were implemented as a result of the first class offering conducted in spring 2011. As part of the assessment, a course survey was used to obtain student feedback regarding instruction. There are a total of twenty questions in the survey: the first eighteen questions are based on best practice and cover not only curriculum but also classroom and lab facilities; the question 19 and 20 are intended to elicit students' feedback on their overall assessment of the instruction. Students were also encouraged to provide written comments to further improve the teaching practice. Students also rated how well the course objectives were achieved on a scale of 1 to 5 with 5 being Strongly Agree and 1 being Strongly Disagree. Table 1 reflects student feedback regarding access to new, effective curriculum modules and labs that more accurately reflect the needs of industry. Overall feedback was extremely positive.

Measurable Outcomes	**Overall Rate**
Students will learn how to model basic digital circuits in hardware description languages.	4.60
Students will learn how to use VHDL to model common digital hardware circuits - combinational and sequential circuits	4.80
Students will learn how to use to use VHDL CAD Tools (editors, debug designs and perform logic simulation).	4.60
Students will learn how to write test benches to verify the design and perform timing analysis of a given design	4.80
Students are more interested in the subject now than they were before they took the class	4.50
The classroom and equipment were adequate to support effective learning	4.60
Instructional resources (textbook, handouts, etc.) furthered learning	4.50
The instructor made students aware of the specific goals of the course	4.67
Given the opportunity, I would take another course from this instructor	4.83
Taking everything into account, I consider this instructor to be an excellent teacher	4.83

Table 1: Students' feedback assessment results

<u>New Course 2: Topics in Programmable Logic Design</u> (3 Cr hrs, Class 2 hrs, Lab 3 hrs)

Course Objectives
Due to industry's increased demand for FPGA designers, the intention of this course is to give students real-world experience in FPGA logic design and provide with the necessary training in design tools widely used in industry. Tools used will include Altera's Quartus® II development

software and FPGA design implementation on Altera's DE2 FPGA evaluation board [1, 2, 3, 4]. The long-term objective of this course is to provide a learning opportunity that will result in research activities focused on FPGA design. This research will provide more in-depth training for senior students and engage undergraduate students in applied research opportunities.

The academic objectives of the FPGA logic design course are to provide students with skills and experience in the FPGA design process. The students will learn the FPGA design flow using Quartus® II [4] development software to develop an FPGA, starting from HDL design entry, circuit simulation followed by FPGA Synthesis for Altera FPGA devices, Place and Route and timing analysis. To accomplish this in a one-semester course, the intent of lectures and labs is to have the students:

1. Learn how to use HDL for modeling basic building blocks of digital system
2. Learn FPGA technology and the impact of using FPGA in logic design
3. Learn FPGA design flow using Altera's Quartus® II development software
4. Gain FPGA design experience by synthesizing, mapping, and placing and routing a given design on Altera's DE2 FPGA evaluation board
5. Work in groups of two or three and thereby learn how to cooperate in teams
6. Learn to document their results

The designs are carried out using modern computer-aided design (CAD) tools, and the Altera's Quartus® II development software [2]. The final systems will be implemented with state of the art devices such as the Altera FPGA device family and micro-controllers. Altera's DE2 evaluation boards will be used as the target platforms.

Course Structure

The course "Topics in Programmable Logic" is three credit hours with two hours per week of recitation and three hours of lab. The course is open to senior students and the pre-requisite is "Digital Design using VHDL". The course will integrate Altera's Quartus® II development software. The lab will use Altera's DE2 FPGA evaluation board, the FPGA boards will be used as target platforms for lab experiments. Students will learn how to implement a complete system on the FPGA evaluation boards.

Altera Corporation represents a market leader and holds a large market share in programmable logic. Each FPGA vendor development software is device dependent, for example, Altera's Quartus® II development software only targets Altera's device family. Learning Altera's Quartus® II development software will give students the opportunity to learn FPGA design flow using the most widely used tools for FPGA design. At the same time, these skills are largely transferable to other design tools, so students will learn valuable skills useful across industrial platforms.

The first class in VHDL was developed and conducted in fall 2011 with a total of six enrolled students. As part of the course assessment, a course survey was used to obtain student feedback regarding instruction. There are twenty questions on the survey, the first eighteen questions are based on best practice and cover not only curriculum but also classroom and lab facilities. On the other hand, question 19 and 20 are intended to elicit students' feedback on their overall assessment of the instruction. Students are also encouraged to provide written comments to help

improvements of the teaching practice. Students were asked to rate how well the course objectives were achieved on a scale of 1 to 5 with 5 being Strongly Agree and 1 being Strongly Disagree. Table 2 reflects student feedback regarding access to new, effective curriculum modules and labs that more accurately reflect the needs of industry. Overall feedback was extremely positive.

Measurable Outcomes	**Overall Rate**
Learn how to use HDL for modeling basic building blocks of digital system	4.75
Learn FPGA technology and the impact of using FPGA in logic design	4.75
Learn FPGA design flow using Altera's Quartus® II development software	4.75
Gain FPGA design experience by synthesizing, mapping, and placing and routing a given design on Altera's DE2 FPGA evaluation board	4.25
Work in groups of two or three and thereby learn how to cooperate in teams	4.50
Gain a basic understanding of timing analysis	3.50
Learn how to build SDC files for constraining FPGA designs	3.75
Learn how to verify timing on simple design using the TimeQuest analyzer	3.50
Learn FPGA design flow using Altera's Quartus® II development software	3.75

Table 2: Students' feedback assessment results

III. Curriculum Development at College of Lake County

To develop curricular resources that will be of value at all levels of engineering technology education, Michigan Technological University and the College of Lake County have partnered on this curriculum development. With this partnership, course enhancements will affect both two-year and four-year EET programs. In addition, the partnership will enable us to develop and test resources with diverse student groups across two initial institutions.

The current electrical engineering technology program curriculum includes one 4-credit course (Introduction to Digital Electronics) that teaches students traditional logic design principles based on discrete components (such as TTL and CMOS). The contents of this existing course will be updated to include topics in logic design using VHDL. In addition to exploration of traditional logic design principles, enhancements will allow students to learn a set of skills that covers VHDL as a new and industry-respected logic design tool. Students who choose to enter the job market after they earn their associate degree will be equipped with skills needed by employers.

<u>Introduction to Digital Electronics</u> – (4 Cr hrs, Class 3 hrs, Lab 2 hrs)

Course Objectives

The new revision of the course will not only teach traditional logic design principles based on discrete components (such as TTL and CMOS) but will also introduce students to the new concept of logic design using hardware description language such as VHDL. In addition to exploration of traditional logic design principles, enhancements will allow students to learn a set of skills that covers VHDL as a new and industry-respected logic design tool.

The academic objectives of the updated course are to provide students who choose to enter the job market after they earn their associate degree with skills needed by employers. Students will

learn principles of operation, performance, and design of digital circuits and digital instrumentation. The digital circuits will be introduced using fixed-function 7400 ICs and evolve into programmable logic devices programmed with VHDL. Coverage will begin with the basic logic gates used to perform arithmetic operations, Number systems, Boolean algebra, logic gates, combinational logic. Students will also learn how to model digital circuits in hardware description languages, how to use VHDL editors, debug designs and perform logic simulation, using Altera's Quartus® II development software. The course will integrate Altera's DE2 FPGA evaluation board and Altera's Quartus ® II development software. To accomplish this in a one-semester course, the intent of lectures and labs is to have the students:

1. Understand the basic logic gates and combinational logic functions, symbols, truth tables, timing diagrams, and logic circuits.
2. Simplify complex logic circuits by applying Boolean algebra laws and theorems and Karnaugh mapping.
3. Understand the operation of basic counters, decoders, multiplexers and arithmetic circuits.
4. Convert between the decimal, binary, and hexadecimal number systems.
5. Understand the basic types of flip-flop.
6. Understand sequential logic systems including synchronous and asynchronous operation.
7. Use modern computer tools for digital design and how to use VHDL to model basic logic gates.
8. Understand the characteristics of modern programmable logic devices and how to use Quartus® II development software.

The first class in the updated Introduction to Digital Electronics class was developed and conducted in spring 2012 with a total of seven enrolled students. Students were surveyed to evaluate the extent to which they felt they understood the top-level topics in the course. Responses were numerically weighted so 0% indicates no understanding and 100% indicates good understanding. In summary, of the 7 students who responded, 6 rated their understanding of the programmable logic design process and VHDL (2 separate questions) at 75% to 100%. On each question there was one "no opinion" (50%) response. The presentation of the material related to programmable logic and VHDL did not result in acceptable understanding of the topics among the students in the class. This was particularly true for the topic of VHDL. These findings are being used to adjust the course for the next implementation. As a result of continuous improvements, the following is a list of planned activities for the next class offering scheduled in spring 2013

- VHDL should be introduced more gradually throughout the semester rather than as a separate topic. For example:
  - introduce the assignment operator and basic Boolean operators when first presenting the topic of logic gates,
  - Introduce conditional assignment when first presenting multiplexers, etc.
- Programmable logic related lab exercises should focus first on the relatively intuitive schematic design entry method so familiarity with the FPGA development board can be developed. Once that familiarity is established, the VHDL design entry method can be introduced as a collection of the VHDL elements presented throughout the semester, which should improve the understanding of the topic.

IV. Faculty Workshop

An integral part of this project is to offer two 2-day workshops for up to 10 faculty members. The workshop is intended for interested electrical engineering technology program faculty. The goal of the workshop is to combine technical information from the vendor training with practical curriculum planning and strategies for developing courses like those developed at Michigan Tech University under this project. The workshop is to be advertised widely, primarily using Engineering Technology Division (ETD) listservs. The participating faculty members will spend approximately four hours learning introductory material on the impact of teaching engineering technology students relevant skills in hardware modeling and FPGA design. In subsequent sessions, the faculty will learn fundamental concepts of hardware description languages and gain knowledge on programmable logic devices (PLD) and their design methodologies. Participating faculty members will tour the Re-configurable Computing Lab and learn more about both the hardware and software necessary to establish a re-configurable lab at their respective institutions. Following the tour of facilities, participants will spend three hours in a hands-on lab experience to practice modeling basic building blocks of digital systems and learn the FPGA design flow starting from HDL design entry and circuit simulation to verifying the correctness of the design. During the second day, faculty participants will spend approximately four hours drafting potential curricular resources to be used at their respective institutions.

The second faculty workshop was offered at College of Lake County in December 2012, the project PIs conducted an intensive, two-day workshop on VHDL and FPGA design. Fifteen representatives from eleven institutions in five states (Indiana, Illinois, Wisconsin, Ohio, and Michigan) engaged in the hands-on learning experience, working with both the software and the hardware. The workshop provided faculty members of community colleges and four-year electrical engineering technology programs with the opportunity to expand their expertise in VHDL and FPGA design. The participants will utilize these skills to develop new courses in digital logic design, using VHDL and FPGA, at their respective institutions.

Assessment is a vital part of any curriculum reform project and helps provide useful information for workshop enhancements and determining if the workshop has met its objectives. Formative evaluation occurred during the workshop delivery and will be used to inform adjustments for subsequent workshop offerings. Embedded assessment is used to measure each workshop objective and determine whether goals are met. Assessment of the effectiveness of the faculty workshops training sessions offered is conducted anonymously using pre- and post-surveys. Assessment data collected and analyzed from the workshop will result in continuous improvement actions to be implemented in year two faculty workshop. We use a pre-test/post-test design and pre-survey/post-survey employing both direct and indirect measures of student learning. The indirect assessment instrument also included questions regarding participants' satisfaction while direct assessment instrument include a set small design problems and multiple choices problems.

Direct Measures of Student Learning:

Participants were given the same instrument for the pre-test and the post-test. The average score on the pre-test was 43% correct answers. On the post-test, following the instruction, the average score rose to 67% correct answers. It is clear that these participants made substantial progress towards mastering course concepts during the two-day workshop.

Indirect Measures of Student Learning:
Participants were also provided a pre-instruction and post-instruction instrument upon which they indicated their level of awareness/proficiency with various aspects of the course before and after the instruction. In addition, on the post-instruction instrument, a series of questions regarding the quality of instruction and student satisfaction were included. On items on a five step Like-type scale with 5 labeled as "Complete Mastery" and 1 labeled as "No Mastery" the following improvement was noted from pre-instruction to post-instruction instruments

Quality of Instruction (5= Strongly Agree, 4=Agree, 3=Neutral, 2=Disagree, 1=Strongly Disagree) **Measurable Outcomes**	**Post-Test Overall Rate**
The instruction was clearly presented	4.7
Any questions I asked were properly answered	4.9
The materials provided helped me to learn	4.9
The pace of the course was appropriate for the amount of material to be learned	4.4
All things taken into consideration, I considered the instruction to be excellent	4.9

Table 3: Quality of Instruction Participants' feedback assessment results

Measurable Outcomes (Average Scores)	**Pre-Test Overall Rate**	**Post-Test Overall Rate**	**Change**
Ability to implement basic constructs of VHDL	3	4	+1
Ability to implement modeling structures of VHDL	2.58	4	+1.42
Ability to use software tools to check the code for correctness and to correct errors	2.75	4.2	+1.45
Write synthesizable VHDL	3.33	4.2	+.87
Control state machine Implementation	3.25	4	+.75
Optimize a design using operator balancing	2.67	3.9	+1.23
Create a test bench and run a simulation	2.58	4.1	+1.53
Create a new Quartus II project	3.5	4.8	+1.3
Create design components using Megawizard	2.58	4.4	+1.82
Compile a design and view results	3.17	4.7	+1.53
Use settings and assignments to control results	2.75	4.8	+2.05
Make pin assignments and evaluate	3.17	4.7	+1.53
Use the TimeQuest timing analyzer	2.25	4.4	+2.15

Table 4: Participants' feedback assessment results

V. Undergraduate Research Opportunities:

The long-term objective of this project is to provide a learning opportunity at the School of Technology which will result in a research activities focused on FPGA and hardware design

modeling. Research experiences will provide more in-depth training for undergraduate senior students. In addition to involving Michigan Tech university undergraduates in research, undergraduate students from partner community colleges can be involved in research at Michigan Tech. Two Electrical Engineering Technology (EET) students from Michigan Tech were hired as summer interns (2011, 2012). They have been given the opportunity to develop more in-depth expertise in VHDL and FPGA design.

VI. Conclusion

With the demand of skilled FPGA designers on the rise, the objectives of this paper was to present the year project activities including curriculum development at both Michigan Technological University and College of Lake County, the second faculty workshop training opportunity for interested faculty members at similar institutions, and finally, the undergraduate research experience at Michigan Tech. The goals of this project are to give students of both two-year and four-year Electrical Engineering Technology a real-world experience on FPGA logic design and give them the necessary training with industry widely used design tools. Students of the electrical engineering technology two- and four-year programs will not only gain skills and knowledge that are highly marketable, but also will work with faculty advisors on applied research projects in hardware modeling and programmable logic design.

Bibliography

1. N. Alaraje and A. Sergeyev (2011). "Developing a digital logic design Curriculum in Electrical Engineering Technology - Bridging the Gap between Industry Needs and Academia", Ed. Philip D. Weinsier, Technology Interface International Journal.
2. N. Alaraje, A. Sergeyev and F. Scheu "Digital Logic Design: Meeting industry's needs through university & community college collaboration" 2011 ASEE Annual Conference & Exposition Proceedings, Vancouver, BC, Canada.
3. N. Alaraje and A. Sergeyev, "Collaborative Curriculum Development of an Industry-Driven Digital Logic Design" 2011 ASEE Annual Conference & Exposition Proceedings, Vancouver, BC, Canada.
4. http://www.altera.com
5. R. Furtner and N. Widmer, "Technology Education and the new frontier of digital electronics," ASEE Annual Conference & Exposition (ASEE 2006), June 2006
6. N. Alaraje and J. E. DeGroat, "Evolution of Re-Configurable Architectures to SoFPGA," IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005), August 2005.
7. B. Zeidman, " The future of programmable logic," Embedded System Design, Oct 2003.
8. H. Nie and R. Pecan, "The Innovative Effects of HDL and FPGA on Digital Hardware Design Education in EET Programs," ASEE Annual Conference & Exposition (ASEE 2007), June 2007
9. http://www.bls.gov/oco/home.htm.
10. http://www.abet.org

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