

HOT CARRIER STRESS EFFECT ON THE PERFORMANCE OF SECOND ORDER OVERSAMPLING CMOS DELTA-SIGMA MODULATOR

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Abstract

This work investigates the effects of hot carrier stress on the characteristic and performance of a second order oversampling delta-sigma modulator of an analog-to-digital converter as a function of stress time and temperature. The stress time is varied up to 4 hours and temperature up to 150°C. The modulator is designed in 0.5µm CMOS n-well process with hot carrier effect (HCE) modes. The performance degradation of a CMOS amplifier under HCE is also investigated in detail which is used in modulator design. SPICE is used for the post-layout simulations and HCE is observed through the MOSFET threshold voltage variation in the MOS modeling. The gain of the amplifier which is dependent on the transconductance and drain conductance of the differential pair changes during hot carrier stress. This causes noticeable degradation in the resolution of the modulator.

1. Introduction

CMOS data converters are the most important and integral part of many integrated electronic systems that are used in automotive, military, and space applications. These applications are often required to operate in harsh environments, where hot carrier effect becomes the primary reliability concern¹. The hot carrier effect also significantly influences the small geometry and scaled CMOS devices and, therefore, it becomes important to study the effect of hot carrier induced performance degradation in the CMOS data converters - analog-to-digital (A/D) and digital-to-analog (D/A) converters.

The hot carrier induced degradation of MOSFETs, especially in n-MOSFETs has been a topic of extensive research in recent years and many physical models and simulation results have been presented. In n-MOSFETs, hot carrier injection is caused by the high energetic charge carriers flowing in the channel of the transistor. These charge carriers gain energy from the electric field induced by the applied drain source voltage. When these hot carriers have a sufficient high energy, they may cause damage to the device as a result of trapping charge carriers in oxide traps or the formation of new oxide traps or interface states. Due to the increase in interface traps and oxide trapped charges, changes in threshold voltage and transconductance will occur.

Delta-sigma type analog-to-digital converters are widely used in wireless sensor networks and are integral part of many sensing devices. In this paper, we discuss the hot carrier effect (HCE) on the performance of a second order oversampling delta-sigma modulator. The empirical model for degradation due to HCE under the stress condition as presented in¹ is used in HCE modeling. The modulator is designed in 0.5 μ m CMOS n-well process with HCE modes. The gain of the amplifier and performance of the integrators which use the amplifier under hot carrier stress at different stress times and temperatures are investigated in detail.

The paper is organized as follows: Section 2 describes block diagram of the second order oversampling delta-sigma modulator and the amplifier used in the design. Section 3 discusses the parametric degradation during HCE in the modulator and the amplifier. Section 4 discusses the simulation results in detail.

2. Delta-Sigma Modulator Design

The block diagram of a second order oversampling delta-sigma modulator is shown in Figure 1 and it is the analog part of the delta-sigma A/D converter². It consists of two discrete time integrators and a 1-bit quantizer (A/D converter) in the forward path and a 1-bit D/A converter in the feedback path of a single feedback loop system. The number of integrators in the forward path determines the order of the modulator. The discrete time integrator is implemented using switched-capacitor parasitic insensitive technique and the need for a sample and hold circuit is removed. Also, switched capacitor system is less sensitive to clock jitter and the manner in which the operational amplifier settles. The switched capacitor integrator is implemented by using a switched capacitor circuits driven by a non-overlapping clock and an operational amplifier.

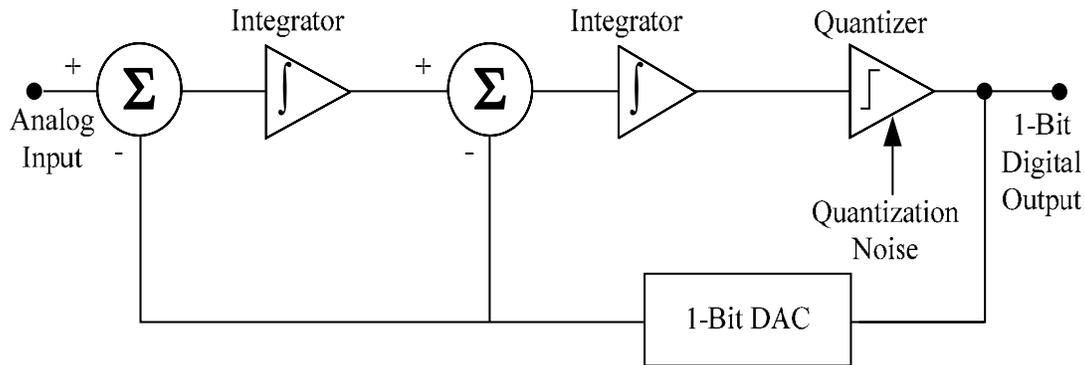


Figure 1: Block diagram of a second order delta-sigma modulator.

The operational amplifier is the core element of most analog and mixed signal systems. A two-stage CMOS amplifier topology has been used to provide good voltage gain, a good common-mode range, high bandwidth, very high input impedance, low output impedance and good output swing. The design consists of an input differential gain stage, differential to single-ended conversion stage and a second gain stage. Most of the critical parameters of the op-amp are decided by the input differential gain stage. The amplifier is made stable by using coupling

capacitances and nulling resistors. The operational amplifier is as shown in Figure 2^{3,4} and used in design of integrators and quantizer of the modulator shown in Figure 1.

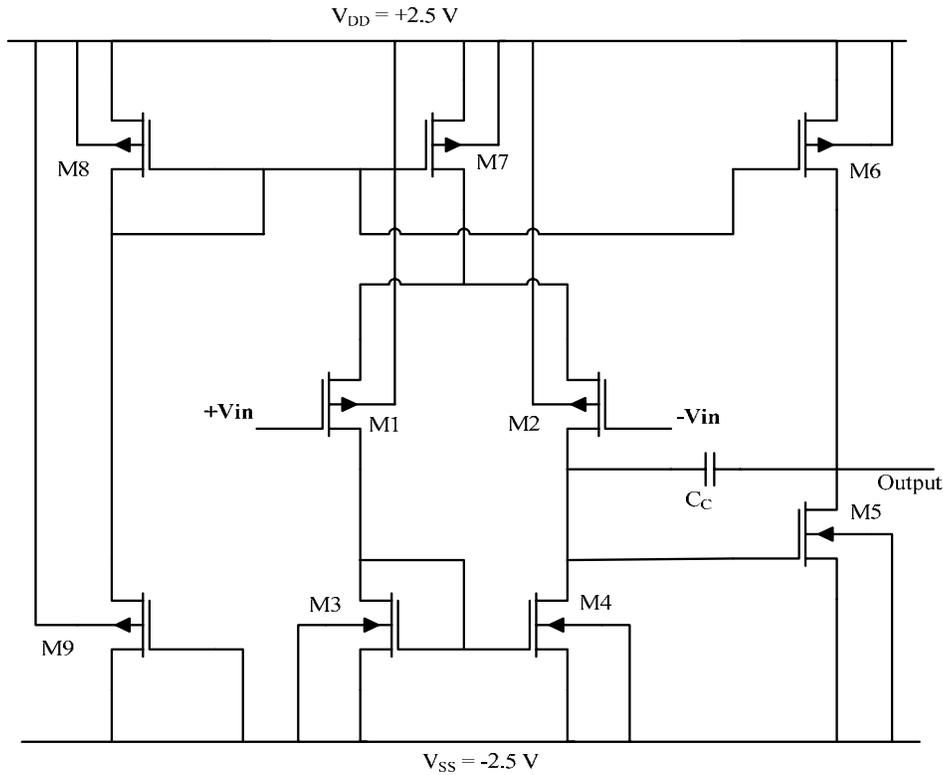


Figure 2: CMOS amplifier with p-MOSFET input differential pair.

3. Degradation during HCE

HCE tests are first performed and investigated under different stress conditions and temperatures of the MOSFETs. In this test, stress condition is created by using an external voltage on the gate and drain of the MOSFET. All the parametric changes are recorded during HCE testing and the degradation of the device parameters is observed. These recorded parametric changes are used to provide necessary information for performance analysis of the amplifier and modulator under hot carrier stress.

In the amplifier and delta-sigma modulator, HCE affects the device parameters including the increase of threshold voltage V_{th} and the decrease of electron and hole mobilities, μ_0 . The empirical hot carrier injection model considers change in threshold voltage (ΔV_{th}) and conductance ($\Delta G_m/G_{m0}$) of MOSFETs [1] which are expressed as follows:

$$\Delta V_{th} \text{ (or } \Delta G_m/G_{m0}) = At^n \quad (1)$$

In Eq. (1), A and n are the empirical parameters extracted separately from the MOSFET stress test and are technology dependent. The parameter n has a strong dependence on the gate to

source bias (V_{GS}) used during the stress mode of experiments but little dependence on the drain to source bias (V_{DS}). Similarly, the parameter A shows a strong dependence on the drain to source bias (V_{DS}) and has little dependence on the gate to source bias (V_{GS}). In our work, $V_{GS} = 5V$ and $V_{DS} = 5V$. In $0.5\mu m$ CMOS n-well process, with $0.5\mu m$ channel length and 14 nm thin gate oxide for the n-MOSFET, $n \approx 0.6$, $A \approx 0.4mV$, then $\Delta V_{th} \approx 125\text{ mV}$ for 4 hours stress time¹.

Using the above model, the shift in threshold voltage (ΔV_{th}) for varying hot carrier stress time is calculated and SPICE is used for simulation by adjusting the model parameter of threshold voltage to include the threshold voltage variation due to HCE. In amplifier, the parametric degradation of the gain is calculated from SPICE.

4. Simulation Results

Figure 3(a) and (b) show the chip layout and microphotograph of the second order delta-sigma modulator design of the block diagram shown in Figure 1. The chip is designed in $0.5\mu m$ CMOS n-well process.

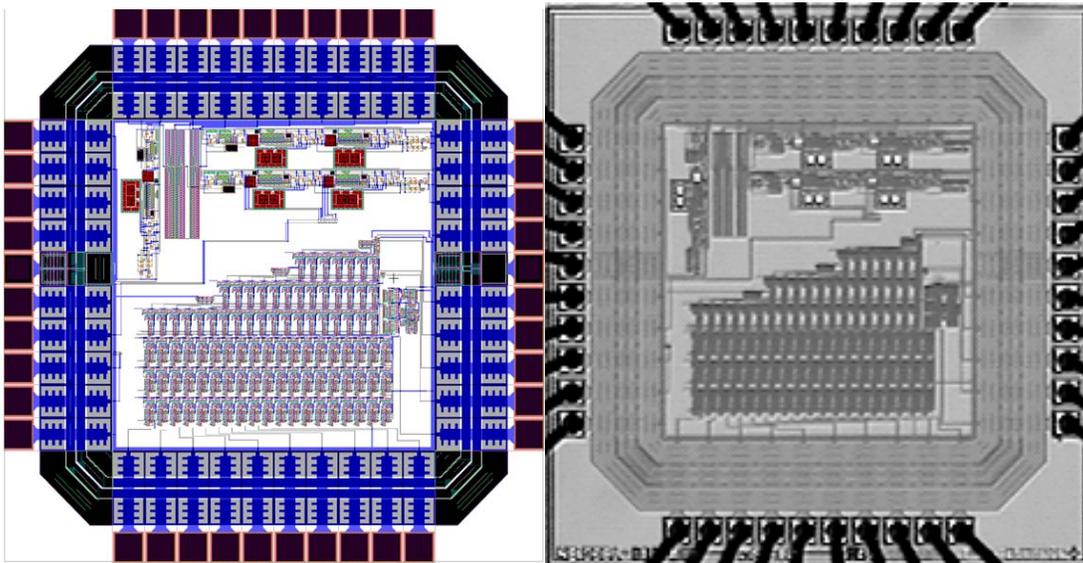


Figure 3: (a) Chip layout of the second order delta-sigma modulator and (b) microphotograph of the fabricated modulator chip.

Figure 4 shows the parametric degradation of the gain of the amplifier for different temperature and stress conditions. The gain of amplifier decreases with the increase of temperature and stress time. Further, due to the hot carrier induced interface trapping, the transconductance of the MOSFETs decreases¹. Drain conductance also decreases as the damage due to HCE is caused primarily by the interface states created close to the drain. Hence in the analog circuit operation, the degradation of drain conductance and transconductance causes the gain to decrease as shown in Figure 4⁵.

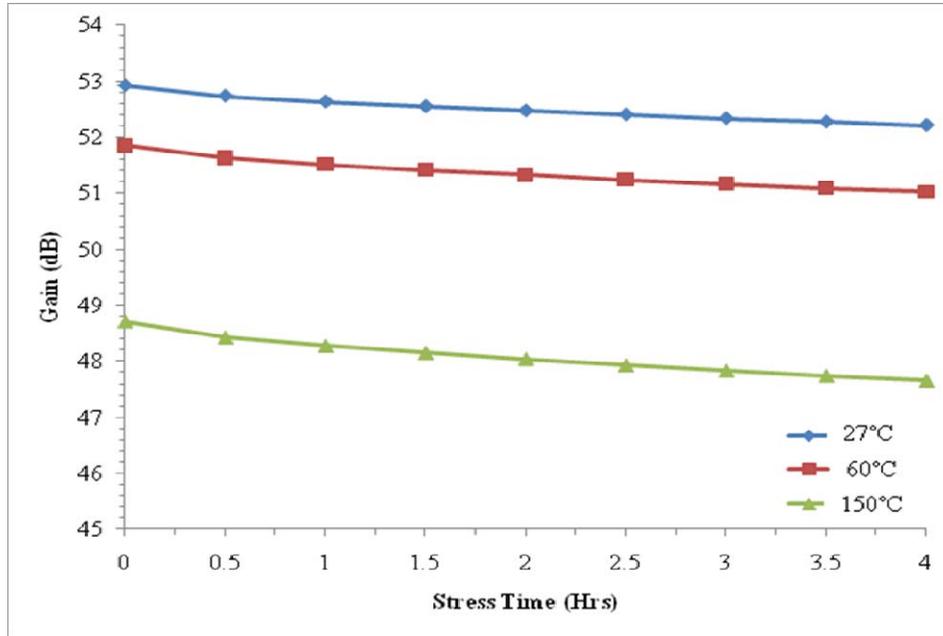


Figure 4: HCE degradation – gain versus stress time of the CMOS amplifier used in modulator chip design of Figure 3.

Since amplifier is an important block of the modulator design, its performance is expected to degrade with HCE which can be observed into the modulated output. Figure 5 shows the modulator output from SPICE at 27°C with no HCE. Hence in the second order delta-sigma modulator with an output resolution of 14-bits using a nominal supply voltage of 5V, the resolution is 0.3 mV which is set as the failure limit for the offset voltage⁵.

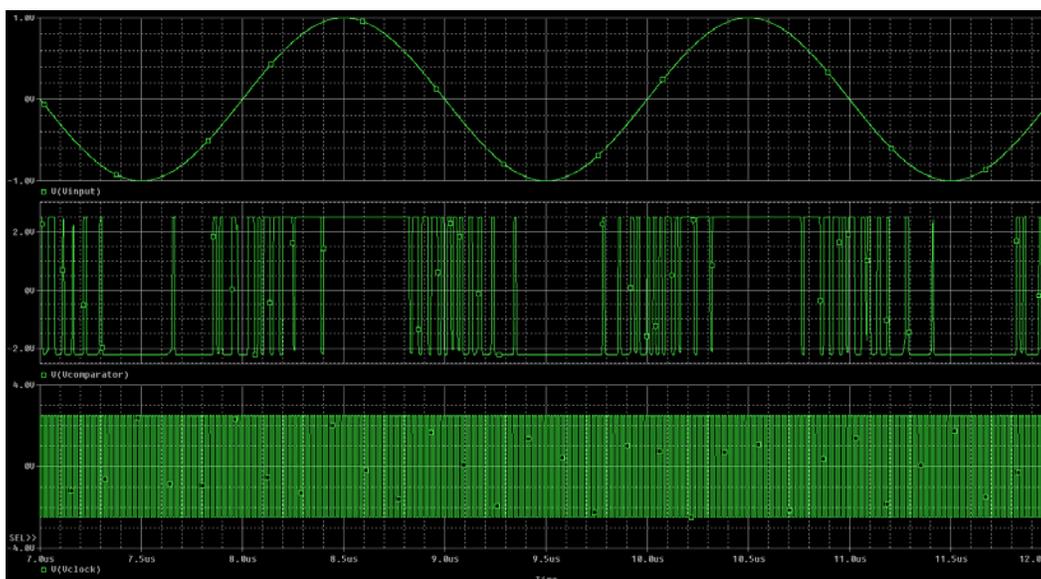


Figure 5: Simulated output from the second order delta-sigma modulator at room temperature (27°C).

Figures 6-8 show the pulse width modulated output of the modulator design of Figure 3 corresponding to 27°C, 60°C and 150°C for 4 hours of stress.

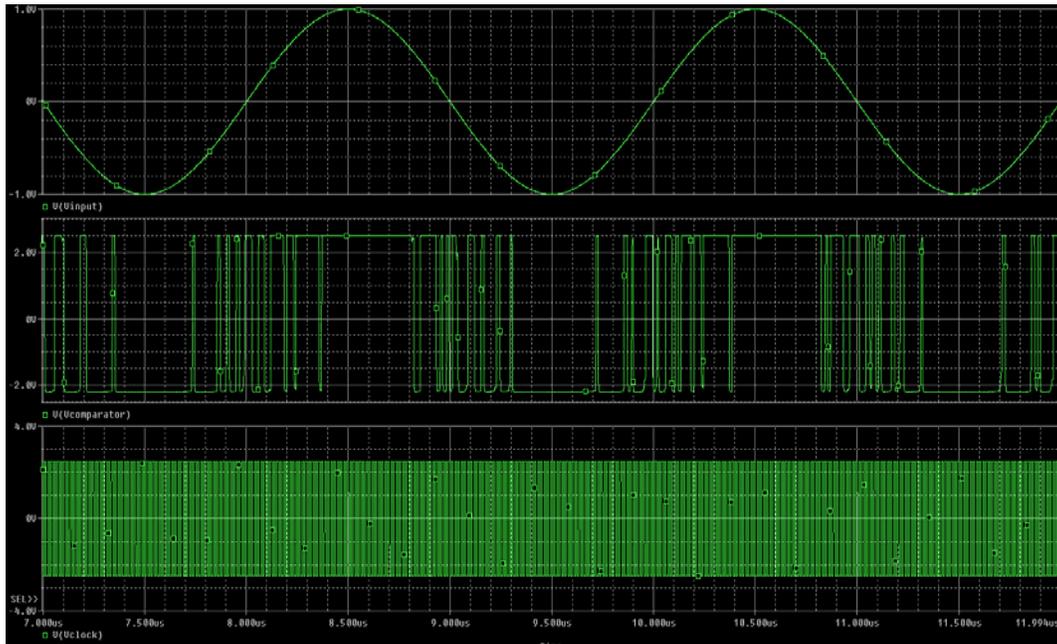


Figure 6: Simulated output from the second order delta-sigma modulator at room temperature (27°C) and 4 hours of stress.

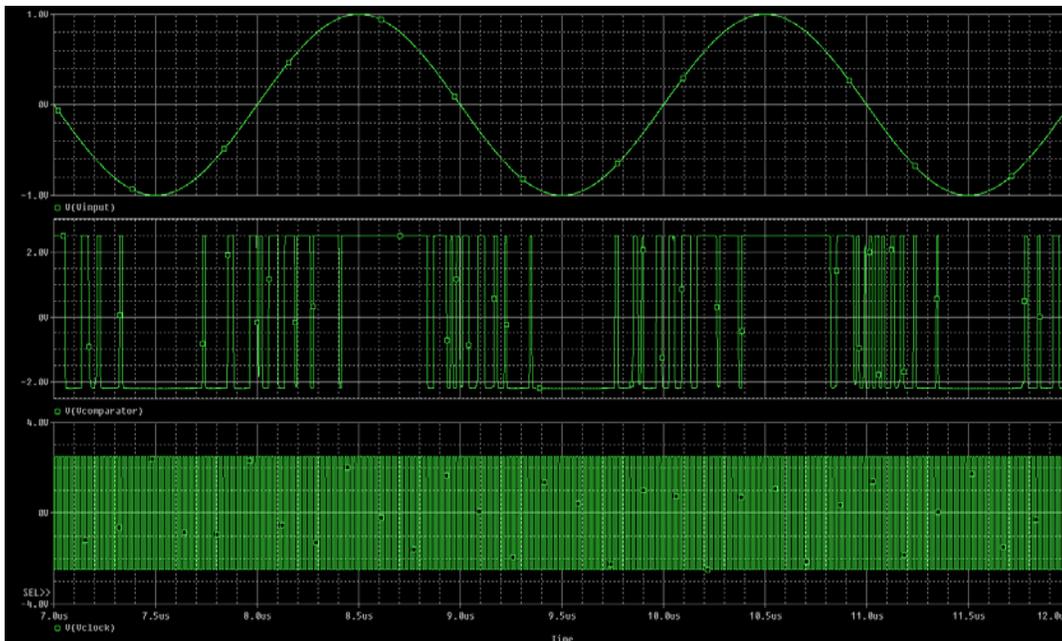


Figure 7: Simulated output from the second order delta-sigma modulator at 60°C and 4 hours of stress.

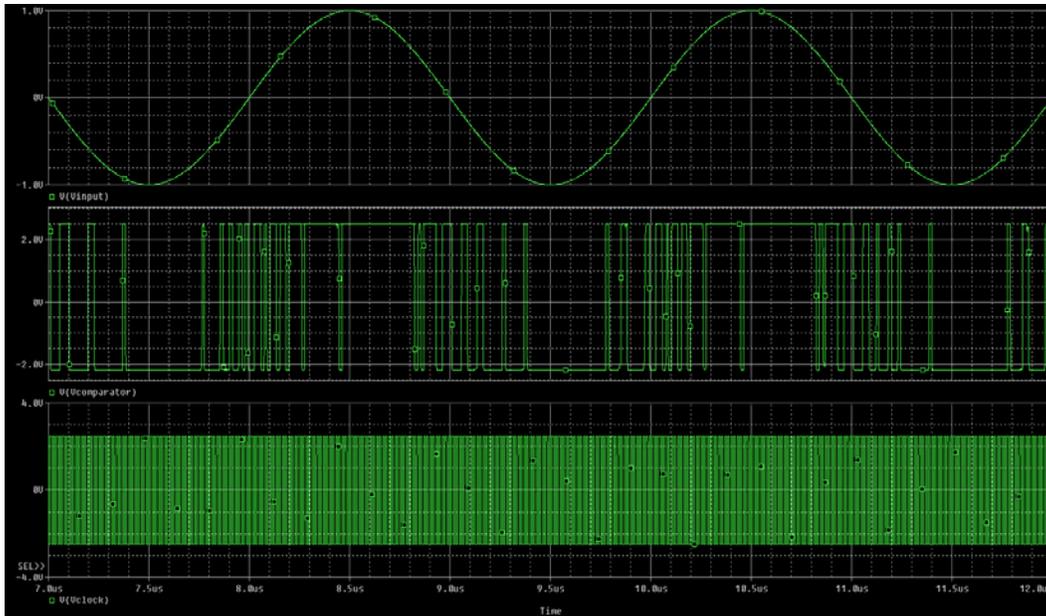


Figure 8: Simulated output from the second order delta-sigma modulator at 150°C and 4 hours of stress.

It can be easily observed from comparison of outputs of the modulator at different temperatures and same stress time that the pulse width output is significantly degraded in resolution at 150°C.

4. Conclusion

Hot carrier effects are investigated in amplifier and second order oversampled delta-sigma modulator, which are designed in 0.5 μm CMOS n-well process. Overall voltage gain of the amplifier decreases with the increase in stress time and degradation is more pronounced at higher temperatures. The degradation in the performance of the amplifier is reflected in the pulse width modulated output of the modulator and the effect is significant at higher temperatures which will have direct effect on the resolution of A/D converter.

References

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