

Implementation and Design of a Novel Student Developed Modular HTOL/HTRB System Using Thermoelectric Control

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Abstract

Addressing reliability issues is critical to the successful design and implementation of new semiconductor material systems proposed for next generation power electronic devices. For military systems, reliability is central to successful device designs, often outweighing other design factors. Several reliability testing schemes are central to validating power semiconductor device reliability. Of these, high temperature operating life (HTOL) and high temperature reverse bias (HTRB) testing are often used as go/no-go metrics for the success or failure of a fabricated lot of devices.

To educate students in the importance of these testing regimens for devices, several undergraduate and graduate students have developed a custom, modular thermoelectrically cooled and controlled HTOL/HTRB system which allows for joint long term HTOL/HTRB testing at both institutions. Under constraints for cost, the system was designed to utilize a novel thermoelectric cooling scheme to provide a temperature range of 55 °C from 5 °C to 62 °C with less than 0.5 °C variation under 15 W heat load from devices-under-test (DUTs). A hermetic DUT environment was designed using nitrogen purging and active humidity sensing to control relative humidity (RH) within the environment to beneath 5% RH. Undergraduate students gained experience designing for manufacturability and machining with CAD tools not typically explored in typical electrical engineering design projects. An automated switch-matrix was designed and implemented to automate testing and allow for programming of complex stress-measure-stress reliability testing profiles. Control and automation were enabled using common Mbed processors used throughout an undergraduate electrical engineering curriculum. To accomplish a unified design which could be installed at multiple locations, students investigated and implemented a server rack mounted design which uses commonly available banana and BNC connections for “plug-and-play” of the system. A control program was developed using a LabVIEW program which managed the system wide control and programming of different reliability testing regimens, such as stress-measure-stress, stepped-stress, and constant current, voltage, or power testing.

Results for the fabricated system performance are shown demonstrating the successful achievement of the design metrics. To demonstrate the use of the system, results from recent undergraduate student-led HTOL testing on novel GaN Schottky diode parts are presented. Current and future senior capstone and masters-level research projects using the novel system are reviewed.

Introduction

Semiconductor materials are critical to the operation and control of power electronic systems. For these systems, particularly in military applications, device reliability takes priority over other design considerations like efficiency or cost. Of course, these other considerations play a significant role in system design; however, reliability is foremost in design specifications for high power systems due to the dangerous nature of faults. It is often this consideration that incentivizes the use of thoroughly tested semiconductor materials. In order to encourage the adoption of new semiconductor materials into power electronic design, there is a need to mature the understanding of how these newer materials are affected by long-term use and exposure to adverse conditions. This not only increases general confidence in the ability of the devices to be implemented into hazardous systems, but also allows for failure analysis to be iterated on in future designs.

Educating students on the importance of reliability testing can be difficult due to the typical ways students are exposed to devices and systems in classrooms and laboratories. Students, especially at the undergraduate level, are often exposed to devices/systems just after learning about them. Laboratory exercises are often geared towards normal system performance and rarely contain fault analysis. When fault analysis is examined in a classroom environment, it is almost always in the context of a total device failure, rather than focusing on an intermittent fault or the progressive changes in a device's performance over time. This is also usually discussed in a purely theoretical sense and is rarely shown to students in a laboratory setting. The lack of this type of laboratory exercise from most student's undergraduate curriculum is reasonable considering the time limitations of most standard courses and the difficulty of producing labs of this kind. However, it does result in students having limited exposure to these topics and would reduce the efficacy of the instruction. [1]

The development of a measurement system was proposed to serve the double purpose of educating students on reliability testing and on the creation of a measurement system. The system proposed is intended to expose students to this critical field of engineering research, without requiring significant changes based on the type of device they would like to test. This makes it easier for students at the undergraduate and graduate levels to gather data on new semiconductor devices, allowing for the general understanding of these materials to mature at a higher rate. The fundamental objectives of engineering instructional laboratories met by the development of the system include: Instrumentation, Experiment, Data Analysis, Design, Learn from Failure, Creativity, and Teamwork. [2] Future laboratory use of the system would meet the following objectives: Instrumentation, Models, Experiment, Data Analysis, Psychomotor, Safety, Communication, and Ethics in the Laboratory. Undergraduate students involved in this project were required to have an interest in semiconductor device fabrication or testing and status as an Electrical Engineering student moving into their junior year.

System Requirements

The proposed system is intended to perform HTOL and HTRB tests on semiconductor devices. The tests apply high temperatures to solid-state devices while applying a stress voltage in order to observe and measure changes in their performance. These changes, in combination with statistical analysis tools, can be used to make assumptions and predictions about the devices.[3] The system was designed by a team of 2 undergraduate students and 3 graduate students to be modular and thermoelectrically cooled to allow for easy transport and assembly. This allows for identical tests to be performed at multiple locations with minimal assistance required to establish a new test environment. This type of system design facilitates long-term joint HTOL/HTRB testing at different laboratories.

The basic system design chosen implements a stress-measure-stress model for reliability testing and generating characteristic curves. Using a design which allows for the automated measurement of device characteristics at specified times during the test gives deeper insight into the physics of observed degradation in device characteristics. The devices are connected to a stressing circuit which applies either a constant or a stepped current for a preset stressing interval. Devices sharing a test box are held at a constant temperature for the duration of the stressing interval. Once the stressing interval has passed, the circuit automatically switches the devices onto a measurement circuit. The measurements are taken at a range of temperatures chosen by the user. At each measurement temperature, a staircase sweep voltage or current measurement is taken of the devices one at a time. This action is done successively for all devices connected to the system. Once the staircase sweep is performed, the system increments the temperature and repeats the measurement until the user's chosen upper threshold for temperature is reached. In addition, due to the possible testing of unpackaged devices, a requirement for a humidity-controlled environment for the device under test was imposed. The system was required to be assembled with low-cost parts in order to facilitate the construction of multiple test boxes under budgetary constraints. The combination of these system design requirements helped students explore all aspects of the engineering design cycle during the project.

Modular Test Unit Design Overview

To support modularity and ease of construction, the basic test unit for the HTOL/HTRB system was designed using a rack-mounted enclosure which integrated all necessary components besides the sources of electrical stress, device measurement instrumentation, system power, and a controlling computer. The Modular HTOL/HTRB test system was designed with joint long-term testing between institutions in mind and, therefore, a modular design was implemented to accommodate easy installation. The test boxes are cut to fit tightly into a standard server rack. This allows the user to install multiple boxes by stacking them on top of each other. Each test

box incorporates an integrated temperature and humidity controlled DUT chamber, microcontroller enabled temperature control circuitry, a 10 A 4x2 custom switch matrix which toggles devices between stress and measurement connections, and a line connected power supply to power all control circuitry within the unit. External connection ports were integrated into the faceplate of the box to connect to stressing sources and measurement instruments, as well as drying gases for humidity control. A picture of the completed unit is shown below in Figure 1. The left side of the picture in Figure 1 is the DUT box and an expanded view is shown below in Figure 3. The right side of the picture in Figure 1 is the Switch matrix and an expanded view is shown below in Figure 4. Further description of these subsystems is included next to those figures.



Fig. 1. Modular Test Box (Top-View)

In each test box, the internal components are controlled by two Mbed LPC1768 embedded microcontrollers. These devices are commonly used in electrical engineering undergraduate curriculums and operate on the C programming language, which is commonly taught to electrical engineering undergraduates. This makes their integration relatively easy and will make further improvements on their implementation possible for junior engineers working with the system. The two Mbed microcontrollers are designed as the Temperature Control Unit (TCU) and the General Control Unit (GCU) and will be referred to as such for the duration of this paper. The TCU is solely responsible for the control of the device temperature and relaying temperature information to the user. The GCU controls all other aspects of the box, including the humidity control system, LCD display, and switching circuit. Both devices can be connected to a PC via serial port, but the preferred method for the test circuit is by TCP/IP connection via

ethernet port. These microcontroller devices support the operation of the control loop shown in Figure 2.

DUT Temperature Control via Thermoelectric Cooling

A DUT temperature control method was developed for efficient and quick temperature movement to the various temperatures required during a testing cycle. This control method necessitated holding device temperature constant under large heat loads while simultaneously changing the device setpoint temperature within a time constant of less than 60 seconds. Based on cost constraints, a design using fluid cooling was ruled out. The cheapest alternative design, using resistive heating to heat the device above ambient temperature and air cooling was rejected due to the large time constants associated with cooling the DUT testing area. Students instead chose a design based upon a novel method using active thermoelectric cooling (TEC). TEC devices use the Peltier effect to move heat upon the application of an applied current. The direction of heat flow can be changed by changing the direction of the applied current. This effect is stronger when doped p and n type semiconductor materials are used for the TEC device. TEC devices can be utilized to control system temperature quickly and with high stability. [4-6] Typical uses of TECs are to maintain system temperatures under heat loads at a desired setpoint, such as in optical systems. However, the ability of TEC based systems to quickly change system temperature under low-heat load conditions allows for a stress-measure-stress system to incorporate accurate temperature variation during the testing phase without unduly increasing testing time.

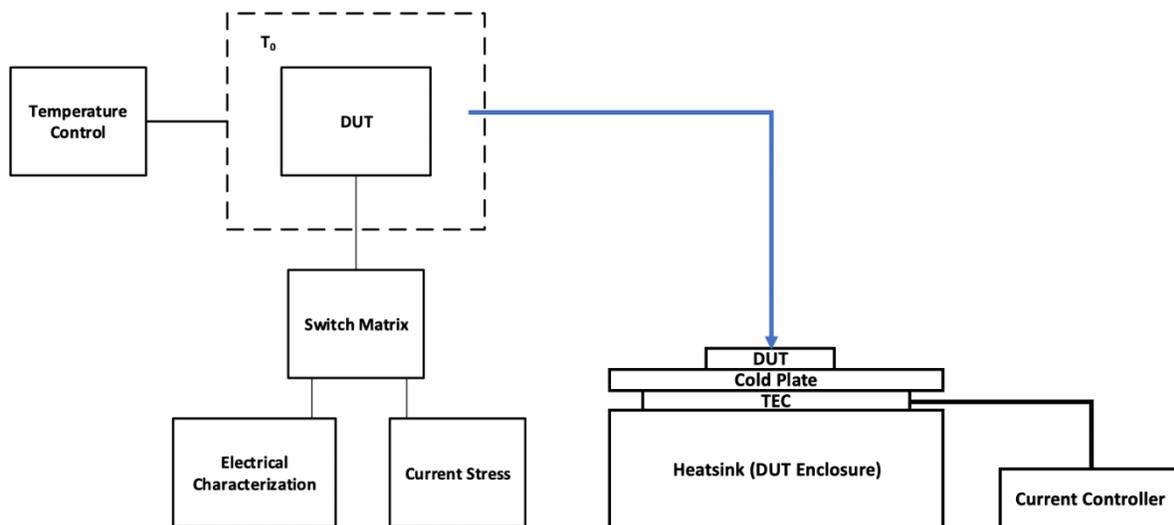


Fig. 2. TEC Device Enabled Stress-Measure-Stress System Diagram

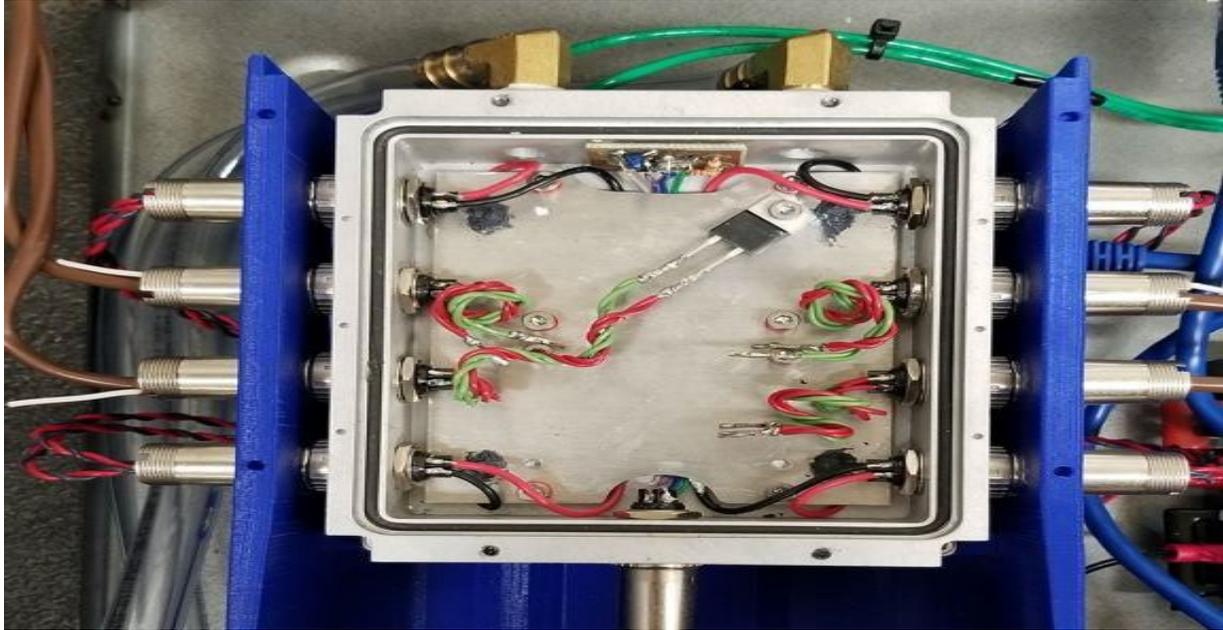


Fig. 3. DUT Box with external connections for electrical DUT connections, TEC, and humidity control

The TEC device is mounted inside of the device housing box beneath a cold-plate on which the DUT is mounted as shown in Figure 3. Based upon a requirement to control the temperature of devices under test generating 20 W of heat load during stress testing at a backplate temperature of 30 C, a design which incorporated four 15W TECs operating in parallel was chosen. These TEC devices are placed underneath the metal plate that the test devices rest on. Heat is rejected directly from the TEC devices to the DUT chamber, which is constructed of aluminum and serves as the heatsink for the TEC modules. The TCU circuit is mounted directly below the DUT chamber and connected to the TEC modules through side-mounted hermetically sealed connections on the chamber body. The TEC modules are driven via 4 MAX1978 TEC driver integrated circuits on the TCU board. Setpoint signals for these drivers are supplied via a multiplexed 4 output digital-to-analog converter (DAC) chip. The main microcontroller for the TCU, an Mbed LPC1768, is mounted on the board and communicates with the DAC via an I2C serial bus. An ethernet connection allows for communications with an external control computer.

The TCU implements a proportional-integral-derivative (PID) loop in order to adjust the current applied to the TEC modules and consequently control the plate temperature. To accomplish PID control, the TCU device was programmed by an undergraduate student using the Mbed real-time operating system (RTOS) multithreading toolkit. The lower-priority thread is the implementation of the PID loop in which it adjusts the current supplied to the TECs. The coefficients for the proportional, integral, and derivative term were determined empirically by testing the temperature convergence time using different coefficient values and comparing their performance. It was found that adjusting the coefficient values over different temperature ranges

achieved the best performance. A LabView program was designed to automate the process of changing these coefficients and testing them. The low-priority thread can be interrupted at any time by an input from the user. The user is able to change the setpoint values, request device temperatures, and toggle the system on/off via a set of commands sent from the TCP/IP connection or serial port.

During the initial construction and shakedown testing of the temperature control system, the students found that the maximum current provided by the system to the TECs could produce significantly high or low temperatures. Unfortunately, we were unable to measure the temperatures reached due to temperature sensitivity range limitations from the thermometers used. The input voltage sensing limits of the Mbed microcontroller and the temperature sensing circuit design restrict the sensitivity range of the system. Future redesign of the system will include ensuring the temperature sensing and TEC power supply circuits are sufficient for TEC modules in the 30W range.

Switch Matrix and GCU Design

In order to automate measurements and make stress-measure-stress testing possible, a switch matrix is needed to change DUT connections. External off-the-shelf options, such as the Keithley 700 series, were explored and rejected due to cost. A custom-built switch matrix was instead designed and fabricated. The switch matrix circuit was constructed using 8 double-pole, double-throw switches in a 4 input by 2/4 output configuration to connect each DUT within the DUT chamber to either a stress input with two terminals or a measurement input in a 4 terminal Kelvin configuration. To accommodate high current and high voltage testing, the chosen relays were designed for a maximum current capacity of 10 A and a maximum applied voltage of 240 V. When the stress input is connected, the third and fourth sense measurement connections are left disconnected by the circuit. In the normally-off position, the DUT devices are connected to the stress terminals. The coil currents for the switches were driven by MOS power transistors to enable compatibility with TTL signals from a control microcontroller. The completed switch matrix is shown in Figure 4.

Unlike the TCU, the control Mbed microcontroller for the switch matrix is not located on board the switch matrix circuit. Instead, the switch matrix control Mbed is located on a third circuit, called the GCU, which handles several other functions besides switch matrix control. An undergraduate student programmed the three main functions of the GCU, which are controlling the box humidity, status display, and controlling the switching circuit. An LCD display that shows pertinent information to the user at a glance is mounted on the GCU board. It cycles through information automatically and is meant to give updates for someone working on the box. This facilitates a design where the test box is remotely controlled by a PC in another location. A user working with the box will not be able to control the system using this display but will know

if a test is in progress and what the status of the system is without needing the controlling computer nearby.

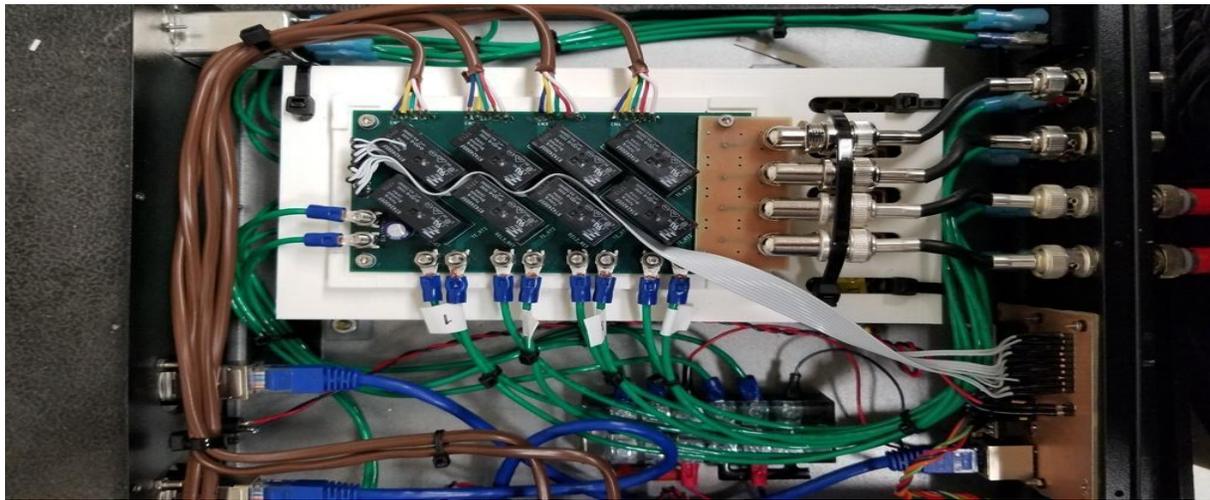


Fig. 4. Switch matrix and GCU circuits

Humidity Control

A hermetic DUT environment was achieved by using a Honeywell relative humidity (RH) sensing circuit integrated in the DUT chamber. This circuit communicates with the GCU via a serial connection to monitor the RH circuit within the DUT enclosure. When the humidity rises above an upper threshold, the GCU sends a turn-on signal to an external circuit which toggles on a solenoid valve, allowing pressurized nitrogen or dry air to flow into the device housing box until the humidity falls below a lower threshold value. After this lower threshold humidity is achieved, the trigger signal from the GCU is removed, shutting the valve until it is needed again. Using dry-nitrogen, the system is designed to achieve less than 5% RH at DUT enclosure environmental temperatures of 25 C. The signal sent to the valve is a simple binary signal. When multiple modular test units are in use, the nitrogen line is connected in series between each unit. The signal from each box is fed into a logical OR gate, which purges all units in use whenever a unit rises above the acceptable humidity threshold. The system in its existing design can achieve a relative humidity as low as five percent.

Full Test System Implementation

The full integrated test system was implemented via construction on a standard 10 ft server rack. The test system is connected via an ethernet switch with each Mbed microcontroller, power supply, scope, and PC having its own unique IP Address. Using ethernet communications to each instrument makes it easy to communicate with individual test boxes despite not knowing how many the user will have connected. The amplifier/solenoid circuit for the humidity control system is placed on a separate rung on the server rack and is attached to a freestanding canister

of gas. Placed above the test boxes are the power supplies needed to implement the stressing of the devices. The number of power supplies needed depends on the number of output ports per supply. The existing implementation of the design requires two power supplies per box. These power supplies are also assigned IP addresses and connected to the switchboard. The bottom of the server rack is used to mount the measurement instrumentation. In one version of the system, an HP4142 modular source-measurement mainframe was used to conduct initial tests. In another version, a Keysight B1505A Power Device Analyzer/Curve Tracer is used for the measurements. Finally, uninterruptible power supplies with expanded battery capacities were used to protect against momentary blackouts. Three test unit modules operating in a single server rack is shown in Figure 5.



Fig 5. Three test unit modules connected for testing

For the existing system, Siglent 30V/3.2A power supplies are used as the stress sources, and connected to the switch via ethernet cable. The system is designed to work with simple banana and BNC connections to allow for easy installation. The PC is connected to the measurement instrumentation via a GPIB cable and to the ethernet switch via ethernet cable. The PC must be set to have a static IP with the same Gateway Mask as the rest of the test network. A schematic of the server rack testing setup is shown in Figure 6.

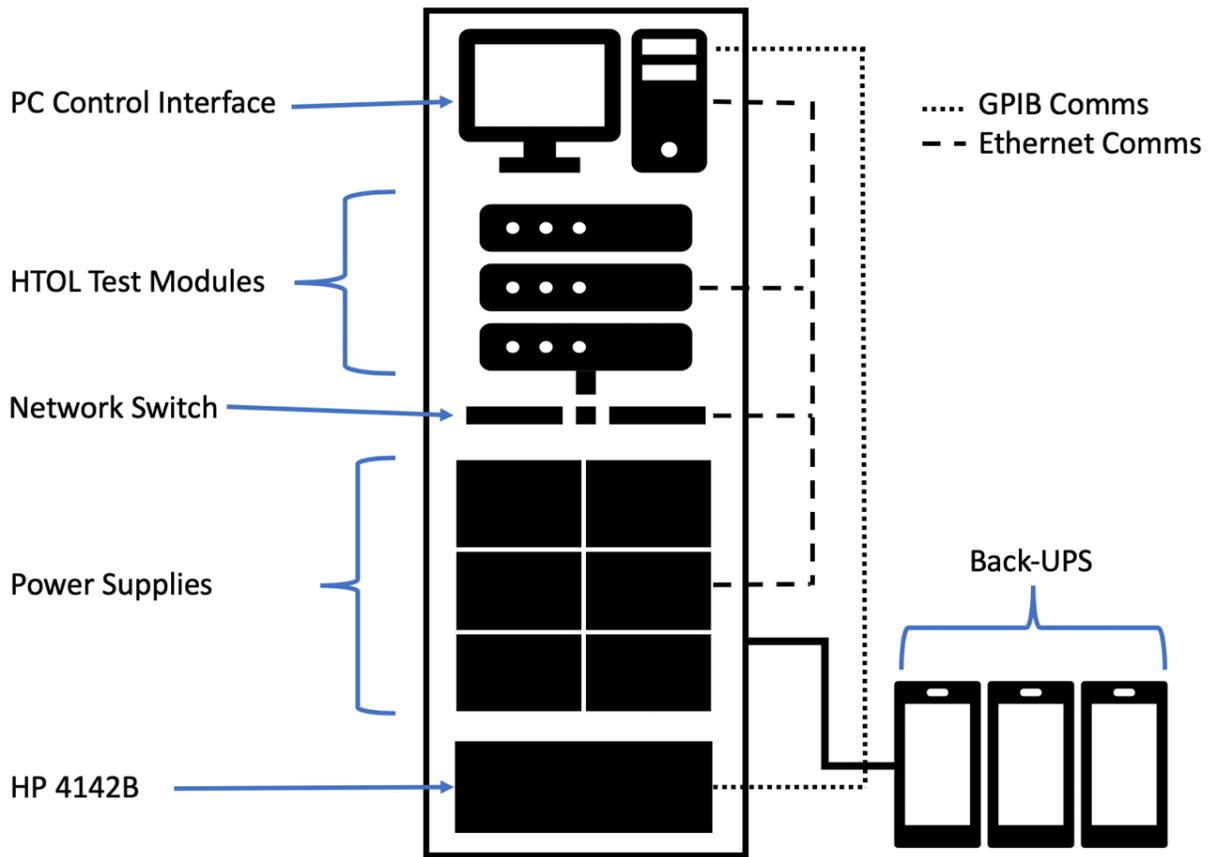


Fig. 6. Server Rack Modular Design

Test Control Program Design and Implementation

The control of the stress testing, timing and data collection are carried out via a central control PC. A custom control program was written by a graduate student to carry out the stress-measure-stress testing in LabView. This program was designed to maximize portability and minimizes the amount of editing the user would need to do after setting up their test rig. This makes it much more effective as a tool for undergraduate students to use and makes the setup easy to pass from person to person and between institutions. The system supports the modular design by adapting to the number of devices and boxes the user designates it to respond to. The user does not need to use all the available boxes or pad space for the program to work properly. The LabView Program remains on the PC screen as shown in Figure 7 and will update with temperature, voltage, and humidity measurements in real-time.

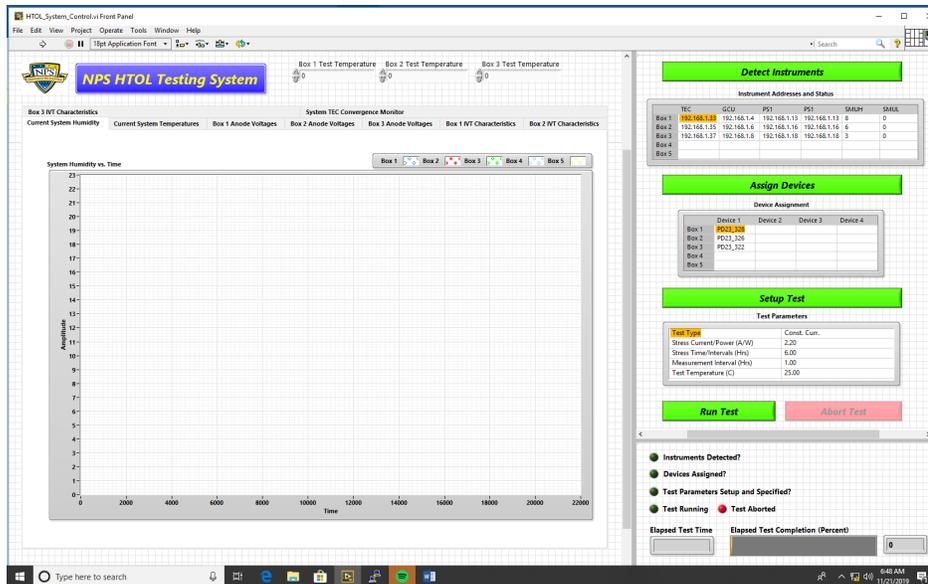


Fig. 7. LabView control program front panel user interface

The LabView control program was designed to give the end-user several options for programming a stress-measure-stress test. Either current or voltage stress can be specified. Measurement over an arbitrary number of temperatures during the measurement period can be specified. Both reverse and forward current-voltage measurements can be acquired. Constant or step-stress in time can be requested. Measurement intervals are programmable and can be as small as a few minutes. The program user interface (UI) automatically adapts to the number of units connected, based upon detected IP addresses, allowing for up to a maximum of 6 test units and 24 DUTs to be connected to a system configuration at a time. Data logging is saved locally for each DUT to a user-specified file. To ensure data integrity during testing in the case of the test being affected midway, data is saved continuously to ensure that testing can be resumed and that test data is not lost if the system has an error. Future implementations will use cloud storage to further ensure the safety of test data.

System Performance and Preliminary Test Results

Initial subcomponent testing by an undergraduate student focused upon stability of the DUT temperature over an extended time period and the responsiveness of the system to a change in temperature setpoint. Tests were carried out examining the effect of a 40-degree setpoint change from 10 °C to 55 °C. A settling time of 40 seconds was achieved for this setpoint change as shown in Figure 8. A similar result of 41 seconds was achieved for a cooling setpoint change from 55 °C to 10 °C.

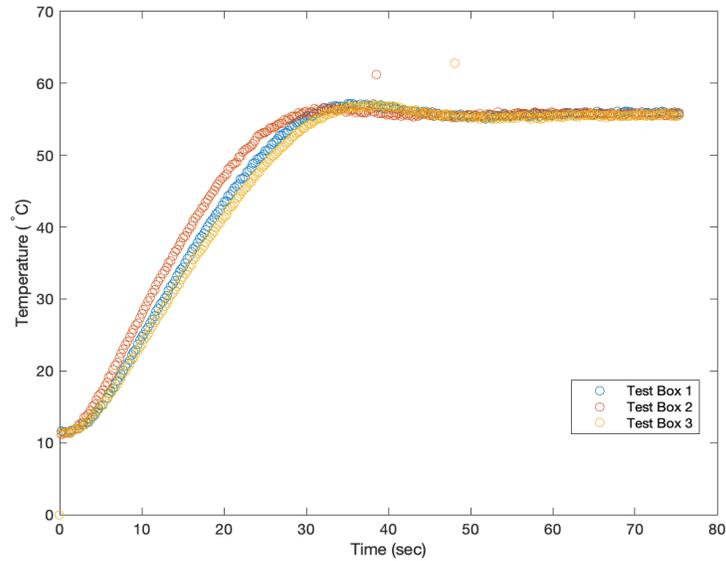


Fig. 8. Step response of DUT temperature in response to a 40 °C setpoint change

Stability of the DUT temperature system was investigated under 15W heat load from a test diode. A diode was biased by the stress source at 5V and 3A continuously in the DUT chamber of 3 test units for a period of 6 hours. The three units were kept at setpoints of 30 °C, 40 °C, and 50 °C. For the unit at the 50 °C setpoint, the unit remained within 1 °C of the target setpoint. The units at 30 °C and 40 °C were kept within 0.5 °C over the test period, which was below the noise floor of the thermistor temperature sensor. No noticeable drift in the temperature setpoint was observed as shown in Figure 9.

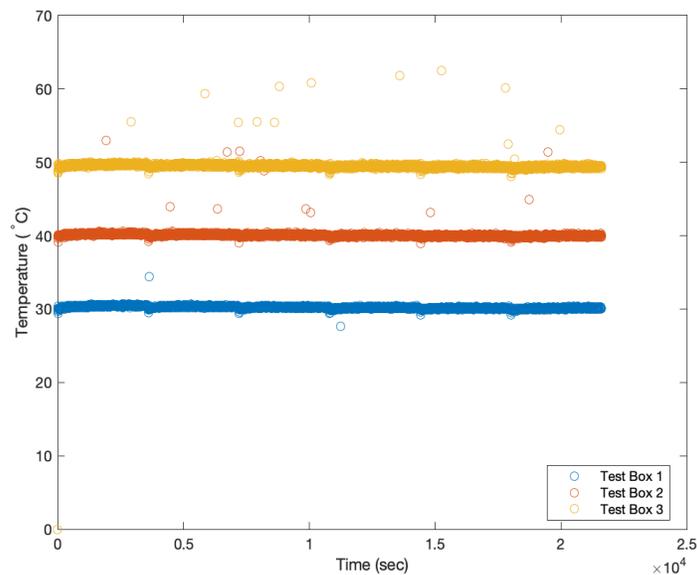


Fig. 9. Temperature variation over a 6-hour period of DUT box temperature with 15 W heat load

The first system tests involved HTOL-type testing of GaN Schottky diodes with Pd Schottky metallization in support of graduate thesis work. These devices were designed solely to test the Schottky metallization contact and were not optimized for reverse bias. Pd metallization was deposited via e-beam deposition upon a 8 um GaN epilayer grown on a bulk GaN n-type substrate. Devices were fabricated with 0.0025 cm² contact area. Step stress current testing was performed on devices in a range where device self-heating was important to examine the effect of high current density stress on the Schottky barrier height. In order to extract this parameter, the fast temperature setpoint capability of the system was essential. Current-voltage-temperature measurements (IVT) were carried out at 1-hour intervals over a step stress measurement which stepped up stress current from 1.7 A to 2.3 A over a 7-hour period. The IVT data was analyzed via the Richardson activation energy method to extract the barrier height, which was then plotted on a time basis.[7] Significant barrier height lowering is observed for devices subjected to stress currents above 1.9 A as shown in Figure 10. It is suspected that self-heating at these current levels is driving a metal-semiconductor diffusion process at the contact interface. Work is being performed to carry out similar tests at varying device temperature to determine the activation energy of this process.

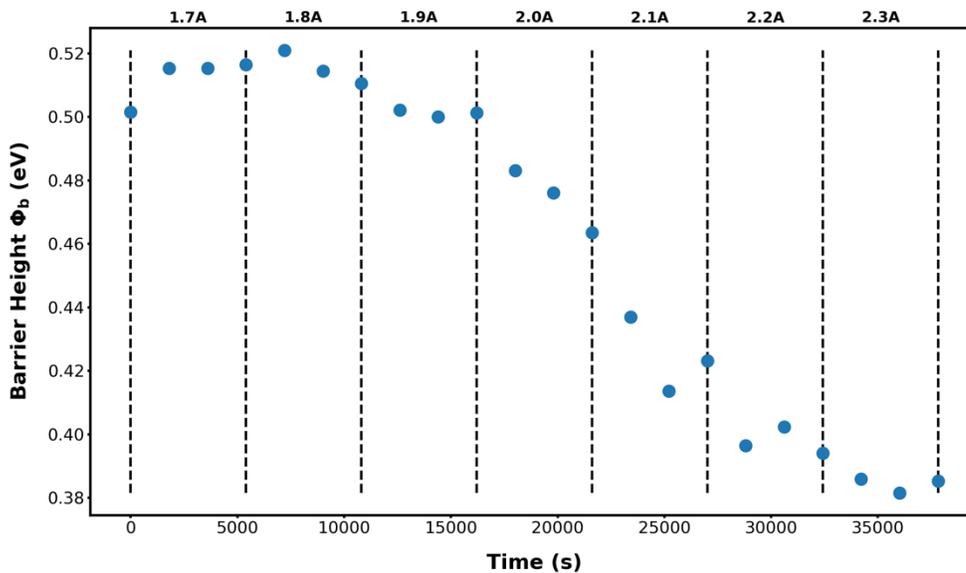


Fig. 10. Barrier height variation of a commercial GaN Schottky diode under current step stress versus time.

In parallel with this graduate level work, initial tests of the novel system were performed at the undergraduate level. The undergraduate work focused on establishing sample datasets using SiC devices to educate the students on the use of the system and the collection/analysis of measurement data. These characteristic curves were compared with data provided by device

manufacturers to verify the efficacy of the novel system. Present testing of GaN PN devices involves IVT measurements taken at 2-hour intervals with constant stress current at 2 A over 48-hour periods. Subsequent tests will be conducted with similar parameters while altering device stressing temperature or stressing current magnitude. In addition, undergraduate research will soon be performing IVT tests on novel designed GaN Schottky diodes. These tests will be conducted in a manner similar to the previous GaN Schottky device tests, and analyzed via the Richardson activation energy method.

A single undergraduate student was able to install this novel test system at the undergraduate institution with limited assistance from professors connecting a more complex measurement scope. Installation at a new location required no changes to the LabView control program with the exception of a small addition to accommodate the module selector required by the measurement scope. In addition to installing the system, the undergraduate student programmed the entire PID temperature control and humidity control systems in the test setup. In order to develop the skills needed to work on the novel test system the student had to become familiar with C programming practices, the MBed operating system and API, control theory, and many other advanced topics. Future iterations on the design will require more students to work on the MBed programs and hardware involved, demonstrating the systems viability as a multidisciplinary teaching tool.

Conclusion and Future Work

The importance of lifetime reliability testing to the adoption of new semiconductor materials cannot be understated as emerging power electronics demand a high degree of safety in operation. In order to facilitate the adoption of new semiconductor materials, it is necessary to mature the understanding of these materials through rigorous stress testing and failure analysis. By streamlining the design of these types of tests, we can encourage engineers at all levels to produce more research into these devices with minimal time commitment on their part. This not only allows junior engineers to contribute to emerging technologies but also gives educators a way to involve students in laboratory exercises while still operating within the constraints of the COVID-19 environment. This system will continue to be used at both the undergraduate and graduate institutions by one to two students at each site for continued reliability testing of Schottky contacts for vertical GaN devices.

The adaptable and modular design of the HTOL/HTRB test system presented in this work makes it ideal for adoption by other educational institutions as a relatively cheap and efficient way to measure device performance without committing a great deal of resources. The design of the system also lends itself to being iterated on with improvements in the separate sections. The modular design allows for sections to be replaced or changed without the rest of the system being affected, making reliability testing across multiple institutions for teaching and research purposes

easy to accomplish. One idea for expansion is to add capacitance-voltage measurement capability by purchasing an additional source measurement unit for the measurement system. There is also interest in redesigning the switch matrix to allow multiple SMU's to drive the DUT and enable 3 terminal device testing. This could most likely be accomplished with minimal alterations to the current test system and only minor updates to the control program. All of these possibilities will be explored by graduate and undergraduate students in the coming years.

References

- [1] S. Freeman, S. L. Eddy, M. McDonough, M. K. Smith, N. Okoroafor, H. Jordt, and M. P. Wenderoth, "Active learning increases student performance in science, engineering, and mathematics," *Proceedings of the National Academy of Sciences, National Academy of Sciences*, 2014, *111*, 8410-8415, doi: 10.1073/pnas.1319030111.
- [2] L.D. Feisel and A.J. Rosa, "The Role of the Laboratory in Undergraduate Engineering Education," *Journal of Engineering Education*, 2005, *94*, pp. 121-130, doi: 10.1002/j.2168-9830.2005.tb00833.x.
- [3] B. Peng, Ing-Yi Chen, Sy-Yen Kuo and C. Bolger, "IC HTOL test stress condition optimization," *19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2004. DFT 2004. Proceedings.*, Cannes, France, 2004, pp. 272-279, doi: 10.1109/DFTVS.2004.1347849.
- [4] S. Li, C. Hsu, C. Liu, M. Dai, H. Chien and R. Tain, "Hot spot cooling in 3DIC package utilizing embedded thermoelectric cooler combined with silicon interposer," *2011 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, Taipei, Taiwan, 2011, pp. 470-473, doi: 10.1109/IMPACT.2011.6117280.
- [5] G. J. Snyder, M. Soto, R. Alley, D. Koester and B. Conner, "Hot spot cooling using embedded thermoelectric coolers," *Twenty-Second Annual IEEE Semiconductor Thermal Measurement And Management Symposium*, Dallas, TX, USA, 2006, pp. 135-143, doi: 10.1109/STHERM.2006.1625219.
- [6] S. Zhang, "Thermoelectric Cooler Based Temperature Controlled Environment Chamber Design for Application in Optical Systems", Dept. Elec. Eng., Virginia Tech, Blacksburg, VA, USA, 2013.
- [7] D. Schroeder, *Semiconductor Materials and Device Characterization*, NJ, USA: Wiley Press, 2006.