AC 2010-943: IMPROVING COLLABORATIVE PROJECT-BASED LEARNING IN DIGITAL ENGINEERING BASED ON PROGRAM ASSESSMENT

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Improving Collaborative Project-based Learning in Digital Engineering Based on Program Assessment

Abstract

This paper presents the assessment results and findings of the National Science Foundation (NSF) sponsored CCLI project, entitled "Collaborative Project-based Learning to Enhance Freshman Design Experience in Digital Engineering." During the first year of the project, a series of interactive in-class projects using a Tablet PC based platform have been developed and implemented in our Introduction to Digital Engineering classes taught in Fall 2008, Winter 2009, and Spring 2009. So far over 100 students were impacted by our proposed Collaborative Project-Based Learning (CPBL) model. To quantify the effect of the course redesign on student learning, comprehensive evaluation using both direct and indirect assessment instruments was conducted. The assessment efforts were led by an expert from the College of Education, and the evaluation was based on class observation, comparison study of student performance, pre and post student surveys, as well as focus groups. While both quantitative and qualitative assessment results will be presented and analyzed, the focus of the paper will be the lessons learned through the first year experience from both the student and faculty perspectives. Overall, the students' feedback on CPBL has been very positive. Most students considered the in-class projects the most valuable and helpful parts in their learning. Through the in-class projects, they not only gained better understanding of the course material and the design process, but also developed stronger interest in engineering careers. Nevertheless, the assessment findings also indicated a few challenges to be addressed. In this paper, we will describe how to continuously improve the implementation of CPBL, how to adjust the teaching strategy and plans to revise in-class projects to be implemented in academic year 2009-2010.

Introduction

In 2008, California State University, Los Angeles (CSULA) received an NSF CCLI grant to redesign "Introduction to Digital Engineering" course (EE244). The core of the course redesign is to incorporate Collaborative Project-Based Learning (CPBL) to enhance student learning outcomes and reinforce their understanding of design principles learned in their freshman design course [1-3]. During the first year of the project, a series of interactive in-class projects using a Tablet PC based platform have been developed and implemented in EE244 classes taught in Fall 2008, Winter 2009, and Spring 2009. More than 100 students have been impacted by this innovative teaching pedagogy. Through the project, we are seeking a sustainable solution to stimulate students' interest in engineering, to increase the retention rate, and to foster students' engineering design knowledge and skills starting from the freshman year.

Project-based Learning (PBL) pedagogy has attracted the attention of many educators in engineering fields [4]. In recent years, PBL has been incorporated into a variety of courses and curriculums (from freshman-level to upper division specialization courses) in different engineering disciplines [4-11]. Compared to the traditional lecture-based instruction, PBL provides a more student-centered learning environment. Pilot studies have shown that although PBL may not necessarily lead to higher grades, it helps to motivate students in the learning process and improve students' hands-on design skills which are critical in engineering training

[11,12]. It is also well recognized that the effectiveness of PBL highly depends on the implementation. Hence, frequent and comprehensive assessment is essential to a successful course redesign that utilizes PBL.

To quantify the effect of CPBL on student learning in our CCLI project, comprehensive evaluation using both direct and indirect assessment instruments were conducted. While both quantitative and qualitative assessment results will be presented and analyzed, the focus of the paper will be the lessons learned through the first year experience from both the student and faculty perspectives. Specifically, the assessment findings revealed the following challenges when applying CPBL to the freshman level digital engineering class with a highly diverse student population:

- How to adjust the implementation of CPBL to address the needs of students with very diverse backgrounds?
- How to balance between direct instruction and in-class projects to achieve the best teaching objectives and learning outcomes?

In this paper, we will present how to continuously improve the implementation of CPBL, how to adjust the teaching strategy to address the above challenges, and how to restructure the in-class projects to make our practice sustainable in an educational environment with limited resource (no TA support, etc.).

Project Assessment and Data Analysis

The objectives of our CCLI project are threefold: 1) To foster the students' design skills at the freshman level; 2) To stimulate the students' interest in engineering design and to increase the students' retention rate; 3) To increase the teaching and learning efficiency in a freshman engineering course by highly interactive instruction using Tablet PCs. The project evaluation involves both formative evaluation which provides feedback during each implementation cycle of CPLB model, and summative evaluation which measures to what extent the project achieves these goals.

Table 1 lists the major assessments instruments used in our project evaluation. Quantitative student opinions are collected in the format of pre /post survey and satisfaction survey. Pre and post surveys were designed to quantify the impact of CPBL on student knowledge and skill development, while the satisfaction survey was designed to solicit students' feedback on the teaching pedagogy and its effect on their learning experience. In addition to quantitative data, qualitative data were also collected through focus group discussions and faculty class observations. Focus groups were hosted at the end of each quarter by our external evaluator to foster open-ended discussion among students. It is a very effective approach to collect student feedback for formative assessment, and also proved useful in evaluating project outcomes that are rather difficult to assess using quantitative approaches (e.g. the impact of CPBL on students' interest in engineering fields). Class observations were made by faculty whenever there was an in-class project. It is a direct measurement of student learning progress, and can provide a quick feedback on how well the students understand the design concepts and how fast the students develop hands-on skills. All assessment results are discussed periodically in PI meetings, and continuous improvements are made accordingly to ensure a successful implementation of CPBL. In the following subsections, we will share some representative assessment data with our

colleagues in the engineering education community and then present our findings through the analysis of the assessment results.

Table 1. List of major assessment instrument.

Assessment Instrument	Type of Data	Frequency
Pre and post surveys (conducted at the begin and the end of the quarter)	Quantitative data with qualitative explanation	Once per quarter
Student satisfaction survey	Quantitative data	Once per quarter
Focus Group led by external evaluator	Qualitative data	Once per quarter
Class observation	Qualitative data	On-going

1) Quantitative Assessment Results

The advantage of quantitative analysis is to provide objective evaluation of expected outcomes using numeric metrics. Tables 2 and 3 compare the pre and post survey results conducted in Fall 2008, Spring 2009, and Fall 2009 (A subset of these results was presented in our previous paper [3]). As a widely used approach to assess the learning outcomes, pre and post surveys allow the students to rank their own knowledge and skills prior to and after the learning (1- "None", 2- "poor", 3- "Fair", 4- "Good", 5-"Excellent"). The data sample sizes in Fall 2008, Spring 2009 and Fall 2009 are 28, 22, and 15[1] respectively.

Table 2. Impact of CPBL on student knowledge growth (pre and post survey analysis).

Learning outcomes (Knowledge)	*Fall, 2008*			*Spring, 2009*			*Fall 2009*		
	Pre	*Post*	*diff*	*Pre*	*Post*	*diff*	*Pre*	*Post*	*diff*
1.Knowledge of engineering design process	2.11	3.27	1.60	2.34	3.52	1.18	3.00	3.42	0.42
2.Knowledge of computer simulation	2.39	3.27	0.88	1.56	3.23	1.67	2.6	3.25	0.65
3.Knowledge of design verification and testing	1.96	3.8	1.84	1.74	3.36	1.62	2.6	3.50	0.9
4.Knowledge of binary number system	2.86	4.18	1.32	2.35	4.00	1.65	3.6	4.58	0.98
5.Knowledge of binary calculation	2.46	4.09	1.63	2.29	3.95	1.66	3.53	4.42	0.89
6.Knowledge of logic functions	2.75	3.91	1.16	2.11	3.76	1.65	3.33	4.25	0.92
7.Knowledge of Karnaugh-maps (K-maps)	1.59	4.09	2.50	1.54	4.14	2.60	2.0	4.33	2.33
8.Knowledge of adder, decoder or multiplexer	1.67	3.73	2.06	1.34	3.95	2.61	1.87	3.83	1.96
9.Knowledge of latches or flip-flops	1.75	3.70	1.95	1.58	3.65	2.07	2.0	3.75	1.75
10.Knowledge of register or memory	1.86	3.54	1.68	2.07	3.23	1.16	2.53	3.83	1.30
11.Knowledge of FPGA	1.22	3.18	1.96	1.31	3.71	2.40	2.13	3.58	1.45
12.Knowledge of Verilog HDL	1.43	3.82	2.39	1.31	3.76	2.45	1.87	3.50	1.63

Table 3. Impact of CPBL on student skill growth (pre and post survey analysis).

Learning outcomes (Skills)	*Fall, 2008*			*Spring, 2009*			*Fall 2009*		
	Pre	*Post*	*diff*	*Pre*	*Post*	*diff*	*Pre*	*Post*	*diff*
1.General computing skills	4.08	4.45	0.37	4.08	4.19	0.11	4.6	4.42	-.18
2.Communication skills	4.08	4.36	0.28	4.08	4.33	0.15	4.2	4.0	-0.2
3.Math skills	4.24	4.54	0.30	4.12	4.28	0.16	4.27	4.5	0.23
4.General design skills	3.09	4.00	0.91	2.96	3.85	0.89	3.33	3.42	0.09
5.Engineering design skills	2.39	3.80	1.41	2.52	3.57	1.05	2.83	3.5	0.67
6.Ability to modularize the design process	1.82	3.78	1.96	2.09	3.50	1.41	2.8	3.67	0.87

[1] The data from Fall 2009 may not be as representative due to two reasons: 1) The pre-survey was not conducted at the very beginning of the quarter so the average score was higher; 2) it was the first time to use on-line survey and only 50% of the students responded. These problems are resolved in Winter 2010 by allocating dedicated time for students to complete online survey during the 1st lecture using Tablet PCs.

7.Ability to design a digital component or system	1.40	3.55	2.15	1.75	3.42	1.67	2.67	3.42	0.75
8.Ability to implement and verify a digital design using a simulation model	1.65	3.90	2.25	1.75	3.43	1.68	2.53	3.42	0.89
9.Ability to implement a digital design in hardware	1.35	3.80	2.45	1.70	3.42	1.75	2.40	3.25	0.85

To ensure a fair comparison, a control group is usually used in pre/post survey analysis. However, since only one session of EE244 (with maximum enrollment of 30 students) is offered per quarter, it is not practical to create control groups in our school. Instead of a control group, some "control questions" were placed in the survey to serve as the reference for the comparison. The control questions are the knowledge or skill outcomes that are not directly reinforced by CPBL (e.g. *Knowledge of register or memory / Math skills*, etc.). Accordingly to the three-quarter survey results in Tables 2 and 3, the top four knowledge outcomes associated with the largest increment in post survey scores are:

- Knowledge of Karnaugh-maps (K-maps)
- Knowledge of adder, decoder or multiplexer
- Knowledge of Verilog HDL (Hardware Description Language)
- Knowledge of FPGA (Field Programmable Gate Array)

And the top three skill outcomes associated with the largest increment in post survey scores are:

- Ability to design a digital component or system
- Ability to implement and verify a digital design using a simulation model
- Ability to implement a digital design in hardware

Evidently, the above outcomes are the ones that have been directly reinforced by CPBL. Specifically, our 2nd in-class project (7-segment LED decoder) directly enhanced the students' understanding in K-map simplification and the project series related to calculator reinforced the knowledge of adder and multiplexer. It is also clear that through the in-class projects, students acquired more knowledge of FPGA and Verilog HDL and improved their skills in the design, implementation and verification of digital systems.

For other learning outcomes that are not directly related to CPBL (e.g. knowledge outcome # 4, #5, #9 and #10), the pre and post survey results showed relatively smaller improvement. The least improvement occurred in the general skill outcomes (skill outcomes #1, #2, #3). This was expected since these skills were not directly reinforced by the course content. Also there was limited room for improvement since the students' self-ranking was high in the pre-survey. In summary, the analysis of the pre/post results demonstrated that the CPBL is quite effective in helping the students to understand course material and to develop design skills. This conclusion was reinforced by both the faculty observation of the students' performance and the results of student satisfaction survey (as shown in figure 1).

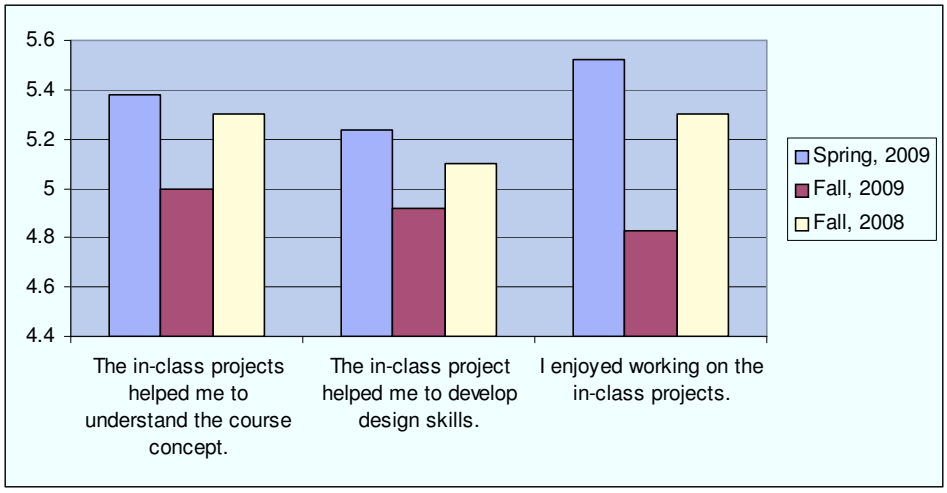

Figure 1. Students satisfaction survey results on CPBL in EE244 (1- don't know, 2-strongly disagree, 3- disagree, 4- neutral, 5- agree, 6- strongly agree).

2) Qualitative Assessment Analysis

Qualitative data from the focus group also highlighted the success of CPBL model using Tablet PC based collaborative learning. Most students considered the opportunities of conducting real world design via in-class projects as the most useful and valuable part in their learning experience. In addition, the students who participated in the focus group *unanimously said that because of the authenticity of the projects they have felt more interested in the Engineering field and almost all of them will continue taking more classes in Engineering*. Some of the comments from the students are:

"The project provided new challenges and chance to do authentic projects with technology. Without this project we would not have been able to come across something like this. It is directly applicable to engineering jobs."

"Using the hardware: I saw something real happen. It shows how much work is involved in doing something as simple as adding binary numbers and that how complex it is and how all the components need to fit with each other"

"I took this class before, and it was just lectures and lectures. This was the first time I got to see the design part and see visually how things work."

"I am from physics and I have developed a new liking for Engineering and I did not know this before."

"Content understanding was fantastic, we are no longer just using the textbook and just reading the theory, but we are uploading it on the board, using the software. It helped all of us who are visual learners"

Overall, the qualitative assessment results also showed that the implementation of CPBL has been successful. The interactive and collaborative Tablet PC based projects helped the students to create connections between the theory and the practice, and further stimulated the students' interest in engineering field. Neverthless, some concerns were raised during the focus group

discussion. Analysis of the student comments and concerns led to valuable findings that helped to improve our teaching strategy. The detials of the assessment findings will be introduced in the next section.

Assessment Findings

Incorporating CPBL into our freshman digital engineering class has been a challenging and rewarding experience. The feedback from the students has been overall very positive and they have also shared valuable insights into what they especially liked about the revised course and what could be improved. Anecdotally, the faculty have observed that after incorporating CPLB students are more engaged in the class and have a better grasp of the engineering design process. Here we would like to share our assessment findings that highlight both effective teaching strategies and areas of improvement.

What works well

In-depth analysis of assessment data revealed a number of teaching strategies that worked really well for our students:

- **Progressive learning via in-class projects**

The key component of CPBL model is a set of well-designed small projects to build up the students' knowledge and design skills in a progressive way. This idea proved to be very successful since it allowed the students to design a complex system step-by-step by completing a set of small projects. For example, the design of 4-bit calculator is a well-liked project by the students. To get the students prepared for the design of this real-world device using FPGA board, a number of small projects were created. Students start with the design and implementation of a 7-segment LED decoder, 1-bit adder, 4-bit adder/substractor, and eventually they can build the 4-bit calculator using these components.

- **Frequent direct asessment**

As part of restructuring the curriculum to create time for in-class projects, we replaced the two 100-minute midterms with five 20 minute quizzes. Quizzes are effective for keeping the students on track in this fast paced course where students must be on top of the class material to fully benefit from the in-class projects. In addition, using InkSurvey exercises [13, 14] provides students with an opportunity to apply class concepts and design principles with immediate feedback from the instructor.

- **Inquiry-based learning**

Rather than lead the students step-by-step through experiments, we are shifting over to more inquiry based learning. Examples of inquiry-based learning include: simple games to introduce the hardware components of FPGA board and basic engineering design process; open-ended discussion to explore various designs of calculator with different functions; an interactive exercise to guide the students to "discover" the characteristics of sequential logic. Assessment results showed that inquiry-based learning gernerally helped to engage students in the learning process and deepen their understanding of engineering concepts.

Challenges to be addressed

The challenges encountered have been mostly related to scheduling and adjusting activities to be more efficient and effective given the tight class schedule and the divserse student backgrounds:

- **How to balance between in-class project and direct instruction**

While students enjoyed the hands-on experience of CPBL, they also expressed their desire for direct instruction of course material. This in fact is one of the biggest challenges for the instructor, learning how to effectively and efficiently deliver the course content with value added from the in-class exercises and projects. It will take several more times teaching the course to find the right balance between showing by example, letting students try it through inquiry based exercises, and letting students apply it in their class projects.

- **How to sustain the project and still meet the needs of students with diverse educational background**

The diverse student population presented another big challenge for the instructors. It is difficult to control the pace of in-class projects since students come to this class with very different computer skills and knowledge levels. Some students even had difficulty starting up the Xilinx software or downloading files. With current NSF funding, TA support is available to offer extra help to the students in need. However, a solution must be devised to address this challenge to sustain the CPBL beyond the funding period. Currently, the PIs are exploring ways to get students more prepared and to make the in-class projects doable without TA support.

- **How to incorporate more hands-on activities**

Currently students use the FPGA board for three out of the five class projects. Students have indicated that they would like more hands-on activities using the FPGA board. We are exploring other opportunities to use the FPGA boards in class to reinforce lecture concepts through inquiry based learning opportunities.

Improving CPBL in Digital Design Course

Driven by the feedback from formal assessment as well as classroom observations, discussions with students, and personal experience with the teaching effectiveness and efficiency the PIs have been continually exploring ways to improve the CPBL experience for our students. In Winter 2009 a relatively major revision of the CPBL in Digital Design is being undertaken to address the challenges mentioned above. The major change is that in-class projects must be completed in one class period. Previously students were given one week to complete their class project write-up and due to the diverse educational backgrounds, some students were given even longer to complete their assignments. Students who could not complete the project in class (the majority of students) would attend additional TA help sessions. However, the intent of the CCLI project was not to create a parallel lab session, which was de facto happening, but rather to create in-class projects that provide a deeper understanding of the course material and improve retention through simple yet engaging design experiences. By ensuring that students can complete the in-class projects within one class period the CPBL becomes sustainable without TA support. Furthermore, students will get immediate feedback on their understanding of the material which was a major motivation behind creating the CPBL Digital Design experience.

The following is a summary of changes made to the implementation of CPBL to ensure that students complete their in-class projects within the class period and to improve the overall effectiveness of the CPBL:

a. Students use Tablet PCs with the DyKnow [15] class management software during every class period. This allows the instructor to embed simple inquiry based exercises using the FPGA board on non-project days.
b. Create a sequence of pre-project in-class inquiry based exercises to familiarize students with the design environment (FPGA prototype board, Verilog code examples, Xilinx development, simulation, and synthesis tools). Additional small hands-on inquiry based projects are being created to allow the student to use the FPGA board both in class and at home to reinforce class concepts not covered by the class projects such as decoders, multiplexers, flip flops, and shift registers.
c. All projects have an associated pre-project homework assignment. In-class projects should be a discovery process where student learn about different facets of engineering design process including simulation, synthesis, and testing as well as reinforce their understanding of the theoretical material. To be able to achieve these goals within class, students must come to class with some initial analysis and design completed for their projects. Previously only a couple projects required students to do pre-project homework and we observed that the students were much more engaged during these in-class projects and more likely to complete the projects on time
d. Streamline the class projects, step-by-step instructions, and associated worksheets to ensure that students have enough time to complete the project within 80 minutes (of a 100-minute class period). Students work collaboratively with their peers but each student must implement and test their own design.
e. Add group discussions of the in-depth questions to the end of the class period. To achieve the learning objectives it is not sufficient to just have students complete step-by-step instructions. In the past we have incorporated more in-depth questions in the project worksheet as after-class exercises to probe their understanding of the project and their knowledge of the underlying digital design fundamentals. While many students were able to answer these questions, some clearly struggled with the concepts. By adding small group discussions students can learn from their peers and receive immediate feedback from the instructor.
f. Students must submit their worksheets online at the end of the class using DyKnow panel submission. The instructor can then grade and provide comments and return them via DyKnow in a timely fashion.

Table 4 shows our revised class project list for Winter 2009 including the related pre-project in-class inquiry based experiments and a description of the associated pre-project homework. The most recent revisions are in italics. We briefly summarize the modifications below.

During class projects two through five students implement their pre-project homework designs, simulate (in some cases), synthesize, and perform hardware testing. While exposing students to the importance of simulation in the design process, hardware testing is especially important since students get great satisfaction from knowing that they have actually designed and implemented a physical component that could be used by others. For this reason, we have ensured that each class project involves hardware verification.

Students expressed that they would have really liked to be able to use the calculator that is designed in the final class project earlier in the quarter to learn about unsigned and signed numbers and 2's complement arithmetic. While we have previously included a first experience with the FPGA board, based on student recommendations we are replacing the ping-pong game with the binary calculator. The ping-pong game and other designs will be available for students to download and experiment with outside of class.

As we have continually evolved the experiments some quarters we included a project related to DeMorgan's theorem and in other quarters we did not. In the quarters it was included students demonstrated a much better understanding of DeMorgan's Theorem and its application and so it has been re-inserted for Winter 2009 even though it is not used in the final calculator project. The displaced full adder project has been converted into an inquiry based experiment where students are shown how to design it in Verilog and then get to experiment with the hardware implementation. Students will use the full adder in the hierarchical design of the 4-bit parallel adder/subtractor in class project 4.

Table 4. Brief description of revised class projects for Winter 2009 (revisions in italics).

Class Project	Description	Objectives
1	*Inquiry based experience with 4-bit binary calculator implemented on Xilinx FPGA Board.* ***Pre-Project In-class Inquiry Based Experiences:*** *None* ***Pre-Project Homework:*** *Decimal to binary conversion of unsigned and signed numbers. Binary addition and subtraction of 4-bit signed and unsigned numbers.*	Familiarize students with FPGA prototype board and software for programming board. Reinforce students understanding of signed and unsigned numbers and 2's complement arithmetic.
2	Prove DeMorgan's Theorem through Verilog structural modeling, simulation, and *hardware testing*. ***Pre-Project In-class Inquiry Based Experiences:*** *Demonstration of structural modeling in Verilog of simple logic gate followed by student hardware testing to determine type of a mystery gate.* *Demonstration of interconnecting multiple gates in Verilog to implement simple logic functions and demonstration of Verilog simulation and waveform verfication. Students generate truth table from waveform.* ***Pre-Project Homework:*** *Use of truth tables to verify DeMorgan's Theorem. Implement invert-OR/AND-invert and invert-AND/OR-invert designs and Verilog code on paper.*	Introduce students to structural modeling in Verilog, simulation, *synthesis*, and Xilinx Webpack design environment. Reinforce students understanding of DeMorgan's Theorem and *how it can be implemented in hardware*.
3	Design of a BCD to 7-Segment Display decoder through Verilog structural modeling and hardware testing. ***Pre-Project In-class Inquiry Based Experiences:*** *Use of Verilog modeling and simulations to demonstrate that application of Karnaugh-maps can produce an equivalent optimized function. Students visually compare waveforms to verify correctness and find mistakes in K-map application when waveforms don't agree.*	Introduce students to more complex hardware components and their control (7-segment display with time multiplexed control). Reinforce students understanding of Karnaugh maps and combinational logic design.

	Pre-Project Homework: Implementation of 7-segment display decoder using K-maps with don't care conditions. Paper designs of two segments with their corresponding Verilog code.	
4	Hierarchical design of a 4-bit parallel adder-subtractor through Verilog hierarchical modeling and hardware testing. ***Pre-Project In-class Inquiry Based Experiences:*** *Demonstration of combinational logic design of a full adder and its implementation and simulation in Verilog. Students hardware test the full adder to verify its correctness.* ***Pre-Project Homework:*** *Paper design of a 4-bit parallel adder-subtractor circuit with overflow detection. Write Verilog code of adder using existing full adder and multiplexer modules.*	Introduce students to hierarchical design process. Reinforce students understanding of full adder, parallel adder-subtractor, and 2's complement arithmetic.
5	System design of 4-bit binary calculator with decimal display. This is a culminating project building upon their experience with signed numbers from class project 1 and incorporating their designs from class projects 3 and 4. ***Pre-Project In-class Inquiry Based Experiences:*** *Further class experimentation with 4-bit parallel adder-subtractor test circuit using switches and LEDs but no registers to store results to explore the usefulness of holding state. Demonstration of sequential logic design of a counter. Students use hardware testing to determine the state diagram of a mysterious counter.* ***Pre-Project Homework:*** *Complete the paper design of a 4-bit binary calculator properly interconnecting the components including registgers and flip-flops.*	Introduce students to system-level design. Reinforce students understanding of signed and unsigned overflow.

Conclusion and Future Work

In this paper, we presented the assessment results of the NSF sponsored CCLI project entitled "Collaborative Project-based Learning to Enhance Freshman Design Experience in Digital Engineering." Both quantitative and qualitative data were collected and analyzed. The assessment findings proved that our proposed CPBL was effective and highlighted some successful teaching strategies such as inquiry-based learning and frequent direct assessment. Several challenges were also revealed, e.g. *how to balance between in-class project and direct instruction*, *how to sustain the project while meeting the students' needs*, and *how to incorporate more in-class projects*. To continuously improve the CPBL experience for our students, the PIs have worked out a procedure to better prepare the students for the in-class project and to deepen their understanding of engineering design through the project experience. In addition, the curriculum and project activities are being adjusted such that a sustainable solution can be found to support in-class project in an educational environment with limited resources.

Acknowledgment

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