I. Introduction

The following project is a design of an infrared emitter-detector circuit. It reviews some of the concepts and applications the students have learned during the first few semesters in the Electrical Engineering Technology program at Purdue University. The advantage of this project is that it progresses in steps that are manageable and easily to conduct laboratory activities.

The project consists of an analog part and a digital part. An infrared light source is modulated at a frequency of 4 kHz and placed in front of a detector. The signal detected by the phototransistor is then processed through a series of analog circuits. The circuit indicates when the infrared beam is blocked. The block diagram of the analog part of the project is shown in Figure 1 below.

![Figure 1 – Block Diagram of the Analog Part](image-url)
When the IR beam is blocked, the digital part of the circuit would display the blockage time to 1/100 of a second. The block diagram of the digital part is given in Figure 2 below.

![Block Diagram of the Digital Part](image)

**Figure 2 – Block Diagram of the Digital Part**

II. The Analog Part

A. The Oscillator and Driver

A 555 Timer is used in its astable mode as an oscillator. The schematic diagram of an astable 555 Timer and a transistor driver is shown in Figure 3 on the next page. In astable mode, the output of the Timer is a square wave whose frequency is calculated as:

\[
f = \frac{1.44}{(R_1 + 2R_2)(C_1)}
\]

In the design, since the desired frequency is 4 kHz, let \(C_1 = 0.0047 \, \mu F\).

Thus,

\[
R_1 + 2R_2 = \frac{1.44}{(4 \, \text{kHz})(0.0047 \, \mu F)} = 76.6 \, \text{k}\Omega
\]

Let \(R_2 = 33 \, \text{k}\Omega\), then,

\[
R_1 = 76.6 \, \text{k}\Omega - 2(33 \, \text{k}\Omega) = 10.6 \, \text{k}\Omega
\]
Since 10.6 kΩ is not a standard value, let R\textsubscript{1} be 10 kΩ.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{oscillator_driver_circuits.png}
\caption{Oscillator and Driver Circuits}
\end{figure}

Using the selected values of the components to re-calculate the output frequency of the Timer, we obtain the frequency of:

\[
f = \frac{1.44}{[10 \text{ kΩ} + 2(33 \text{ kΩ})](0.0047 \text{ µF})} = 4.031 \text{ kHz}
\]

which is close to what we desire.

The duty cycle of the square wave is:

\[
\text{Duty Cycle} = \frac{R\textsubscript{1} + R\textsubscript{2}}{R\textsubscript{1} + 2R\textsubscript{2}} \times 100\% = \frac{10 \text{ kΩ} + 33 \text{ kΩ}}{10 \text{ kΩ} + 2(33 \text{ kΩ})} \times 100\% = 56.6\%
\]

In Figure 3, the capacitor C\textsubscript{2} is used to eliminate positive overshoot (if there is any). Its value can be from 10 µF up to 100 µF. Capacitor C\textsubscript{3} is optional and has no effect in the operation. It is used to bypass the control (pin 5) to ground. Figure 4 on the next page shows the waveform of the 555 Timer output voltage.
The infrared emitter is obtained from RadioShack (part # 276-143) and it requires a continuous current of 20 mA and a forward biased voltage of 1.3 V. Since the IR emitter is driven by a square wave of 4 kHz in frequency (period of 250 µs) and 56.6% duty cycle, the 20 mA current can be considered as the average current through the emitter. Thus, the peak value of the current is calculated as following:

\[
\text{On Time} = (0.566)(250 \, \mu s) = 141.5 \, \mu s
\]

\[
\text{Peak Current} = \frac{(20 \, mA)(250 \, \mu s)}{141.5 \, \mu s} = 35.3 \, mA
\]

With this amount of current, the 555 Timer operates at:

\[
P = (15 \, V)(35.3 \, mA) = 529.5 \, mW
\]

Which is close to its maximum power specification (600 mW). Therefore, a transistor driver is designed to allow the Timer to operate at a lower power level.

Let the IR emitter current be 35 mA, the collector resistor of the driver is calculated as:

\[
R_4 = \frac{V_{CC} - V_D}{I_D} = \frac{15 \, V - 1.3 \, V}{35 \, mA} = 391.4 \, \Omega
\]
Since the above value of $R_4$ is not standard, use a $390 \, \Omega$ resistor. Then, the IR emitter current is:

$$I_D = \frac{V_{CC} - V_D}{R_4} = \frac{15 \, \text{V} - 1.3 \, \text{V}}{390 \, \Omega} = 35.13 \, \text{mA}$$

To ensure the transistor is operating in its switching mode, the base current has to be at least 10% of the collector current. Let the base current $I_B$ be 4 mA, the base resistor can be calculated as:

$$R_3 = \frac{V_{BB} - V_{BE}}{I_B} = \frac{14 \, \text{V} - 0.7 \, \text{V}}{4 \, \text{mA}} = 3.325 \, \text{k}\Omega$$

Since the above value of $R_3$ is not standard, use a $3.3 \, \text{k}\Omega$ resistor. Then, the base current is:

$$I_B = \frac{V_{BB} - V_{BE}}{R_3} = \frac{14 \, \text{V} - 0.7 \, \text{V}}{3.3 \, \text{k}\Omega} = 4.03 \, \text{mA}$$

This will ensure the hard saturation of the transistor when the input voltage is 14 V peak. Basically at this point of the design, the infrared emitter is blinking at the frequency of 4 kHz. These circuits are connected on the right most side of the protoboard because the Timer is very noisy and we try to keep it as farther away as possible from the beginning of the detection circuit.

**B. The Detector, the Passive High Pass Filter, and the Non-Inverting Amplifier**

The schematic diagram of the first section of the detection circuit is shown in Figure 5 on the next page. The component used to detect the IR source is a phototransistor (RadioShack part # 276-145) connected with a DC collector bias configuration. The phototransistor is mounted on the left most side of the protoboard aiming at the IR emitter. The output voltage $v_{out1}$ of this circuit has an ac signal (from “seeing” the IR source and ambient light) and a DC offset from the biasing. The values of these voltages vary depending on ambient light, the alignment and the distance between the IR source and the phototransistor. In my setup, the DC offset voltage is 150 mV. The ac signal consists of two main signals: an “almost” square wave with a peak-to-peak value of approximately 50 mV at the frequency of 4 kHz riding on a sine wave with a peak-to-peak value of 80 mV at the frequency of 60 Hz. The 4 kHz signal comes from the IR source being detected and the 60 Hz signal comes from ambient light. Figure 6 on the next page shows the waveform of $v_{out1}$.
Figure 5 – The Detector, Filter, and Amplifier

Figure 6 – Waveform of $v_{out1}$
Since the 4 kHz signal is the only one we wish to retain, a passive high pass filter is used to eliminate the DC offset and the 60 Hz signal. This high pass filter consists of capacitor \( C_4 \) and resistor \( R_6 \). The cutoff frequency of this filter is calculated as:

\[
f_0 = \frac{1}{2\pi R_6 C_4}
\]

Let \( f_0 \) be 1 kHz (this arbitrary frequency is low enough to pass the 4 kHz signal and is high enough to block the DC and 60 Hz signals) and \( C_4 \) be 0.47 µF:

\[
R_6 = \frac{1}{2\pi f_0 C_4} = \frac{1}{2\pi (1 \text{ kHz})(0.47 \text{ µF})} = 338.6 \text{ Ω}
\]

Since the above value is not standard, select \( R_6 \) to be 330 Ω. Then, the cutoff frequency is:

\[
f_0 = \frac{1}{2\pi R_6 C_4} = \frac{1}{2\pi (330 \text{ Ω})(0.47 \text{ µF})} = 1.026 \text{ kHz}
\]

The signal passing through this passive high pass filter becomes an “almost” square wave with its peak-to-peak value of about 48 mV. The DC offset and 60 Hz signals are eliminated. The waveform of this voltage \( v_{out2} \) is in Figure 7.

![Figure 7 – Waveform of \( v_{out2} \)](image-url)
This signal is then amplified with a factor of 11. To do this, a Non-Inverting amplifier is used. The closed-loop gain of this amplifier is:

\[ K = 1 + \frac{R_8}{R_7} \]

Since the desired gain is 11, the ratio of \( R_8/R_7 \) is 10.

Let \( R_8 \) be 15 kΩ, then,

\[ R_7 = \frac{R_8}{10} = \frac{15 \text{ kΩ}}{10} = 1.5 \text{ kΩ} \]

The peak-to-peak value of the output voltage of the Non-Inverting amplifier is:

\[ v_{out3} = Kv_{out2} = (11)(48 \text{ mV}) = 0.528 \text{ V} \]

Figure 8 below shows the waveform of this output.

![Figure 8 – Waveform of \( \text{v}_{out3} \)](image)

C. The Butterworth Second Order Active High Pass Filter

To further prevent interference from other light sources, a Second Order Active High Pass filter with a Q value of 6 is used. Since this filter has a high Q, around the center frequency it behaves...
very similarly to a band pass filter. The normalized frequency response of this filter is in Figure 9 below.

![Normalized Frequency Response for Q = 6](image)

Figure 9 – Normalized Frequency Response for Q = 6

The schematic diagram of the filter is below.

![Second Order Active High Pass Filter](image)

Figure 10 – Second Order Active High Pass Filter
In this circuit, if we let \( R_9 = R_{10} = R \) and \( C_5 = C_6 = C \), the center frequency is calculated as:

\[
 f_0 = \frac{1}{2\pi RC}
\]

In this filter, the desired center frequency is 4 kHz. Let \( C = 0.0022 \mu\text{F} \):

\[
 R = \frac{1}{2\pi f_0 C} = \frac{1}{2\pi (4 \text{ kHz})(0.0022 \mu\text{F})} = 18.085 \text{ k}\Omega
\]

Use 18 k\( \Omega \) resistors for \( R_9 \) and \( R_{10} \), 0.0022 \( \mu\text{F} \) capacitors for \( C_5 \) and \( C_6 \). Note that matching the resistor and capacitor values within 1% of their calculated values will ensure the performance of the project.

For the resistor value of 18 k\( \Omega \), the center frequency of the filter is:

\[
 f_0 = \frac{1}{2\pi RC} = \frac{1}{2\pi (18 \text{ k}\Omega)(0.0022 \mu\text{F})} = 4.02 \text{ kHz}
\]

This frequency is very close to the desired frequency of 4.031 kHz.

The Q value of the filter is calculated as:

\[
 Q = \frac{1}{3 - K}
\]

where \( K \) is the closed-loop gain of the amplifier.

For Q of 6, the closed-loop gain is calculated as:

\[
 K = 3 - \frac{1}{Q} = 3 - \frac{1}{6} = 2.83333
\]

Since this gain is \( 1 + (R_{12}/R_{11}) \), the ratio of \( R_{12}/R_{11} \) is 1.83333.

Let \( R_{11} \) be 12 k\( \Omega \),

\[
 R_{12} = 1.83333(12 \text{ k}\Omega) = 22 \text{ k}\Omega
\]

If it is possible, use precision resistors for \( R_{11} \) and \( R_{12} \) because a slight change in their values will cause a significant change in Q. For example, if the resistors have 5% tolerance, the maximum
value of $R_{12}$ can be $23.1 \, \text{k}\Omega$ and the minimum value of $R_{11}$ can be $11.4 \, \text{k}\Omega$. Then, the closed-loop gain of the amplifier is:

$$K = 1 + \frac{23.1 \, \text{k}\Omega}{11.4 \, \text{k}\Omega} = 3.026$$

This value of the gain forces the $Q$ value to be negative. The filter becomes an oscillator. The output voltage $v_{\text{out}4}$ of this filter is a sine wave with its peak value of approximately $4.5 \, \text{V}$. The waveform of this output is in Figure 11 below. This output $v_{\text{out}4}$ becomes zero when the IR beam is blocked.

![Figure 11 – Waveform of $v_{\text{out}4}$](image)

D. The Absolute Value Circuit

The Absolute Value Circuit is used to double the operating frequency of the project to enhance the performance of the Peak Detector Circuit. This circuit is also called an Active Rectifier. Its schematic diagram is in Figure 12 on the next page. In the circuit resistors $R_{13}$ through $R_{17}$ are equal in value. Let $R_{13} = R_{14} = \ldots = R_{17} = R$. Also in the analysis of this circuit, we use ideal diode for the ease of establishing the equivalent circuits for different cycles of the input voltage. The output $v_{\text{out}6}$ of this circuit is zero when the IR beam is blocked.
During the positive half cycle of the input voltage, diode D\textsubscript{2} behaves as a short (use ideal diodes) and diode D\textsubscript{3} acts as an open. The circuit becomes:

The first part of the circuit acts as an Inverting Amplifier with a unity gain. Thus, the voltage \( v_{\text{out5}} \) is:
The second part of the circuit behaves as a Summing Amplifier. The output of this amplifier is:

\[
\begin{align*}
\text{v}_{\text{out}6} &= -R_{18} \left[ \frac{\text{v}_{\text{out}4}}{R_{15}} + \frac{\text{v}_{\text{out}5}}{R_{16}} + \frac{\text{v}_{\text{out}5}}{R_{17}} \right] \\
&= -18 \text{k}\Omega \left[ \frac{\text{v}_{\text{out}4}}{12 \text{k}\Omega} + \frac{\text{v}_{\text{out}5}}{12 \text{k}\Omega} + \frac{\text{v}_{\text{out}5}}{12 \text{k}\Omega} \right]
\end{align*}
\]

\[
\text{v}_{\text{out}6} = -\frac{18 \text{k}\Omega}{12 \text{k}\Omega} \left( \text{v}_{\text{out}4} + \text{v}_{\text{out}5} + \text{v}_{\text{out}5} \right) = -\frac{18 \text{k}\Omega}{12 \text{k}\Omega} \left( \text{v}_{\text{out}4} - \text{v}_{\text{out}4} - \text{v}_{\text{out}4} \right) = \frac{18 \text{k}\Omega}{12 \text{k}\Omega} \left( \text{v}_{\text{out}4} \right)
\]

The positive half cycle of the input voltage is amplified by a gain of \(18 \text{k}\Omega/12 \text{k}\Omega = 1.5\).

During the negative half cycle of the input voltage, diode D2 acts as an open and diode D3 behaves as a short. Figure 14 shows the equivalent circuit for this cycle.

\[
\begin{align*}
\text{v}_{\text{out}5} &= -\frac{R_{14}}{R_{13}} \text{v}_{\text{out}4} = -\frac{12 \text{k}\Omega}{12 \text{k}\Omega} \text{v}_{\text{out}4} = -\text{v}_{\text{out}4}
\end{align*}
\]

Figure 14 – Equivalent Circuit During Negative Half Cycle

The first part of the circuit behaves as an Inverting Amplifier with a gain of zero because the feedback resistor (from pin 6 to pin 2 of the 741) is a short. Thus, the voltage at \(v_x\) is zero. It is also because \(v_x\) is at virtual ground. This effectively removes \(R_{14}\), \(R_{16}\) and \(R_{17}\) from the circuit. Therefore, the second part of the circuit becomes another Inverting Amplifier and its output is:
Thus, the input voltage is inverted and amplified by a factor of 1.5. The voltage $v_{out6}$ is a full-wave rectified signal with its peak value to be:

$$V_{out6\, peak} = 1.5 \times (V_{out4\, peak}) = 1.5 \times (4.5 \, V) = 6.75 \, V$$

Figure 15 shows the waveform of $v_{out6}$. It has a peak value of 6.75 V and a frequency of 8 kHz. In order for the circuit to function properly, matching resistors $R_{13}$ through $R_{17}$ is very important.

![Figure 15 – Waveform of $v_{out6}$](image)

E. The Peak Detector Circuit

The Peak Detector circuit converts the full-wave rectified output signal from the Absolute Value Circuit into an “almost” DC signal. Figure 16 on the next page shows the configuration of this circuit. The output $v_{out7}$ has a ripple voltage riding on a DC level. The peak-to-peak value of this ripple voltage is calculated as:

$$V_{ripples} = \frac{I}{fC7}$$
When the time constant $R_{20}C_7$ is much larger than the period of the wave, the conversion will take place. The larger the time constant, the smoother the output $v_{out7}$ will be. However, if there is any change in the input voltage level, a very large time constant will result in a very slow response time. Thus, in the design, we must try not to go to either extreme of having a very smooth output or very quick response time. In the circuit, the time constant is:

$$\tau = R_{20}C_7 = (5.6 \, \text{k}\Omega)(0.47 \, \mu\text{F}) = 2.632 \, \text{ms}$$

The period of the input signal is:

$$T = \frac{1}{f} = \frac{1}{8 \, \text{kHz}} = 125 \, \mu\text{s}$$

From the above calculations, the conversion from a full-wave rectified signal into an “almost” DC signal will take place. The diode $D_4$ prevents the discharging of the capacitor back to the output of the 741 operational amplifier and the feedback resistor $R_{19}$ is much larger than $R_{20}$ ensuring the resistor $R_{20}$ would control the discharging of the capacitor.

The approximate DC current is:

$$I = \frac{V_{out7}}{R_{20}} = \frac{6.75 \, \text{V} - 0.7 \, \text{V}}{5.6 \, \text{k}\Omega} = 1.08 \, \text{mA}$$

The peak-to-peak value of the ripple voltage is:

$$V_{\text{RIPPLE}} = \frac{I}{fC_7} = \frac{1.03 \, \text{mA}}{(8 \, \text{kHz})(0.47 \, \mu\text{F})} = 0.27 \, \text{V}$$
Figure 17 below shows the output $v_{out7}$ of the circuit. This voltage has an ac signal riding on a DC level. This voltage will come down to zero when the IR beam is blocked.

![Waveform of $v_{out7}$](image)

**Figure 17 – Waveform of $v_{out7}$**

F. The Voltage Comparator

Up to this point of the design, the output voltage $v_{out7}$ is a DC signal of about 6 V when the IR detector “sees” the IR beam and this voltage goes to 0 V when the beam is blocked. The Voltage Comparator is used to give an indication when blockage occurs. Figure 18 shows the schematic diagram of the comparator. The circuit utilizes the open-loop gain of the 741 operational amplifier. The voltage $v_{out7}$ is fed into the inverting input of the opamp and a voltage divider is set up as a reference voltage at the non-inverting input. A 100 kΩ potentiometer $R_{21}$ is used for this purpose to vary the reference voltage when necessary because in the design, the voltage $v_{out7}$ varies depending on the intensity of the IR emitter, the alignment and distance between the emitter and the phototransistor and ambient light.

When the reference voltage is less than the voltage $v_{out7}$, the open-loop gain causes the comparator to produce a negative saturation voltage (about $-14.5$ V). When the reference voltage is more than the voltage $v_{out7}$, the open-loop gain causes the comparator to produce a positive saturation voltage (about $+14.5$ V). In the design, we set the reference voltage to 5 V.

The positive saturation voltage is used to drive an LED. Let the current flowing through the LED be 20 mA, and the forward biased voltage of the LED be 1.2 V, the current limiting resistor $R_{22}$ is calculated as:
R_{22} = \frac{14.5 \text{ V} - 1.2 \text{ V}}{I_{\text{LED}}} = \frac{13.3 \text{ V}}{20 \text{ mA}} = 665 \text{ Ω}

Use a 680 Ω for R_{22}.

![Figure 18 – The Voltage Comparator](image)

The voltage \(v_{\text{out8}}\) is for the digital part of the design.

III. The Digital Part

The primary function of this part is to display the time of the blockage. When the IR beam is blocked, the three-digit display resets itself to 0.00 and starting counting the blockage time.

Figure 19 on the next page shows the schematic diagram of this part. The transistor switch is used to attenuate the output voltage \(v_{\text{out8}}\) as well as to produce a falling edge for the monostable-multivibrator circuit and a LO voltage level to enable the count sequence. The 555 Timer is designed to generate a clock signal of 100 Hz to clock the first counter. The one-shot generates a 10 ms pulse to reset the counters. In Figure 19, only one counter, one decoder/driver, and one seven-segment display are shown. For the remaining two digits, the connections are noted in the Figure.
Figure 19 – The Digital Part

Bibliography

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