I. Introduction

The following project is a design of a simple infrared emitter-detector circuit used as a remote control to turn on and off an ac light bulb. It reviews some of the basic concepts and applications the students have learned during the first few semesters in the Electrical Engineering Technology program at Purdue University. The advantage of this project is that it consists of off-the-shelf parts and it progresses in steps that are manageable and easily to conduct laboratory activities.

The project has an analog part and a digital part. An infrared light source emits two modulated signals at the frequencies of 1 kHz and 4 kHz. A phototransistor detects the signals and passes them through a series of analog circuits for processing. When the infrared source emits the 1 kHz signal, a light bulb is on and the 4 kHz signal commands to turn off the bulb. When the bulb is on, the digital part of the circuit would reset the time to 00.0 and would display the on time of the bulb to 1/10 of a second. When the bulb is off, this circuit freezes the displayed time. The block diagram of the analog part of the project is in Figure 1 below.

![Block Diagram of the Analog Part](image-url)
Figure 2 below shows the block diagram of the digital part of the project.

![Block Diagram of the Digital Part](image)

Figure 2 – Block Diagram of the Digital Part

II. The Analog Part

A. The Oscillator and Driver

A 555 Timer is used in its astable mode as an oscillator. The schematic diagram of the Timer and a transistor driver is shown in Figure 3 on the next page. We will look at the Timer operation under three conditions: both NC momentary PB switches SW₁ and SW₂ are closed, SW₁ is open, and SW₂ is open.

1. Both SW₁ and SW₂ are closed

Under this condition, both timing capacitors C₁ and C₂ are shorted out. The output voltage V₁ of the Timer is a DC signal of approximately the power supply voltage of 15 V.

The base current of the transistor driver is:

\[ I_B = \frac{V_1 - 0.7 \text{ V}}{R_3} = \frac{15 \text{ V} - 0.7 \text{ V}}{3.3 \text{ k}\Omega} = 4.33 \text{ mA} \]

The maximum collector current of the transistor driver is:

\[ I_{C_{\text{MAX}}} = \frac{V_{CC}}{R_4} = \frac{15 \text{ V}}{560 \text{ } \Omega} = 26.80 \text{ mA} \]
Since the base current is more than 10% of the maximum collector current, the transistor is in hard-saturation. Thus, the voltage $V_2$ is zero resulting in the IR emitter $D_1$ being off.

The power dissipated in resistor $R_4$ is:

$$P_{R4} = (26.80 \text{ mA})^2 (560 \Omega) = 0.4 \text{ W}$$

Therefore, use a $\frac{1}{2}$ W resistor for $R_4$ as shown in Figure 3.

2. Switch $SW_1$ is open

When switch $SW_1$ is open, the timing capacitor $C_1$ controls the output frequency. The output of the Timer is a square wave with its peak value of approximately 15 V and its frequency of:

$$f = \frac{1.44}{(R_1 + 2R_2)(C_1)}$$
In the design, since the desired frequency is 1 kHz, let $C_1 = 0.0047 \mu F$.

Thus,

$$
R_1 + 2R_2 = \frac{1.44}{(1 \text{ kHz})(0.0047 \mu F)} = 306.4 \text{ k}\Omega
$$

Let $R_2 = 150 \text{ k}\Omega$, then,

$$
R_1 = 306.4 \text{ k}\Omega - 2(150 \text{ k}\Omega) = 6.4 \text{ k}\Omega
$$

Since 6.4 k\Omega is not a standard value, let $R_1$ be 6.8 k\Omega.

Using the selected values of the components to re-calculate the output frequency of the Timer, we obtain the frequency of:

$$
f = \frac{1.44}{(R_1 + 2R_2)(C_1)} = \frac{1.44}{[6.8 \text{ k}\Omega + 2(150 \text{ k}\Omega)](0.0047 \mu F)} = 998.6 \text{ Hz} \approx 1 \text{ kHz}
$$

which is about the desired frequency.

The duty cycle of the square wave is:

$$
\text{Duty Cycle} = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\% = \frac{6.8 \text{ k}\Omega + 150 \text{ k}\Omega}{6.8 \text{ k}\Omega + 2(150 \text{ k}\Omega)} \times 100\% = 51.1\%
$$

During the off cycle of the Timer output voltage $V_1$, the transistor is in cut-off. Therefore, the IR emitter is on with a current of:

$$
I_{IR} = \frac{15 \text{ V} - 1.2 \text{ V}}{560 \Omega} = 24.6 \text{ mA}
$$

During the on cycle of the Timer output voltage $V_1$, the transistor is in saturation. Thus, the IR emitter is off.

In Figure 3, the capacitor $C_3$ eliminates positive overshoot (if there is any). Its value can be from 10 µF up to 100 µF. The capacitor $C_4$ is optional and has no effect in the operation. It bypasses the Timer control (pin 5) to ground.
The infrared emitter is from RadioShack (part # 276-143). When switch SW1 opens, the IR emitter “blinks” at the frequency of 1 kHz.

3. Switch SW2 is open

When switch SW2 opens, the timing capacitor C2 controls the output frequency. The output of the Timer is a square wave with its peak value of approximately 15 V and its frequency of:

\[
 f = \frac{1.44}{(R_1 + 2R_2)(C_2)}
\]

In the design, since the desired frequency is 4 kHz, R1 and R2 have been selected previously, the capacitance C2 is:

\[
 C_2 = \frac{1.44}{(R_1 + 2R_2)(f)} = \frac{1.44}{[6.8 \text{ k}\Omega + 2(150 \text{ k}\Omega)](4 \text{ kHz})} = 0.00117 \mu\text{F}
\]

Since 0.00117 \mu\text{F} is not a standard value, we select a 0.0012 \mu\text{F} capacitor.

Using the selected values of the components to re-calculate the output frequency of the Timer, we obtain the frequency of:

\[
 f = \frac{1.44}{(R_1 + 2R_2)(C_2)} = \frac{1.44}{[6.8 \text{ k}\Omega + 2(150 \text{ k}\Omega)](0.0012 \mu\text{F})} = 3.91 \text{ kHz} \approx 4 \text{ kHz}
\]

The duty cycle of the square wave is the same as in the previous condition because the R1-R2 values remain unchanged. Therefore, the IR emitter is “blinking” at the frequency of 4 kHz when switch SW2 opens.

The waveforms of the 555 Timer output voltage V1 and the transistor driver voltage V2 under three conditions are in Figure 3.

The oscillator and driver circuits are in a box shown in Figure 4 on the next page. This is the remote control to turn on and off the ac load.
B. The Detector, the Passive High Pass Filter, and the Non-Inverting Amplifier

The component used to detect the IR source is a phototransistor (RadioShack part # 276-145). The phototransistor is inside a box (RadioShack part # 270-211) that has an IR optical filter to minimize the effect of ambient light. This filter allows the IR wavelengths to pass through and blocks most of other light sources in visible spectrum. Figure 5 below shows the set up of the phototransistor box.
The schematic diagram of the first section of the detection circuit is in Figure 6 on the next page. The output voltage $V_3$ of this circuit has an ac signal (from “seeing” the IR source and ambient light) and a DC offset from the biasing. The values of these voltages vary depending on ambient light, the alignment and the distance between the IR source and the phototransistor. In our setup, the DC offset voltage is about 12 V. The brighter ambient light results in a less collector-emitter impedance of the phototransistor. Thus, the DC offset voltage decreases as the intensity of ambient light increases. The ac signal is an “almost” square wave with a peak-to-peak value of approximately 2 mV at the frequency of 1 kHz when switch SW$_1$ opens and 4 kHz when switch SW$_2$ opens. These ac signals come from the IR source being detected by the phototransistor. The waveform of this voltage is in Figure 6 on the next page.

Since the 1 kHz and 4 kHz signals are the only ones we wish to retain, a passive high pass filter is used to eliminate the DC offset and the 60 Hz interference from ambient light. This high pass filter consists of capacitor $C_5$ and resistor $R_6$. The cutoff frequency of this filter is:

$$f_0 = \frac{1}{2\pi R_6 C_5}$$

![Figure 6 – The Detector, Filter, and Amplifier](image-url)
Let $f_o$ be 700 Hz (this arbitrary frequency is low enough to pass the 1 kHz and 4 kHz signals and is high enough to block the DC and 60 Hz signals) and $C_5$ be 0.22 $\mu$F:

$$R_6 = \frac{1}{\frac{2\pi f_oC_5}{2\pi(700 \, \text{Hz})(0.22 \, \mu\text{F})}} = 1.03 \, \text{k}\Omega$$

Since the above value is not standard, select $R_6$ to be 1 k$\Omega$. Then, the cutoff frequency is:

$$f_o = \frac{1}{\frac{2\pi R_6C_5}{2\pi(1 \, \text{k}\Omega)(0.22 \, \mu\text{F})}} = 723.4 \, \text{Hz}$$

The signal passing through this passive high pass filter becomes an “almost” square wave with its peak-to-peak value of about 2 mV at 1 kHz when switch SW1 opens. The filter eliminates the DC offset and ambient interference.

When switch SW2 opens, the waveform is similar except that the frequency is 4 kHz. The waveforms of voltage $V_4$ under different conditions are in Figure 6.

This signal is then amplified with a factor of 101. To do this, we use a Non-Inverting amplifier. The closed-loop gain of this amplifier is:

$$K = \frac{R_8}{1 + \frac{R_8}{R_7}}$$

Since the desired gain is 101, the ratio of $R_8/R_7$ is 100.

Let $R_8$ be 120 k$\Omega$, then,

$$R_7 = \frac{R_8}{100} = \frac{120 \, \text{k}\Omega}{100} = 1.2 \, \text{k}\Omega$$

The peak-to-peak value of the output voltage of the Non-Inverting amplifier is:

$$V_5 = KV_4 = (101)(2 \, \text{mV}) = 0.202 \, \text{V} = 0.2 \, \text{V}$$

Figure 6 also shows the waveforms of this output.
C. The Butterworth Second Order Active High Pass/Low Pass Filters

To further prevent interference from other light sources and re-condition the signals, we use two Second Order Active filters with a Q value of 6. Since these filters have a high Q, around the center frequency they behave very similarly to band pass filters. Figures 7 shows the normalized frequency responses of these filters.

Figure 7 – High Pass/Low Pass Normalized Frequency Response for Q = 6

Figure 8 – Second Order Active High Pass/Low Pass Filters
Let’s focus onto the top high pass filter. In this circuit, if we let $R_{13} = R_{14} = R$ and $C_6 = C_7 = C$, the center frequency is:

$$f_0 = \frac{1}{2\pi RC}$$

In this filter, the desired center frequency is 4 kHz. Let $C$ be 0.0033 $\mu$F:

$$R = \frac{1}{2\pi f_0 C} = \frac{1}{2\pi (4 \text{ kHz})(0.0033 \text{ $\mu$F})} = 12.057 \text{ k}\Omega$$

Use 12 k$\Omega$ resistors for $R_{13}$ and $R_{14}$, 0.0033 $\mu$F capacitors for $C_6$ and $C_7$. Note that matching the resistor and capacitor values within 1% of their calculated values will ensure the performance of the filter.

For the resistor value of 12 k$\Omega$, the center frequency of the filter is:

$$f_0 = \frac{1}{2\pi RC} = \frac{1}{2\pi (12 \text{ k}\Omega)(0.0033 \text{ $\mu$F})} = 4.019 \text{ kHz}$$

This frequency is very close to the desired frequency of 3.91 kHz.

The Q value of the filter is calculated as:

$$Q = \frac{1}{3 - K}$$

where $K$ is the closed-loop gain of the amplifier.

For $Q$ of 6, the closed-loop gain is calculated as:

$$K = 3 - \frac{1}{Q} = 3 - \frac{1}{6} = 2.83333$$

Since this gain is $[1 + (R_{15}/R_{11})]$, the ratio of $R_{15}/R_{11}$ is 1.83333.
Let $R_{11}$ be 12 kΩ,

$$R_{15} = 1.83333(\ 12 \text{ kΩ}) = 22 \text{ kΩ}$$

If it is possible, use precision resistors for $R_{11}$ and $R_{15}$ because a slight change in their values will cause a significant change in Q. For example, if the resistors have 5% tolerance, the maximum value of $R_{15}$ can be 23.1 kΩ and the minimum value of $R_{11}$ can be 11.4 kΩ. Then, the closed-loop gain of the amplifier is:

$$K = 1 + \frac{23.1 \text{ kΩ}}{11.4 \text{ kΩ}} = 3.026$$

This value of the gain forces the Q value to be negative resulting in oscillation of the circuit.

On the other hand, with 5% tolerance, the minimum value of $R_{15}$ can be 20.9 kΩ and the maximum value of $R_{11}$ can be 12.6 kΩ. Then, the closed-loop gain of the amplifier is:

$$K = 1 + \frac{20.9 \text{ kΩ}}{12.6 \text{ kΩ}} = 2.6587$$

This gain reduces the Q value to only about 3. The passing band of the filter becomes wider and the amplification around the center frequency is a lot less. The filter performs poorly.

The output voltage $V_6$ of this filter is a sine wave with its peak-to-peak value of approximately 3.4 V when switch SW2 opens. The waveforms of this output under different conditions are in Figure 8. Note that when switch SW1 opens (condition #3), the peak-to-peak value of $V_6$ is approximately 30 mV. This is very insignificant in comparison to the desired 3.4 V and it does not have any impact on the performance of the remaining circuits. Thus, we can safely ignore this effect.

The analysis of the bottom low pass filter is similar to what we discussed above except that its center frequency is 1 kHz. The output $V_7$ of this filter is a sine wave with a peak-to-peak value of approximately 3.4 V when switch SW1 opens. The peak values of voltages $V_6$ and $V_7$ vary depending on the distance between the IR emitter and the phototransistor, and the alignment between these components.
D. The Absolute Value Circuits

The Absolute Value Circuits are used to double the operating frequencies of the signals to enhance the performance of the Peak Detector Circuits. This type of circuits is also called an Active Rectifier. Their schematic diagrams are in Figure 9 below. In the circuit, resistors $R_{17}$ through $R_{26}$ are equal in value. Let $R_{17} = R_{18} = \ldots = R_{26} = R$. Also in the analysis of these circuits, we focus on only one of them and use ideal diodes for the ease of establishing the equivalent circuits for different cycles of the input voltage.

Figure 9 – The Absolute Value Circuit
During the positive half cycle of the input voltage, diode D2 behaves as a short (use ideal diodes) and diode D3 acts as an open. The circuit becomes:

![Circuit Diagram]

**Figure 10 – Equivalent Circuit During Positive Half Cycle**

The first part of the circuit acts as an Inverting Amplifier with a unity gain. Thus, the voltage $V_X$ is:

$$V_X = -\frac{R_{19}}{R_{17}} \cdot \frac{V_6 + V_X + V_X}{12 \, \text{k}\Omega} = - \frac{R_{19}}{R_{17}} \cdot \frac{V_6}{12 \, \text{k}\Omega} = - \frac{V_6}{12 \, \text{k}\Omega}$$

The second part of the circuit behaves as a Summing Amplifier. The output of this amplifier is:

$$V_8 = -\frac{R_{27}}{R_{21}} \cdot \frac{V_6}{12 \, \text{k}\Omega} + -\frac{R_{27}}{R_{23}} \cdot \frac{V_X}{12 \, \text{k}\Omega} + -\frac{R_{27}}{R_{24}} \cdot \frac{V_X}{12 \, \text{k}\Omega}$$

$$V_8 = -\frac{R_{27}}{12 \, \text{k}\Omega} \cdot (V_6 + V_X + V_X) = -\frac{R_{27}}{12 \, \text{k}\Omega} \cdot (V_6 + V_X + V_X) = -\frac{R_{27}}{12 \, \text{k}\Omega} \cdot (V_6 - V_6 - V_6) = \frac{R_{27}}{12 \, \text{k}\Omega} \cdot (V_6)$$

The circuit amplifies the positive half cycle of the input voltage with a gain of $\left( \frac{R_{27}}{12 \, \text{k}\Omega} \right)$. 

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During the negative half cycle of the input voltage, diode D2 acts as an open and diode D3 behaves as a short. Figure 11 shows the equivalent circuit for this cycle.

![Equivalent Circuit During Negative Half Cycle](image)

The first part of the circuit behaves as an Inverting Amplifier with a gain of zero because the feedback resistor (from pin 6 to pin 2 of the 741) is a short. Thus, the voltage at \( V_Y \) is zero. It is also because \( V_Y \) is at virtual ground. This effectively removes \( R_{19} \), \( R_{23} \) and \( R_{24} \) from the circuit. Therefore, the second part of the circuit becomes another Inverting Amplifier and its output is:

\[
V_8 = - \frac{R_{27}}{R_{21}} V_6 = - \frac{R_{27}}{12 \, k\Omega} V_6
\]

Thus, the circuit inverts the negative half cycle of the input voltage and amplifies it with a gain of \( \frac{R_{27}}{12 \, k\Omega} \).

The potentiometers \( R_{27} \) and \( R_{28} \) are set to obtain full-wave rectified signals at \( V_8 \) and \( V_9 \) with their peak values of 8 V. The setting values of these potentiometers vary depending on the distance between the IR emitter and the phototransistor and the alignment between them. We can increase their values to obtain larger voltage gains for \( V_8 \) and \( V_9 \).
E. The Peak Detector Circuits

The Peak Detector circuits convert the full-wave rectified output signals from the Absolute Value Circuits into an “almost” DC signals. Figure 12 below shows the configuration of this circuit.

![Figure 12 – The Peak Detector Circuits](image)

The output voltages $V_{10}$ and $V_{11}$ have ripple voltages riding on a DC level.

When the RC time constant is much larger than the period of the wave, the conversion will take place. The larger the time constant, the smoother the output will be. However, if there is any change in the input voltage level, a very large time constant will result in a very slow response time. Thus, in the design, we must try not to go to either extreme of having a very smooth output or very quick response time. In the circuit, the time constants are:

$$\tau_1 = R_{31}C_{10} = (10 \, k\Omega)(2.2 \, \mu F) = 22 \, ms$$

$$\tau_2 = R_{32}C_{11} = (10 \, k\Omega)(10 \, \mu F) = 100 \, ms$$
The periods of the input signals are:

\[
T_1 = \frac{1}{f} = \frac{1}{8 \text{ kHz}} = 125 \mu\text{s}
\]

\[
T_2 = \frac{1}{f} = \frac{1}{2 \text{ kHz}} = 500 \mu\text{s}
\]

From the above calculations, the conversion from full-wave rectified signals into “almost” DC signals will take place. Diodes D6 and D7 prevent the discharging of the capacitors back to the outputs of the 741 operational amplifiers. Feedback resistors R29 and R30 are much larger than R31 and R32 ensuring that load resistors R31 and R32 would control the discharging of the capacitors.

The approximate DC currents are:

\[
I_{DC1} = I_{DC2} = \frac{8 \text{ V}}{10 \text{ k}\Omega} = 0.8 \text{ mA}
\]

The peak-to-peak values of the ripple voltages are:

\[
V_{RIPPLE1} = \frac{I_{DC1}}{fC_{10}} = \frac{0.8 \text{ mA}}{(8 \text{ kHz})(2.2 \mu\text{F})} = 0.05 \text{ V}
\]

\[
V_{RIPPLE2} = \frac{I_{DC2}}{fC_{11}} = \frac{0.8 \text{ mA}}{(2 \text{ kHz})(10 \mu\text{F})} = 0.04 \text{ V}
\]

Figure 12 shows the outputs of the circuits. These voltages have ripple voltages riding on a DC levels.

F. The Voltage Comparators and Transistor Drivers

Up to this point of the design, the output voltage \( V_{10} \) is a DC signal of about 8 V when the switch \( \text{SW}_2 \) opens. Otherwise, it stays at 0 V. The output voltage \( V_{11} \) is a DC signal of about 8 V when the switch \( \text{SW}_1 \) opens. Otherwise, it stays at 0 V. The Voltage Comparators are used to give an indication when either the switches opens. Figure 13 shows the schematic diagrams of the comparators and transistor drivers.
Let’s look at the top comparator and driver circuits. The Voltage Comparator utilizes the open-loop gain of the 741 operational amplifier. The voltage $V_{10}$ goes to the non-inverting input of the operational amplifier and a voltage divider is set up as a reference voltage at the inverting input. A 100 kΩ potentiometer $R_{33}$ is used for this purpose to adjust the reference voltage when necessary because in the design, the voltage $V_{10}$ (when switch SW2 opens) varies depending on the intensity of the IR emitter, the alignment and distance between the emitter and the phototransistor and ambient light.

When the reference voltage is more than the voltage $V_{10}$, the open-loop gain causes the comparator to produce a negative saturation voltage (about $-14.5$ V). When the reference voltage is less than the voltage $V_{10}$, the open-loop gain causes the comparator to produce a positive saturation voltage (about $+14.5$ V). In the design, we set the reference voltage to 4 V. Therefore, when switch SW2 opens, the voltage $V_{10}$ increases from 0 V to approximately 8 V resulting in a change from $-14.5$ V to $+14.5$ V of the voltage $V_{12}$. However, the transition from negative saturation to positive saturation of $V_{12}$ is not smooth as shown in its waveform in Figure 13. At the very moment when $V_{10}$ crosses the DC reference voltage, the ripple voltage causes a series of 8 kHz pulses. These pulses create false triggering for the digital circuits. We will eliminate these pulses in the transistor driver circuit.

Figure 13 – The Voltage Comparators and Transistor Drivers
The analysis of the transistor drivers is similar to the one discussed previously. The transistor drivers attenuate the output voltages $V_{12}$ and $V_{13}$ to TTL level, produce a falling edge for the monostable-multivibrator circuit, a LO TTL level to enable the count sequence for the counters and the latching circuit.

At the collector output of the driver, we connect a $10 \mu$F capacitor. This capacitor and the $1 \, k\Omega$ collector resistor (the output impedance of the driver) form a passive low pass filter. The cut-off frequency of this filter is:

$$f_0 = \frac{1}{2\pi R_{36} C_{12}} = \frac{1}{2\pi (1 \, k\Omega)(10 \, \mu F)} = 16 \, Hz$$

This filter effectively removes the $8 \, kHz$ pulses resulting in a TTL falling edge when switch SW$_2$ opens. The same situation occurs at the bottom driver when switch SW$_1$ opens. The waveforms of the output voltages of the drivers are in Figure 13.

G. The Latch and ac Driver Circuits

Up to this point of the design, we have a transition from 5 V to 0 V when one of the switches opens. This voltage returns to 5 V when we release the switch. The latch circuit allows us to maintain the desired voltage level. Figure 14 shows the schematic diagram of this circuit.

We use a D flip-flop with Active Low Preset and Clear inputs. When the input signal $V_{15}$ goes from HI to LO (switch SW$_1$ opens), the output $Q$ of the flip-flop goes HI and stays HI after the input $V_{15}$ goes back up HI (switch SW$_1$ closes). When the input signal $V_{14}$ goes from HI to LO (switch SW$_2$ opens), the output $Q$ of the flip-flop goes LO and stays LO after this input goes back up HI (switch SW$_2$ closes). Therefore, we latch the response of the openings of the switches. The output of the flip-flop is the controlled voltage to drive an ac load.

The ac-controlled device is a solid-state relay (RadioShack part # 275-310). This SSR requires a DC input voltage of 1.2 V and current of 15 mA. Since the maximum output current of the 7474 is only 8 mA, we use a transistor driver to provide appropriate controlled signal to the SSR. The operating principle and calculations for this driver are similar to the one discussed before.

In the design, when we press switch SW$_1$, the SSR is energized turning on the 40 W light bulb. Switch SW$_2$ de-energizes the SSR turning off the bulb.

Figure 15 shows the timing diagram of the flip-flop.
III. The Digital Part

The primary function of this part is to display the time the bulb being on. When we turn on the light bulb, the three-digit display resets itself to 0.00 and starting counting the on time.
Figure 16 below shows the schematic diagram of this part. It consists of an oscillator, a pulse generator, counters, decoders/drivers, and seven-segment displays. The oscillator provides the clock signal to the first counter and the Ripple Clock Output of this counter is the clock signal for the second counter and so on. The monostable-multivibrator provides a short pulse to reset the counters.

A. The Oscillator

A 555 Timer functions as an oscillator generating a 10 Hz TTL clock signal $V_{19}$ for the first 74190 counter. The design principle of this circuit is similar to the one discussed previously.

The clock frequency is:

$$f = \frac{1.44}{(R_{41} + 2R_{42})(C_{15})} = \frac{1.44}{[1 \text{ k}\Omega + 2(330 \text{ k}\Omega)](0.22 \mu\text{F})} = 9.9 \text{ Hz}$$

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The duty cycle of the clock signal is:

\[
\text{Duty Cycle} = \frac{R_{42} + R_{43}}{R_{42} + 2R_{43}} = \frac{1 \text{ kΩ} + 330 \text{ kΩ}}{1 \text{ kΩ} + 2(330 \text{ kΩ})} = 50.1\%
\]

B. The Monostable-Multivibrator (One Shot), Counter, Decoder/Driver Circuits

The output voltage \(V_{16}\) of the flip-flop triggers the 74121 One-Shot circuit. This circuit produces a single pulse \(V_{18}\) that loads the data (00.0) resetting the counters. The pulse width is:

\[
\text{Pulse Width} = 0.7 \times R_{40}C_{14} = 0.7(18 \text{ kΩ})(0.82 \mu\text{F}) = 10.33 \text{ ms}
\]

The voltage \(V_{17}\) enables the 74190 counters to count providing 4-bit outputs to the decoders. The 7446 (or 7447) decoders/drivers then drive the common-anode seven-segment displays. Figure 17 below shows a typical the timing diagram of the first counter. Its initial output is a decimal 3 or a binary 0011.

![Timing Diagram](image)

**Figure 16 – Timing Diagram**

Bibliography
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