

Integrated Circuits Design Course to Satisfy ABET Design Requirements in Electrical Engineering

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Abstract

Accreditation Board for Engineering and Technology (ABET) requires that electrical engineering graduates must be able to solve open ended theoretical problems and provide practical design engineering solutions for projects utilizing the knowledge they gained from the curriculum. The electrical engineering design curriculum is enhanced by offering the integrated circuit design course elective that provides real, practical, hands on experience in circuit design for the graduating seniors. Such projects can either be used as a stand alone cap-stone design or to assist the student to accomplish a multidisciplinary design projects in collaboration with other engineering disciplines.

Introduction

ABET program criteria for electrical engineering curriculum require that the curriculum must provide the depth and breadth across the range of engineering topics implied by the title of the program [1]. The acquired knowledge in the program should allow the student to analyze and design complex electrical circuits using appropriate CAD tools. The general criteria for basic level programs includes; students; program educational objectives; program outcome and assessments; professional component; faculty; facilities; institutional support; and program criteria ^[1]. In this paper we address the professional component in the electrical engineering program.

The professional component requires that the engineering graduate should be exposed and involved in a major and practical engineering accomplishment to facilitate his/her transition to practice in a real world engineering projects. The major design experience should utilize engineering standards and various constraints. These constraints include: economic, environmental, manufacturability, ethical, health, safety, social, and political issues directly related to the engineering project ^[1]. This paper recommends the course "Analysis and Design of Integrated Circuits" as a stand alone course to provide the students in electrical engineering the experience to analyze, design, use CAD, fabricate, and test a real world engineering design circuit. This is similar to what is known in the industry as application specific integrated circuits (ASIC). We shall briefly describe the course and what the students will experience and be able to accomplish.

Analysis and Design of Integrated Circuits

The analysis and design of integrated circuit course adequately addresses the major items required in the professional component for ABET criteria. This course has been around for a while, but it is not taught as a required course in some electrical engineering curriculums because of the time constraints to fabricate and test the design circuit. Theoretical skills learned in the curriculum, for example, mathematics, physics, and electrical engineering are fully and appropriately applied to satisfy the intended circuit specifications and demand. This involves the applications of the underlying physical concepts and proper choice of parameters, values of components, layout dimensions of the circuit, verifications of the circuit according to the design rules before fabrication, and proper performance to satisfy the design specification after fabrication.

The theoretical part of the course provides an introduction to the basic fundamental understanding of the operation of the electronic devices, mainly the metal oxide semiconductor field effect transistor (MOSFET). This device is widely used for theoretical and practical applications for analog and digital circuits. We have tailored the course to address design of digital circuits using complimentary MOS (CMOS) devices. However the course can be extended to include analog circuits. CMOS is a combination of an n-type and a p-type MOSFETs connected in series. Such CMOS connection produces the digital gate NOT or the inverter. The same idea can be extended to built all the fundamental logic gates, for example: NOR, NAND and XNOR using AND-OR-INVERT (AOI) or OR-AND-INVERT (OAI). All combinational or sequential circuits can be built from the bottom up using the basic logic gates.

The course is built and extended on the knowledge the student acquires in circuit analysis, an introductory course in device physics, and electronics. The theory for the metal oxide semiconductor field effect transistor (MOSFET) is covered in details. The current-voltage characteristics of the device are described, developed, and analyzed. The physical parameters that can change the characteristics of the device are discussed. For example the current in the linear and saturation regions are given by ^[2]:

$$I_D = \{u_n C_{ox}\} (W/L) [(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \quad (1)$$

$$I_D = \{u_n C_{ox}\} (W/L) [(V_{GS} - V_{TH})^2] \quad (2)$$

Equations (1) and (2) represent the current voltage characteristics for an nMOS in the linear and the saturation regions respectively. Where I_D , is the drain to source current, u_n is the mobility of electrons, C_{ox} is the silicon dioxide capacitance, W is the width of the device, L is the length of the channel, V_{GS} is the voltage between the gate and the source, V_{DS} is the voltage between the drain and the source, and V_{TH} is the threshold voltage of the device. A similar equation can be written for a pMOS except that the mobility of the holes is far less than the mobility of the electrons. The physical dimensions of the PMOS

can be changed to accommodate equal drain currents for both devices when connected in series.

This is the basic theoretical part of the course as an integrated circuit design. It demonstrates to the student how to change the characteristics of the device by changing the physical parameters of the device to suit the performance required. The MOSFET (n or p-type) is the building unit for CMOS. The CMOS is the building block for the fundamental logic gates. The fundamental logic gates are the building blocks for flip flops, half and full adders. The flip flops and the fundamental logic gates are the building blocks for shift register, and counters. Shift registers and counters can be used to build complex systems from the bottom up. The transmission gate, made up of a p-type and n-type MOS connected in parallel, is described and can be used to build sophisticated digital circuits as well.

VHDL or Verilog CAD for Design of Integrated Circuits

In general, design projects start from a concept or an idea. In order to realize or implement the idea, it should be described using a very high level description language (VHDL) ^[3]. This is called the behavioral model. It does not refer to any technology, fabrication process, device, or physical dimensions. VHDL is a powerful CAD tool that can be used to describe a complete system and facilitates the system simulation. If the result of the simulation or the performance satisfies the project needs, then a VHDL schematic or component level program will follow. Otherwise alternative behavioral descriptive VHDL programs or models can be suggested until a satisfactory model is accomplished. VHDL provides an opportunity to experiment with different design concepts than would otherwise be possible using a hardware testing facility ^[3]. For example, the following is an example of a VHDL program to describe the behavior for a NAND gate. This is for illustration purpose only and not necessarily the type of projects the students create in their projects:

```
library IEEE;
use IEEE.std_logic_1164.all;
entity AND is
port(x,y: in std_ulogic;
     z: out std_ulogic);
end entity NAND;
architecture behavioral of AND is
begin
    if (x=y=1 then
        z <= '0' after 5 ns;
    else
        z <= '1' after 5ns;
    end if;
end architecture behavioral;
```

The program does not indicate how the NAND gate is built and what technology or device will be used to realize it. It describes the behavior or the function of the NAND gate. Input voltage pulses can be placed to test the output voltage conformity to model prediction. Elaborate and sophisticated behavioral programs can be written for other more complex sub-systems or systems ^[4,5,6].

SPICE Text Program

SPICE text program is used to verify the expected performance of the inverter, NAND, NOR, XOR, at the device or component level. In SPICE the physical dimensions of the device can be changed at will [7]. For example the MOS channel length (L) or the width (W) provides a remarkable change in the output performance. Other parameter describing the model of the MOS in SPICE can also be changed as required.

The following is a SPICE text program that is very simple but powerful and is given here as an example for illustration purposes only. Programs written in SPICE for the basic logic gates can be used over and over again as a sub-program. These subprogram can be called to build sophisticated and complicated programs for flip flops, shift register, counters etc.

```
nand gate program
V1 1 0 5
M1 4 2 1 1 pm
M2 4 3 1 1 pm
M3 6 4 1 1 pm
M4 4 2 5 5 nm
M5 5 3 0 0 nm
M6 6 4 0 0 nm
.MODEL pm PMOS L=2U W = 8U
.MODEL nm NMOS L=2U W = 4U
V2 2 0 pulse(0 5 0 .1n .1n 1m 2 m)
V3 3 0 pulse(0 5 0 .1n ,1n 2m 4m)
.tran 0 8m 0.01m
.probe
end
```

Similar programs can be written for NOR, NOT, and XNOR.

Layout of the Designed Circuit

Once the circuit design performance is predicted by the description language (VHDL/Verilog), followed by a structural or schematic build up performance to meet the expected results using a SPICE program, the circuit is already to be transferred to a

layout for possible fabrication processes on a silicon chip. Processing of integrated circuit is covered briefly, in the course, to provide the students about the sequence of masks and various chemical processes that will be used to fabricate the integrated circuit.

The layout of the circuit requires knowledge about the design rules that govern the minimum dimension of each mask and the minimum separation between adjacent masks. LEDIT or similar CAD layout tools can be used to layout the circuit. The fundamental logic gates, for example, the NOT, AND, OR, XOR, and the transmission gate (TG) are laid out separately and stored in the library for future use. They are used to build any digital module, sub-system, or system.

A thorough verification of the layout should be made before sending the circuit for fabrication. In the course taught in the fall/2003, the projects made by students were not sent for fabrication. This is because of the time limits of the course to one semester. The second reason is we have used the student's version of LEDIT that does not allow fabrication. However, the same circuit can be copied to the complete version where it can be fabricated. One of the students who attended the course has an accepted abstract for his project, in this conference. He may present separately. A layout for a AND gate composed of a NAND and NOT is shown in Figure 1.

Testing and Verifications

The fabricated LEDIT layout must be tested for proper performance before and after fabrication on a silicon chip so that it should work as expected. LEDIT has a program to test for design rules errors in the layout. It also can give the parasitic resistors and capacitors created due to the layout. A new SPICE program should be written and simulated that includes the added parasitic components and how they affect the performance of the circuit. If the added parasitic components change the circuit performance, a new design or layout must be made otherwise the layout is ready for fabrication.

After fabrication the circuit must be tested one more time to meet the design specifications. This culminates the completion of an ASIC chip.

Summary and conclusion

This is one of few comprehensive elective courses that utilize all the knowledge the student gains in the curriculum to allow him/her to practice, solve, design, realize, fabricate, and test a real world engineering projects in electrical engineering. The course provides a theoretical solution for the prediction of the performance of a circuit. The performance can be manipulated using simulation tools at the behavioral level or structural level to satisfy the customer's needs and produces and tests a product for use by the consumer. This course satisfies ABET requirement for the professional component. Student can realize what the engineering profession can accomplish. The

projects made in this course can be used as stand alone capstone design project or to compliment it.

References

1. 2002-2003 Criteria for Accreditation, www.abet.org.
2. John P. Uyemure, Physical Design f CMOS Integrated Circuits Usin g LEDIT” PWS Publishing Company 1995. PSPICE User’s Guide, Cadnce PCB System Division, Portland, ORV97223
3. S. Yalamanchili, “Introductory VHDL From Simualtion to Sythesis”, Prentice Hall ISBN
4. E. H. Shaban,” Applications of CAD in Simulations of Laboratories for Electrical Engineering Education,” Intertech. 2000,University of Cincinnati, OH June 13-16, 2000.
5. E. H. Shaban,” Electrical Engineering Education in Underdeveloped and Developing Countries,” ASEE/Annual, June 10-13, 1999, Charlotte, NC.
6. E. H. Shaban,” Senior Design Logic Projects Using VHDL,” Proceedings ASEE/GSW, hosted by Le Torneau University, March 7-9, 1999, Dallas, TX.
7. PSPICE User’s Guide, Cadence PCB System Division, Portland, OR 97223.

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