AC 2010-947: INTERDISCIPLINARY LABORATORY PROJECTS INTEGRATING LABVIEW WITH VHDL MODELS IMPLEMENTED IN FPGA HARDWARE

Ronald Hayne, The Citadel

Ronald J. Hayne, PhD, is an Assistant Professor in the Department of Electrical and Computer Engineering at The Citadel. His professional areas of interest are digital systems and hardware description languages. He is a retired Army Colonel with experience in academics and Defense laboratories.

Mark McKinney, The Citadel

Mark H. McKinney, PhD, is an Associate Professor in the Department of Electrical and Computer Engineering at The Citadel. His professional areas of interest include power systems, measurement and instrumentation systems and engineering outreach and education.

Interdisciplinary Laboratory Projects Integrating LabVIEW with VHDL Models Implemented in FPGA Hardware

Abstract

Senior level electrical engineering elective courses often have a fairly narrow focus with little view of how the material from one EE discipline may integrate with another. Projects and in-class demonstrations encompassing material from multiple classes give students the opportunity to see how different concepts from within the EE curriculum integrate and allow them to observe the interactions from a larger perspective. Projects and demonstrations using computer aided design tools from different disciplines can be leveraged to exploit their strengths, while improving overall system design by interaction with other tools.

Prototype projects and in-class demonstrations have been developed that combine material from two senior electives: Advanced Digital Systems and Electrical Measurements and Instrumentation. The advanced digital course uses VHDL to model digital designs which can be simulated using ModelSim to verify their function. The electrical measurements course uses LabVIEW to develop computer-based instrumentation and measurement systems. The goal of these interdisciplinary projects is to develop systems that integrate a digital design modeled in VHDL with an instrumentation and test system built using LabVIEW. Due to the small student population overlap between the two classes, the projects are currently used as demonstration exercises with the ultimate goal being full integration in both courses.

The projects utilize LabVIEW's FPGA design module and Xilinx Spartan 3e FPGA boards to create a hardware-in-the-loop system that integrates concepts from both courses. VHDL models designed in the advanced digital class are implemented in FPGA hardware and integrated with a system designed in LabVIEW. LabVIEW's graphical programming environment allows for simple and straightforward testing and verification of the VHDL modules' designs.

One example project uses a VHDL model for a floating-point multiplier. This digital system uses the IEEE 754 single precision format with 32 bits representing a floating-point number. A significant challenge for testing this design is correctly formatting the test data. This is where LabVIEW can be leveraged to develop a test framework for the multiplier. The programming tools include type cast operators that readily convert floating-point numbers into their 32-bit single precision representations. These correctly formatted inputs and outputs are interfaced with the VHDL module to create a complete system that can be implemented and tested.

Concepts from these senior electives have been combined to develop projects and demonstrations that provide an integrated design and testing environment. Each discipline provides tools which contribute to the overall system. This interdisciplinary experience will better prepare students for the types of challenges they are likely to encounter as practicing engineers.

Introduction

The structure of many senior level electrical engineering elective courses often leads to a fairly narrow focus with little view of how the material from one electrical engineering discipline may integrate with another. Computer aided design tools are also often specific within each specialty and students usually learn to use numerous discrete tools with little or no integration between them. The goal of this research project was to create interdisciplinary design projects and in-class demonstrations that would give students the opportunity to witness the integration of concepts from disparate EE disciplines and begin to understand and appreciate the inter-relatedness of the many aspects of electrical engineering.

Two senior electives that use design projects to reinforce course concepts were chosen. Advanced Digital Systems uses VHDL to model digital designs, which are then simulated using ModelSim to verify their function. Electrical Measurements and Instrumentation uses LabVIEW to develop computer-based instrumentation and measurement systems. There was no prior interaction between these courses, but an opportunity existed to develop Field Programmable Gate Array (FPGA) systems integrating digital designs modeled in VHDL with LabVIEW-based test and instrumentation systems. Computer aided design tools from the different disciplines could then be leveraged to exploit their strengths, while improving overall system design by interaction with other tools.

Computer Aided Design Tools

The advanced digital course develops models of digital systems using VHDL. One method of testing these designs is via simulation using ModelSim.[1] A testbench can be created which provides input stimulus to the unit under test and then checks output signals for proper results. The input and output signals can be traced in a simulation window called a Wave, which resembles the output of a hardware logic analyzer. The simulation results provide functional verification that the VHDL model correctly implements the target design.

Another alternative to test the VHDL models is to implement them using FPGAs. The challenge then becomes instrumentation of the hardware to provide access to signals in real time. One method utilizes Xilinx ChipScope™ Pro to integrate test and measurement hardware components with the target design inside the FPGA.[2] The results are traced via an integrated logic analyzer very similar to the simulation output provided by ModelSim.

In the electrical measurements course, LabVIEW is used to develop computer-based instrumentation and measurement systems. The development environment uses a graphical programming language to create Virtual Instruments (VIs) to measure and interact with signals. Students can rapidly interface with measurement and control hardware and analyze data.

The opportunity to integrate designs from both courses using these computer tools comes from the LabVIEW FPGA Module and its support for Xilinx Spartan3e FPGA boards.[3] VHDL models designed in the advanced digital class are implemented in FPGA hardware and integrated with an instrumentation system designed in LabVIEW . This creates a hardware-in-the-loop system that can take advantage of the strengths of each design environment. Using LabView's

graphical programming tools, the students can easily interact with the FPGA hardware and readily test and verify the design of the VHDL modules.

A Simple Example

As a first prototype project, consider the simple example of converting a binary coded decimal (BCD) digit into the signals necessary to drive a seven-segment display. A digital clock displays time by turning on a combination of the segments on the display according to patterns shown in Figure 1. The digital design is easily modeled in VHDL as an entity defining the I/O interface and an architecture describing the functional relationship between the inputs and outputs, as shown in Figure 2.

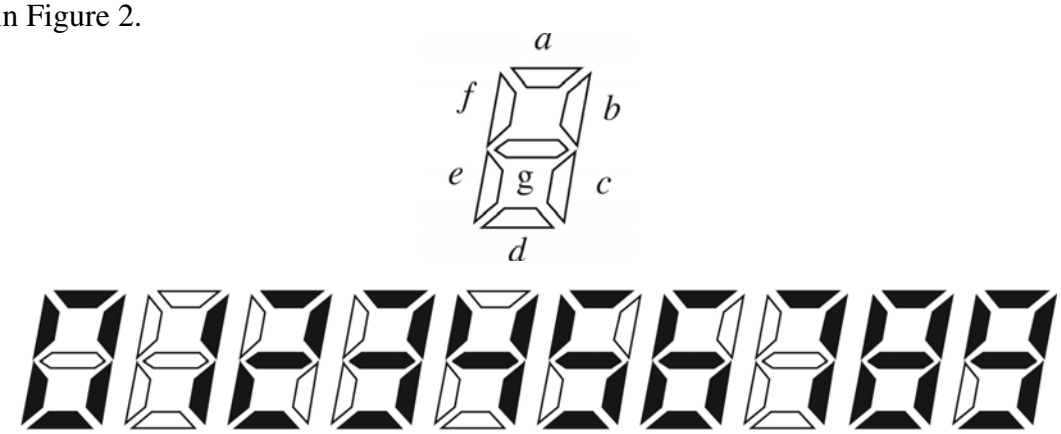

Figure 1. Seven-Segment Display.[4]

```
entity bcd_seven is
  port(bcd  : in  std_logic_vector(3 downto 0);
       seven: out std_logic_vector(6 downto 0));
                  -- MSB is segment g, LSB is segment a
end bcd_seven;

architecture behavioral of bcd_seven is
begin
  process(bcd)
  begin
    case bcd is
      when "0000" => seven <= "0111111";
      when "0001" => seven <= "0000110";
      when "0010" => seven <= "1011011";
      when "0011" => seven <= "1001111";
      when "0100" => seven <= "1100110";
      when "0101" => seven <= "1101101";
      when "0110" => seven <= "1111101";
      when "0111" => seven <= "0000111";
      when "1000" => seven <= "1111111";
      when "1001" => seven <= "1101111";
      when others => null;
    end case;
  end process;
end behavioral;
```

Figure 2. VHDL Behavioral Model.[4]

The design can be tested via simulation with ModelSim as shown in Figure 3. The resulting waveform does in fact provide functional verification of the design, but not in a readily discernable format. What is desired is a graphical representation of the segments, configured to match the layout provided in Figure 1. This is where the strengths of LabVIEW's graphical programming tools can be applied to provide an instrumented test environment for the VHDL model.

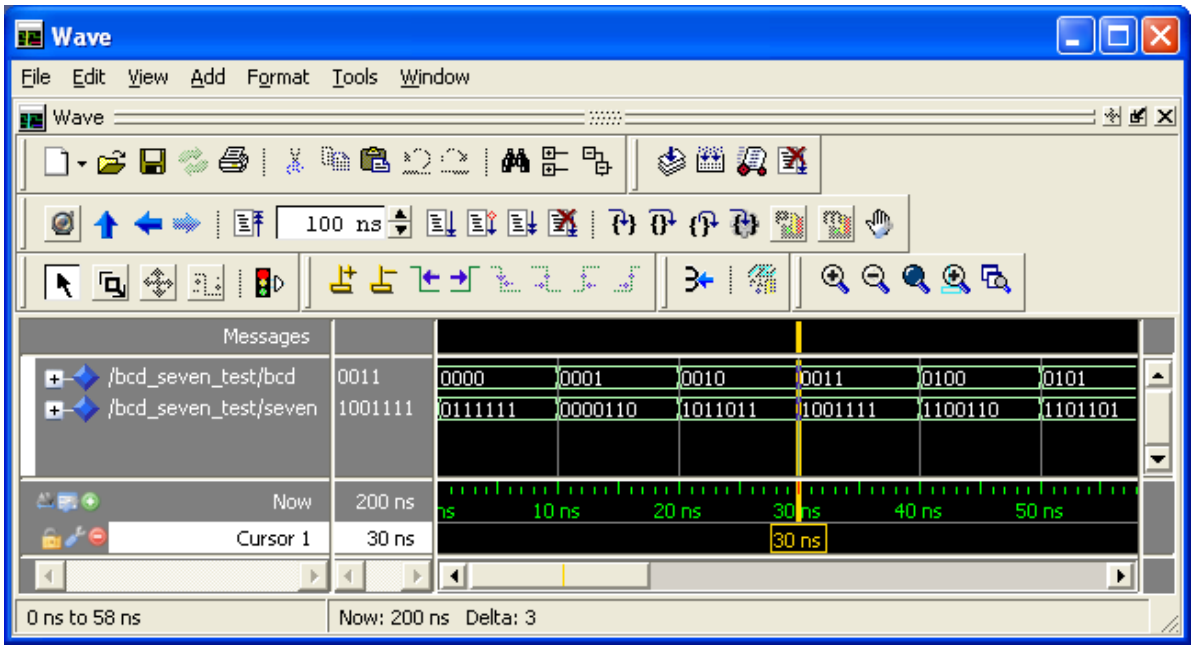

Figure 3. VHDL Simulation Waveform.

Using the LabVIEW FPGA Module, a VI can be created for the FPGA target. The HDLNODE shown in Figure 4 maps directly to the VHDL entity, specifying the inputs and outputs of the digital system. The variables *bcd* and *seven* are arrays of Boolean values representing the BCD digit and the output of the digital system, respectively. The existing VHDL model is also readily linked to the FPGA Target VI, which is compiled by the Xilinx ISE[5] software and loaded onto the FPGA.

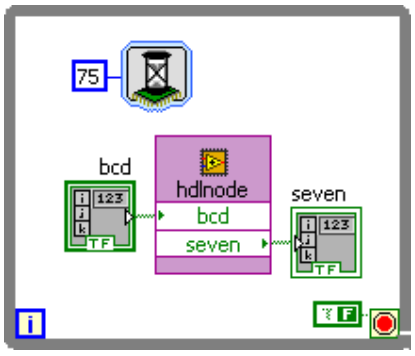

Figure 4. LabVIEW FPGA Module HDLNODE.

To complete the LabVIEW interface, a VI is created on the host computer to properly format the input BCD value and to translate signals generated by the FPGA into a format that can be displayed graphically on the front panel of the VI. The example Host VI is shown in Figure 5 and the front panel is shown in Figure 6. When the VI is run, it creates an interactive test environment that communicates with the FPGA target via the USB programming cable. Results are displayed in real-time on the graphical interface.

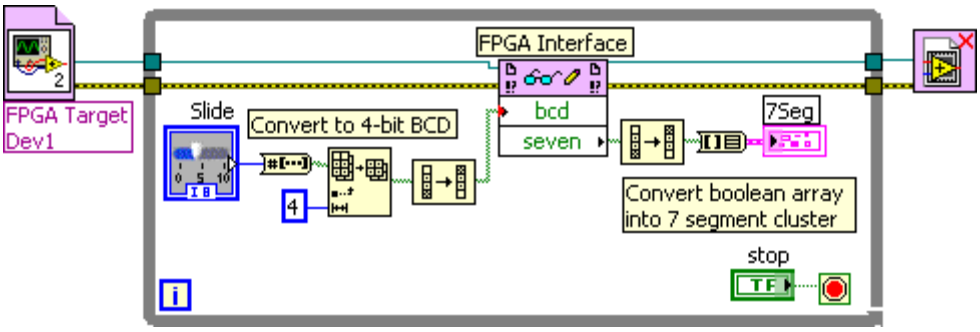

Figure 5. LabVIEW Host VI.

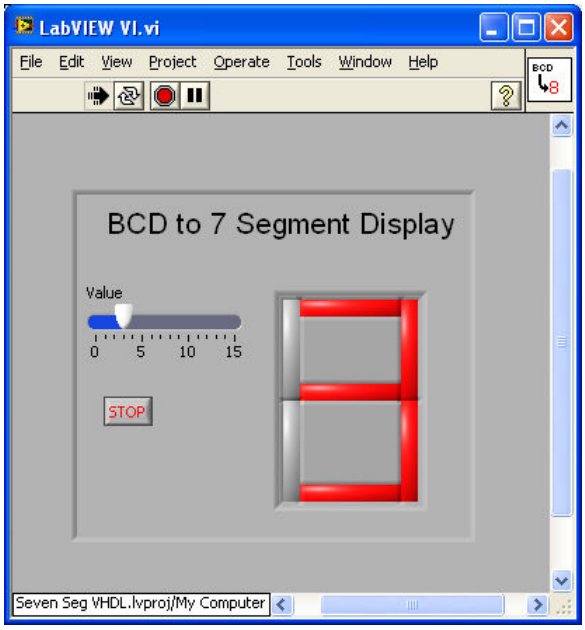

Figure 6. LabVIEW Host VI Front Panel.

Floating-Point Multiplier

Another example project implements a floating-point multiplier that uses the IEEE 754 single precision format. This is an existing design project in the advanced digital systems course which models a hardware multiplier with 32 bits representing each floating-point number. The sign, exponent and fraction bits are shown in Figure 7.

S	Exponent	Fraction
1 bit	8 bits	23 bits

Figure 7. IEEE Single Precision Floating-Point Format.[4]

A significant challenge for testing this design is correctly formatting the test data. For example, to represent the number 25.25_{10} the binary equivalent is $1.100101_2 \times 2^4$, which translates to S = 0, an excess-127 exponent of 10000011 and a fraction (without the leading 1) of 10010100000000000000000. The 32-bit number can be represented in hexadecimal as $41CA0000_{16}$. Testing the VHDL model using ModelSim results in a simulation waveform shown in Figure 8. In this example, two sets of numbers are to be multiplied together with all values represented in IEEE 754 format. Although not readily discernable, the simulation correctly displays the results of $25.25_{10} \times -2.5_{10} = -63.125_{10}$ and $-7.5_{10} \times -7.5_{10} = 56.25_{10}$.

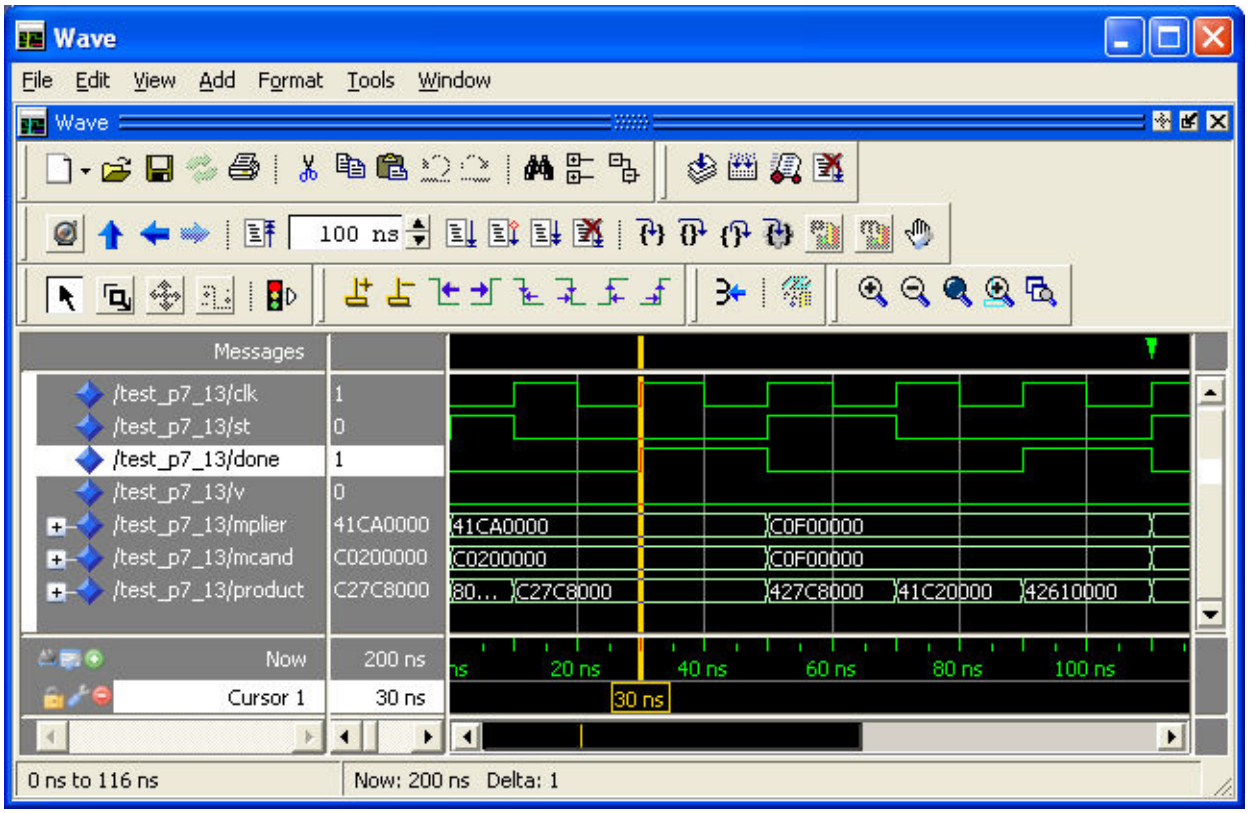

Figure 8. Floating-Point Multiplier Simulation Waveform.

The strength of the LabVIEW graphical programming environment can now be leveraged to develop a test and instrumentation framework for the multiplier. The VHDL model is again developed with an entity defining the I/O interface and a behavioral architecture describing the hardware multiplication algorithm. This VHDL model is similarly linked to the FPGA Target VI and loaded onto the Xilinx Spartan 3e board. LabVIEW is then used to develop a Host VI to create an interactive test environment.

Because LabVIEW uses the IEEE 754 format for internal storage of 32-bit single precision numbers, type cast operators are used to readily convert floating-point numbers into their 32-bit single precision representations. These correctly formatted inputs and outputs are interfaced with the VHDL module in the Host VI as shown in Figure 9. The complete VI includes a front panel which the can be used to input test values and observe the results in real-time as shown in Figure 10. The test interface now more readily shows the correct results of the multiplication 25.25_{10} x $-2.5_{10} = -63.125_{10}$.

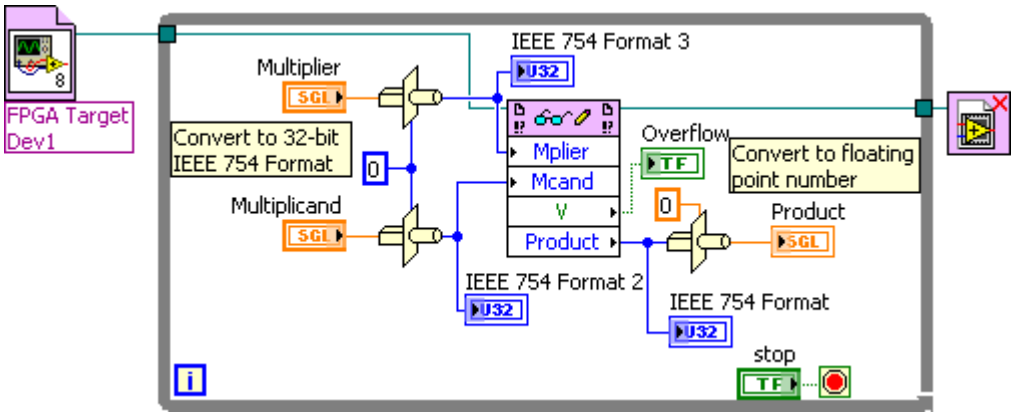

Figure 9. Floating-Point Multiplier Host VI.

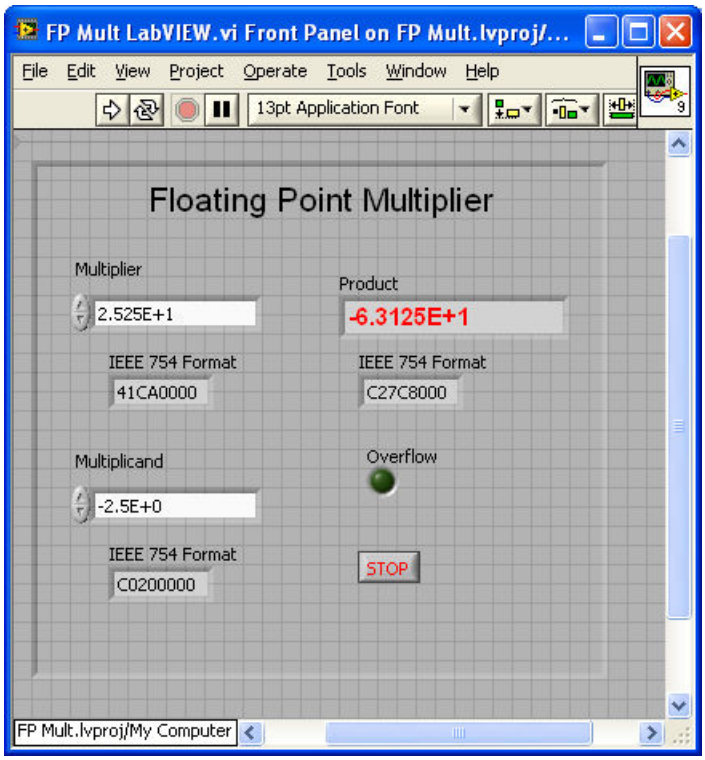

Figure 10. Floating-Point Multiplier Front Panel.

Results and Conclusions

The goal of these interdisciplinary projects is to provide the students with real examples of the importance of interdisciplinary systems in electrical engineering by developing systems that integrate a digital design modeled in VHDL with an instrumentation and test system built using LabVIEW. The projects described in this paper are currently being used in the Advanced Digital course as in-class demonstrations and the ultimate goal is to have them as integrated design projects in both classes. Currently, the small student overlap between the two electives makes this infeasible.

The projects utilize LabVIEW's FPGA design module and Xilinx Spartan 3e FPGA boards to create a hardware-in-the-loop system that integrates concepts from both courses. Computer aided design tools from different disciplines are leveraged to exploit their strengths, while improving overall system design by interaction with other tools. Using LabVIEW's graphical programming environment, students are able to interact with the FPGA hardware and readily test and verify the design of the VHDL modules.

Initial response to the in-class demonstrations has been positive and based on the success of the projects and student feedback, future directions may include adding FPGA projects designed via the LabVIEW programming environment. Comparisons could be made relative to the ease of the system design and the overall complexity of the FPGA hardware generated. There are many possible areas to explore the intersection of these two courses of instruction.

In summary, concepts from multiple senior electives have been combined to form projects that provide an integrated design and testing environment. Each discipline provides design tools which contribute to the overall system. This interdisciplinary experience will better prepare students for the types of engineering challenges they are likely to encounter as practicing engineers.

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