AC 2008-1119: INTRODUCTION OF ADVANCED CMOS DEVICE MODELS INTO THE CURRICULUM AT THE INTRODUCTORY ELECTRONICS LEVEL

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Introduction of advanced MOS device models into the curriculum at the introductory electronics level

Abstract

Most contemporary electronics design is accomplished in the CMOS technology and makes use of a design cycle that employs advanced MOS device models. These models accommodate many technologies, high-field effects, and second-order approximations and thereby must be deployed with a large parameter set. The models have a fairly high mathematics overhead. Consequently they are nearly impenetrable to the average student, even those with a relatively high level of expertise. In this respect it is almost unnecessary to do more with the models than the first-order treatments espoused by textbook reference and instead treat the subject of CMOS design in terms of a simulation methodology.

This paper identifies a set of simulation techniques and exercises that efficiently deploy this perspective. With the introductory electronics courses a set of simulation exercises have been developed which include the BSIM3V4 model, and identify effects in terms of the model simulation parameters, most of which can be associated with first-order physical roots. The process is simple and direct. In the classroom setting the effect of simulation at different CMOS levels is also appropriate and is deployed by these exercises, usually by collateral use of a spreadsheet utility and its graph/plot capabilities. The student version of Cadence/ORCAD/pSPICE, the most common classroom circuit simulation platform, is the principal operational utility, with the MS/Excel platform as a complementary spreadsheet utility.

I. Introduction

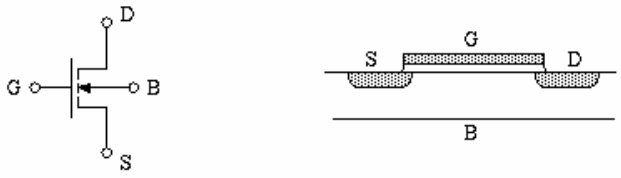
The Metal-Oxide-Semiconductor (MOS) transistor is the key component for most of the current electronics technology. Most of the integrated circuits that define our highly linked global environment system make use of complementary MOS transistors (CMOS) in order to achieve high-density circuits with both high-speed and a reduced power budget. These factors are also how we define much of our classroom dialogue in all forms of electrical and computer engineering.

Driven by demands for smaller, faster, and more extensive circuits, MOS device dimensions have been reduced to sub-micron levels [1]. At these sizes a few volts of potential produces extremely high electric fields, a factor that is both beneficial and problematic. The high fields are what enables the desired qualities of the MOS device. But the high fields also push the analyses well beyond most of the simple physics, which has its laws and roots in low-field laboratory benchwork. So classroom descriptions of the device physics for the MOS device need to accommodate both the familiar low-field analyses and the high-field facts of the technology.

For the instruction coverage of electronics the span of circuits and devices is already extremely crowded, and there truly is not enough time for either much device physics or much technology history. The simpler, low-field models of the MOS transistor are usually all that can be deployed.

But it is essential and necessary that even the most disinterested student be acquainted with the technology environment, and therefore a connection with more advanced device models, i.e. the BSIM3V4 model [2,3] need to be made. This is where the circuit simulation environment is of great benefit since it takes up most of the high mathematics overhead and allows the novice professional to see the concepts without either investment in the analytical overhead nor in the extensive set of second-order parameters reflected by the parameter sets for these advanced device models.

The simplest model of the MOS transistor is represented by figure 1.1, and identifies the essential operation of the device and minimum set of device parameters.



(a) 4-terminal schematic symbol (b) physical cross-section

Figure 1.1. MOS device cross-section and circuit symbol.

The device cross-section is the basis for the symbol and emphasizes that the device is a field-controlled transistor (field-effect transistor), since the conduction path between drain(D) and

source(S) is electrically isolated from the gate(G). The fact of the technology is emphasized by the circuit symbol and the requirement of a reasonably high gate field. The figure and the facts emphasize that this requirement can be accomplished at the low voltage levels of integrated circuits only if the gate is separated from the semiconductor substrate by a thin insulation layer, which, for the choice of silicon as substrate, is SiO_2, one of the best electrical insulators known. Since this oxide layer must be on the order of nanometers (10^{-9} m), the strong link to technology is immediate and recognizable.

The transistor action is also relatively simple and reasonably accurate for large MOS devices, as represented by figure 1-2, which illustrates the output characteristics as a plot of current vs voltage, and show that higher levels of gate voltage produce higher levels of current, and that the proportionality roughly follows a parabolic relationship. This lends itself to the textbook [4,5] models of the transistor, which are as far as we usually wish to reach for the first exposure of a young professional to the device physics.

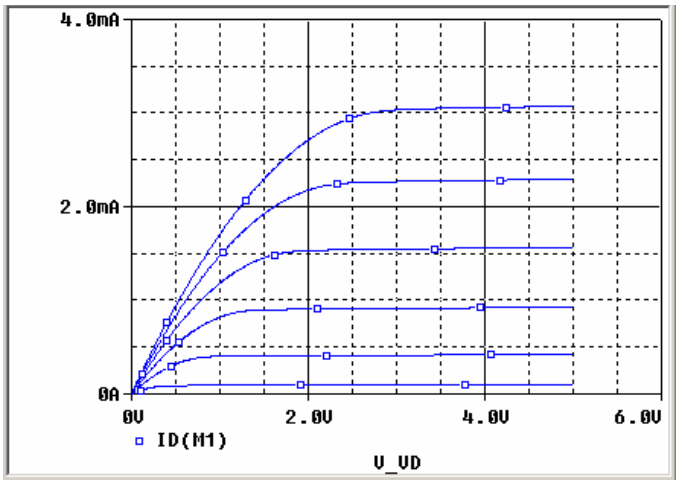


Figure 1-2: Output characteristics of the MOS transistor, level-1 model. In this example the gate voltage is stepped from 1.0 V to 4,0V in increments of 0.6V

The level-1 model [5] equations are:

$$I = \beta\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \qquad \text{for } V_{DS} < (V_{GS} - V_{TH}) \qquad \text{(1-1a)}$$

$$\text{and} \qquad I = \frac{1}{2}\beta(V_{GS} - V_{TH})^2 \qquad \text{for } V_{DS} > (V_{GS} - V_{TH}) \qquad \text{(1-1b)}$$

Where the subscripts *G,D,S* relate to the terminals of the transistor, as represented by device symbol and the technology cross-section of figure 1-1.

The equations visibly match the characteristics of figure 1-2 and also serve to introduce the fact of a threshold voltage (= V_{TH}) and a conduction coefficient = β. The conduction coefficient β is further expanded to acknowledge its simplicity in relationship to the transistor size factors of width (W) and length (L) as

$$\beta = \mu_0 C_{OX} \frac{W}{L} \qquad (1\text{-}2)$$

Where μ_0 is defined as the mobility of the charge carriers and C_{OX} is identified as the gate capacitance/area. The mobility concept brings the device physics element in closer focus, because it relates to the fact of charge flow in semiconductor materials. The gate capacitance C_{OX} emphasizes the facts of charge and field relationships on the conduction characteristics that are represented by figure 1-2.

Threshold voltage is also a critical concept, because it represents the essential ON/OFF factor of logic gates. In fact, for IC design, the threshold factor dominates much of the design philosophy. It is strongly dependent on second-order effects and usually finds itself backed up by a set of parametric equations [3], plus associated parameters.

The circuit electronics of logic circuits are an essential part the menu for the instruction sequence in electronics that incorporates MOS devices and is usually tied to the particular symbol set of logic synthesis, as represented by the primitive NAND and NOR logic gates of figure 1-3.

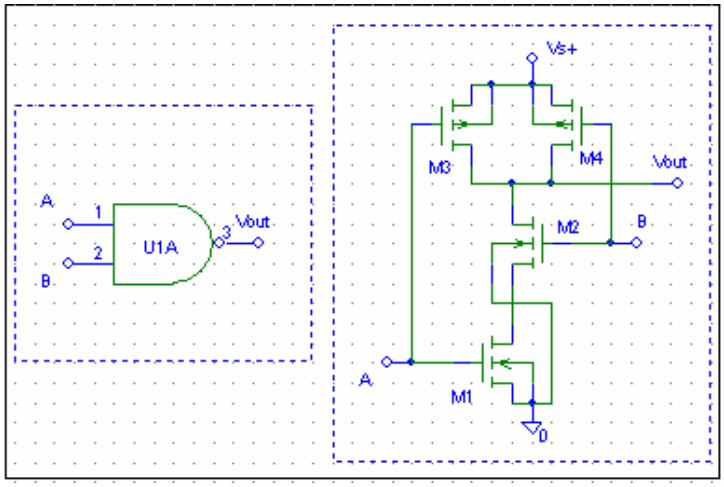


Figure 1-3a. Primitive logic gates and MOS transistors: CMOS NAND gate

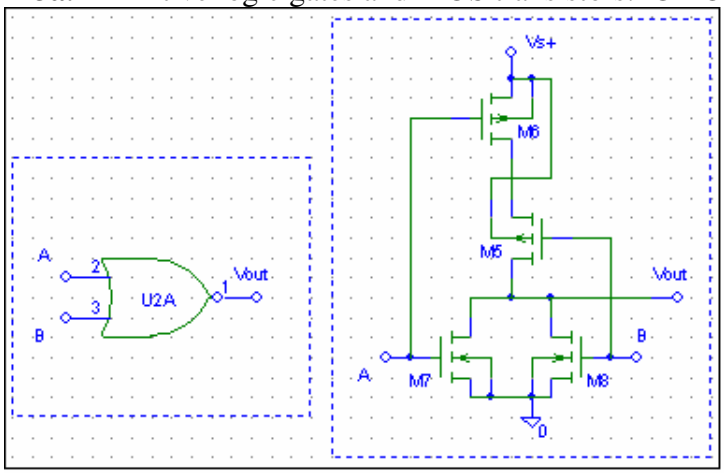


Figure 1-3b. Primitive logic gates and MOS transistors: CMOS NOR gate.

Other that the fact that these two logic gates are duals of one another, they omit the fact that there are functional limitations in performance. The logic gate format does not attempt to address anything other than the switch logic of the NAND and NOR (and other) logic gates. Logic design is a mostly a matter of identifying Boolean synthesis techniques and switch logic dynamics.

So it is incumbent on the electronics instruction to address the electrical facts and constraints of logic synthesis, at least at the foundation level. And therefore this makes it clear that the little switches, which, as represented by figure 1-3, are MOS transistors, and that their definition and performance is an embedded part of logic design. Much though we would like to assume that the Boolean logic is executed without fault, the electronics instruction is intended to provide exposure to reality, particularly when the effects of small-geometry and technology and it embedded high-fields are represented.

The subject area of electronics as an instructional metaphor also ties to the one of linear circuit theory. Linear circuit theory is used to introduce basic artifacts and techniques for which circuits are analyzed. It also identifies how electrical facts are predicted and extracted, whether by analytical means, simulation, or workbench experience. In this respect, the concept of a circuit function is usually that we have an input and an output and that the output is a function of an input. The output can be a logic function of one or more inputs, or it could be one of greater amplitude and power capability that that of the input. The 'amplifier' concept of electronic circuits was (historically) the first major application of electronics.

So the transfer nature of electronics is also part of the menu. With respect to MOS transistors this is represented most strongly by figure 1-4, which represents the simplest of the CMOS topologies, that of the 'CMOS inverter'. This circuit is usually used as a means to benchmark the technology; it is also used to benchmark the distinction between logic terminology and signal amplification, since the 'transfer curve' represents both.

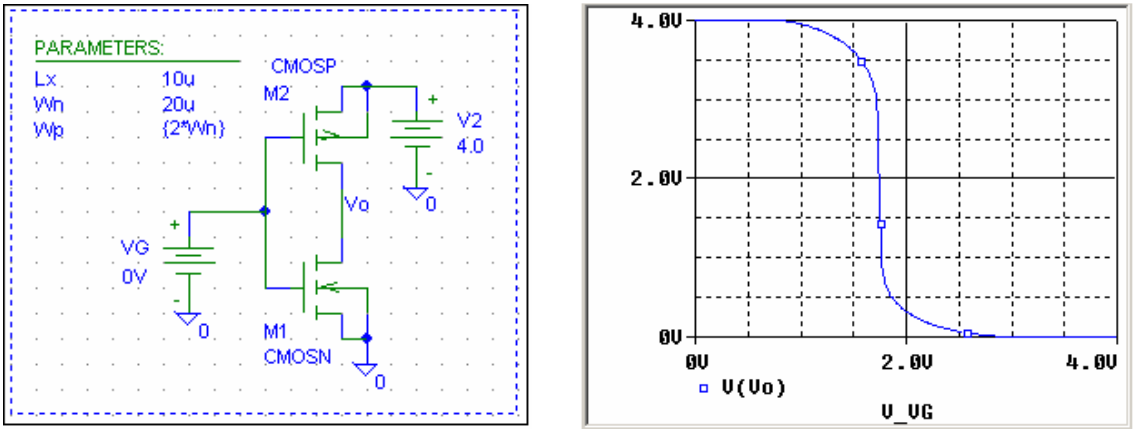


Figure 1-4(a), (b): CMOS inverter and transfer curve.

The high and low levels represent the logic states, for which the high level is usually defined as logic-1 and the low level is defined as logic-0. The transition region represents a logic fault. The CMOS action is one for which the upper transistor (in this case the pMOS device)

serves as a “pull-up” and then lower transistor (the nMOS device) serves as a “pull-down”. The logic context is then one for which the output node charges and discharges a capacitance, which makes the relationship between capacitance, current and speed more evident.

The transition region always includes a ‘transfer slope’. Since this slope is invariably large (negative) it implies the small increments on the horizontal scale (input) are transferred as larger increments on the vertical scale (output). This transfer amplitude gain is the basic concept of the signal amplifier, and represents the other side of electronics as an operational platform.. Amplifiers relate to the slope dynamics, and therefore usually demand much more analytical overhead. Whether or not we wish to invest in differential equations it is necessary but the mathematics is embedded mostly though the simplifications wrought by Laplace transforms. Laplace transforms are the environment we use to qualify circuit design and application in the frequency domain [6].

Since the MOS transistor is a non-linear device it is necessary that we have some of the basic mathematical description, as reflected by equation (1-1). We particularly need the analytical forms to define transfer concepts such as trans-resistance (name derivation of the transistor), which is usually expressed in terms of the transconductance, and defines much of the circuit facts and constructs in the amplifier or ‘analog electronics’ domain. The greater part of the instruction in electronics is directed toward analog electronics, since many applications relate to either signal conditioning or signal strength.

The electrical touchstone for both logic and analog electronics is therefore the transfer curve, and that points a simple and natural way to accommodate both the instructional needs and the technology evolution, since reasonably robust simulation platforms exist that have all of the necessary mathematics, device qualifications, and post-processors embedded within their little icons and constructs. It is usually a simple and direct process to use preprocessor artifacts to draw a circuit schematic and then let the schematic capture software pass the construct into the analytical domain. The most common platform for the classroom setting is the pSPICE software[7], which traditionally is available in evaluation copy form and is of sufficient versatility to address most small-circuit needs.

At the device physics level, equation (1-1) represents a device that is conceptually simple but does not exist. It is called the ‘level-1’ model. The ‘physical model’ is called level-2, and can be derived from semiconductor physics. The level-1 and level-2 models both have the same primitive form, which is that represented by equation (1-1), but level two identifies the effects of the transverse fields, which are the gate field that induces the conduction properties and the drain field that causes current to flow through the induced conducting channel.

The BSIM3V3 model [3] used to describe devices fabricated under the more advanced technologies is identified as level-49. The level number is an indication of how much effort has gone into characterization of the electrical properties of the MOS transistor. In part, models at this level exist because the high-field effects must be accommodated, whether or not the nature of the effects are well understood. But models at this level also exist because there is more than one approach to the explanation and exposition of the MOS transistor. And because of market forces, many of these models are not in the public domain.

II. Electronics and MOS devices

The electronics sequence and coverage for most college/university settings is one for which the lead semester is invested in basic circuit theory, which establishes most of the basics of circuits, and identifies the concept of a circuit as a graphic of nodes and branches. This semester is then followed by either one or two semesters in the subject area of electronics.

The distinction between linear circuits and linear electronics is fairly slight when approached in terms of ideal components. Ideal components are linear. Linear mathematics can be accomplished without too much mathematical trauma, and the semester is often as much a confidence semester as a discipline. A well-versed student in linear circuit theory has integrated the concepts of differential equations and circuits to the extent that he/she can visualize the circuit, not just in terms of a topology, but in terms of performance criteria.

Electronics is the part of the sequence for which the devices are non-linear. They are invested into the circuit graphic as branch elements, but the branches are linked by dependence relationships. These relationships break into the categories of operational levels and incremental signals, which is of the form of the logic vs analog interpretations of electronics.

But not quite. In the linear electronics world, the transistor circuits are treated in terms of an equilibrium state, known as the operating point. Incremental signals, usually identified as "small signals" are passed into the circuit for purpose of varying the (input) control node of the transistor and cause it to vary the level of output current.

So the natural framework of electronics has an analog signal processing orientation. The model of a circuit as an integrated context of transistors is therefore somewhat indistinct and the concept of a transistor as a single element embedded within a framework of resistances is very distinct. The transistor is treated as discrete devices, which is its evolutionary story but not likely to be its application context. The evolution of circuits into the semiconductor realm is embedded in the philosophy for which transistors were a replacement for vacuum tubes, which were a technology completely separate from those of the other components.

The MOS transistor is a component that is not actually found in single-transistor circuits. It is treated in the same context as its forbears, as if it were a transfer device biased into active-mode operation by a bias frame of resistances. But they are not discrete devices. In fact most MOS integrated circuits, to include those of analog persuasion, are constructs that are entirely MOS transistors. It is often a point of frustration to the novice instructor who expects that textbook components are available in discrete form and yet does not find any MOS catalog parts.

So the MOS transistor, in addition to being a device of some modeling complexity, is included in the philosophical stream almost entirely as a conceptual transistor, whose only true visibility is through its device models. So it almost seems to exist only in the framework of interesting integrated circuit layout geometries and somewhat impenetrable device models.

Fortunately, the reality of MOS as a classroom circuit element is reconditioned by the connection between the university community and the rapid-prototyping environment. In this respect an operating environment for which a low-cost multi-project fabrication context was developed through a DARPA (defense advance research projects agency) program that involved several universities and defense-related industries. The program, even though it is now more commercialized, goes by the name MOSIS (MOS Information Systems) fabrication services.

The MOSIS fabrication service is still strongly committed to university and educational support. Of particular significance to the educational context, the MOSIS service generates BSIM3V4 parameters for each fabrication run. Test devices for any one of several 'foundry' sources are the basis of these parameters and give the educational arena a very real connection with both the behavioral and the performance characteristics of the MOS devices in some very advance technologies. An example of the BSIM3V4 parameters, in the case for an nMOS device fabricated under a 0.5um process is shown by figure 2-1.

```
.MODEL CMOSN NMOS (                                 LEVEL   = 49
+VERSION = 3.1           TNOM    = 27               TOX     = 1.4E-8
+XJ      = 1.5E-7        NCH     = 1.7E17           VTH0    = 0.6530764
+K1      = 0.9088687     K2      = -0.1076085       K3      = 24.6853298
+K3B     = -8.1580591    W0      = 1E-8             NLX     = 1E-9
+DVT0W   = 0             DVT1W   = 0                DVT2W   = 0
+DVT0    = 3.7212749     DVT1    = 0.4323985        DVT2    = -0.0907965
+U0      = 453.8468529   UA      = 1E-13            UB      = 1.47429E-18
+UC      = 1.091073E-11  VSAT    = 1.696709E5       A0      = 0.5875444
+AGS     = 0.1309601     B0      = 2.471913E-6      B1      = 5E-6
+KETA    = -1.335088E-3  A1      = 2.583854E-5      A2      = 0.3465284
+RDSW    = 1.339926E3    PRWG    = 0.059421         PRWB    = 0.0440407
+WR      = 1             WINT    = 2.512406E-7      LINT    = 3.272367E-8
+XL      = 0             XW      = 0                DWG     = -1.020893E-8
+DWB     = 4.692871E-8   VOFF    = 0                NFACTOR = 0.8333572
+CIT     = 0             CDSC    = 2.4E-4           CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0325938        ETAB    = -9.58539E-4
+DSUB    = 0.2852215     PCLM    = 2.6257947        PDIBLC1 = -0.1069022
+PDIBLC2 = 2.464134E-3   PDIBLCB = -0.0822411       DROUT   = 0.4899918
+PSCBE1  = 5.796075E8    PSCBE2  = 8.004341E-5      PVAG    = 0
+DELTA   = 0.01          RSH     = 81.8             MOBMOD  = 1
+PRT     = 0             UTE     = -1.5             KT1     = -0.11
+KT1L    = 0             KT2     = 0.022            UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11         AT      = 3.3E4
+WL      = 0             WLN     = 1                WW      = 0
+WWN     = 1             WWL     = 0                LL      = 0
+LLN     = 1             LW      = 0                LWN     = 1
+LWL     = 0             CAPMOD  = 2                XPART   = 0.5
+CGDO    = 2.16E-10      CGSO    = 2.16E-10         CGBO    = 1E-9
+CJ      = 4.191468E-4   PB      = 0.99             MJ      = 0.4421449
+CJSW    = 3.240521E-10  PBSW    = 0.1              MJSW    = 0.1159188
+CJSWG   = 1.64E-10      PBSWG   = 0.1              MJSWG   = 0.1159188
+CF      = 0             PVTH0   = 0.0858702        PRDSW   = 141.0812323
+PK2     = -0.0336284    WKETA   = -0.0316284       LKETA   = 3.128335E-3    )
*
```

Figure 2-1. BSIM3V4 parameters for MOSIS run T1AW.

This parameter set can be imported directly into the circuit simulation environment cited (pSPICE), since it includes advanced MOS device models in its operating platform. As might be expected, the device model level is also a keyword that defines the rest of the usage of the parameter, and in this case invoking the model formulations that are collateral to this set of parameters.

Under this set of parameters there are some reasonably obvious connections to the embedded device physics. For example the parameter VTHO is the (extracted) zero-bias threshold

voltage, as might be appropriate for citation in its simplest context by equation (1-1). The parameter TOX is the thickness of the gate oxide from which C_{OX} can readily be defined as well as the gate capacitances. The parameter U0 is of special interest since it is the zero field surface mobility, and is measured from the characteristics of a large device consistent with one for which the level-2 parameters are valid. The parameter K1 is the first-order body-effect parameter and will relate to threshold shifts due to back-bias on the gate.

It should also be evident that there are an extensive number of effects covered by the parameter listings of figure 2-1 which can be exposed by little more than a simulation of single devices. The evidence points the novice professional to the device physics without the necessity of a heavy investment in the physics overhead, and does so adequately to address the circuit electronics. The simulations then become the key to the device physics as a buried formulation, unencumbered by the somewhat idealistic theorems and assumptions of semiconductor physics.

III. Insertion and Exposition

If the intention of the simulation platform is strictly the device physics, then a relatively simple construct, such as that represented by figure 3-1, is possible and practical, for which a single device is examined in terms of the effect of the gate length. In this context it is good for the appreciation of the field effects in these small devices but is not directed to the context of the MOS component as a circuit element. Electronics is definitively oriented toward the application of devices to circuits, usually as a transfer device but also in the context of loads and references. So it is probably more worthwhile to let the circuit context expose the effect of the device and its embedded fields.

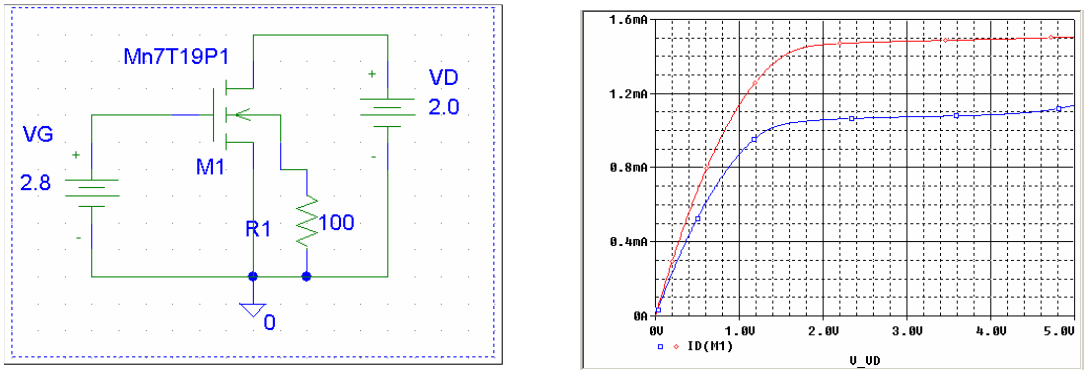


Figure 3-1(a),(b): Simple single nMOS device simulations. The drain characteristics are represented. The upper trace is the level-2 model and the lower trace is the level-49 model.

Comparison modes of the effect of the device physics are relatively simple if it is assumed that the level-49 (BSIM3V3) is designed to be extensive with respect to device size and with respect to technology options. If the devices are cast as large transistors, the device model essentially collapses to that of level-2, for which only first-order effects will play a role.

One of the more important logic circuits is a good example, as represented by figure 3-2. In this case, the CMOS 'Schmitt trigger' (also known as a 'tickle-thump' circuit) is used to shape degraded logic signals by using two circuits in parallel, one of which holds the circuit in its logic state beyond its normal transition (hysteresis), so that when it is released, the pull of the complementary transistor is much stronger and more decisive than it would be for a simple inverter of the type represented by figure 1-4a. The effect is that the logic signal at the output is squared off much more effectively and thereby is much less prone to logic faults or to timing problems.

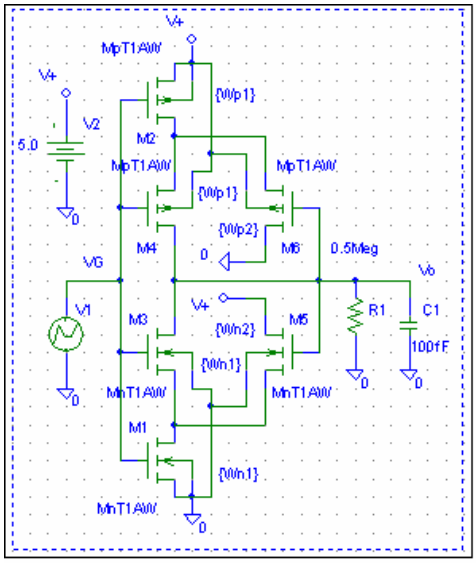


Figure 3-2a: CMOS Schmitt-trigger circuit.

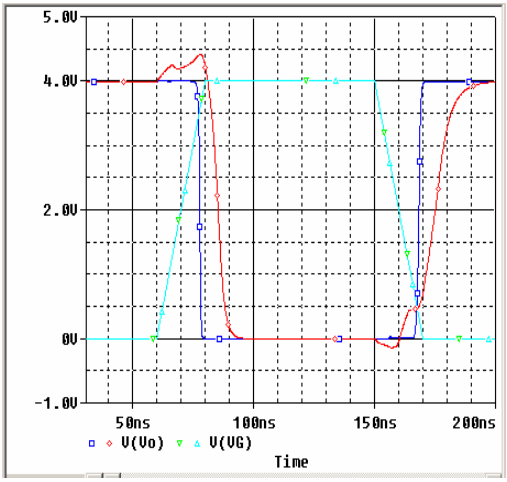


Figure 3-2b: Output of CMOS Schmitt trigger overlaid against an artificially degraded input pulse. Outputs for level-2 and level-49 behavior are compared.

In the analog integrated circuit domain there are many circuit candidates of interest, but the one that is most appropriate to the undergraduate instruction is that represented by the CMOS common-source construct, as represented by figure 3-3, for which an nMOS transistor is used to drive a pMOS active load. In this respect both the concept of active load and amplification are well represented. So the circuit is more than just an exposition into the device physics. It is also a circuit for which the transistor count is sufficiently low so that two copies, each with different device characteristics or feature sizes, can be run concurrently in the mildly constrained environment (10-transistor limit) of the evaluation copy of pSPICE.

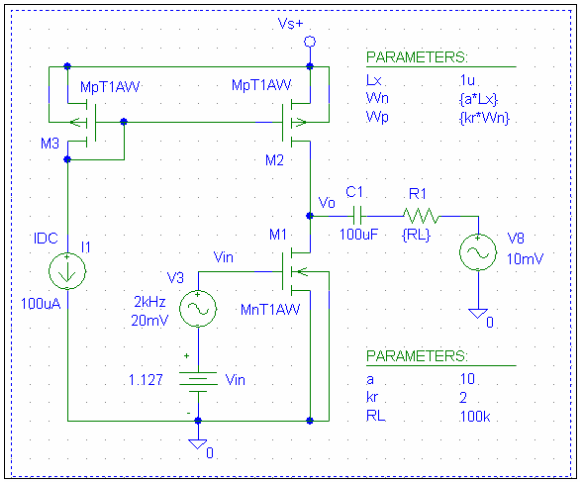


Figure 3-3a: CMOS common-source topology with active load

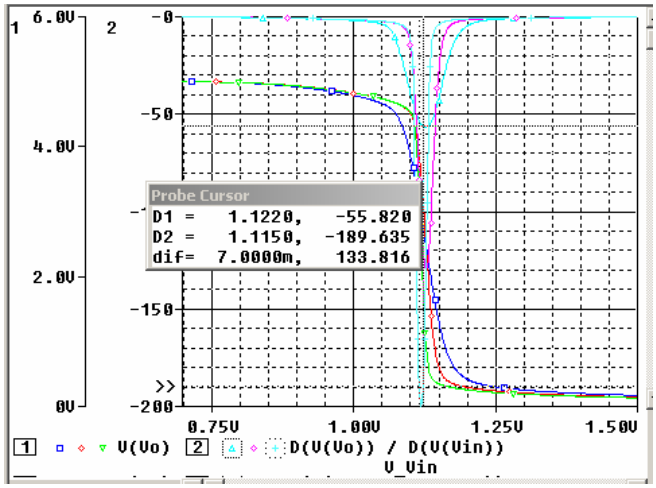


Figure 3-3b: Transfer curve for figure 3-3a overlaid with the derivative. The device sizes are stepped through a progression of transistor dimensions by the parametric option of pSPICE, for which all devices have the same W/L ratio but exhibit considerably different field effects do to the consequences of technology. The higher transfer gain (shown as =189.6 V/V) is for the larger transistors, consistent with the level-2 device model.

Although there are probably many options of circuits and effects thereto, the circuit simulator also allows considerable exposition at the charge/capacitance level, as illustrated by figure 3-4a, the simple CMOS inverter. In this case the performance analysis feature of pSPICE and a sampling artifact [8] are used to examine the effect of voltage on output capacitance. Since output capacitances for the MOS transistor are a brew that depends on the junctions it is also essential that junction areas and perimeters be defined for each of the transistors, which invites the novice professional to take a look at figure 1-1 and the meaning of the MOS transistor in terms of its embedded *pn* junctions.

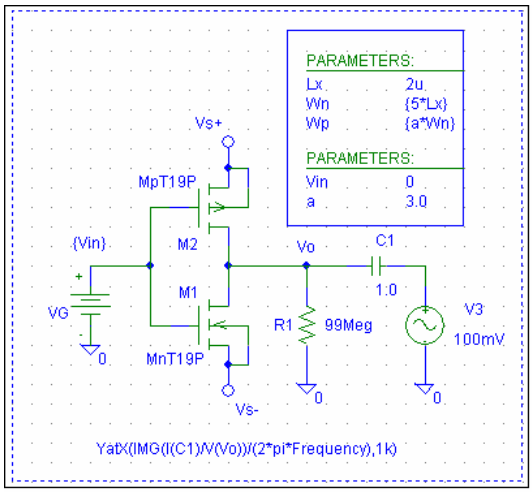


Figure 4-1a: CMOS inverter construct with probe source at the output for the assessment of device drain capacitances.

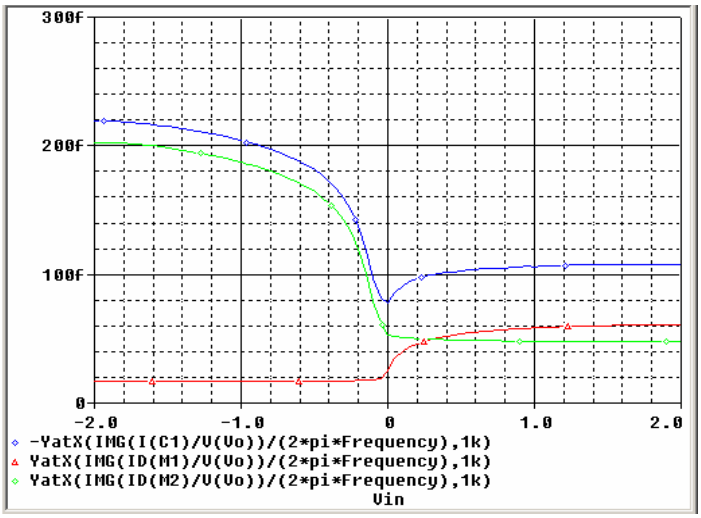


Figure 4-1b: MOS junction capacitances at the output as a function of input voltage. The uppermost trace is the sum of the lower two traces. The lower traces are the drain junction capacitances of the nMOS and pMOS transistors, respectively.

It is sufficient to note that these are junction capacitances and consequently are voltage dependent. The circuit simulation under the advanced MOS device model is a simple and direct exposition thereto. In this case it shows that the pull-up transistor (pMOS) dominates the output capacitance. The simulation also shows that the output capacitance minimum is at Vin = 0, a fact which would take considerably more investment to show otherwise. The example shows how to use the simulation environment to cut to the chase in the assessment of complex circuit electrical characteristics.

IV: Summary and conclusions

The use of the circuit simulation artifact is a tool of considerable benefit in the exposition of high-field effects of advanced technologies without the overhead of the accompanying device physics. The examples reflect an approach and post-processor options that invite novice professionals to explore the MOS technology evolution through the use of models that are equal to the task. Since the higher-level models are well supported by both the simulation platforms and the MOSIS fabrication service, the options are not just another instructional exercise but a true visit to state-of-the-art MOS technologies.

The use of higher-order models does not imply any extra overhead in the normal course of electronics instruction. In fact it may slightly reduce the load, since the software platform is as effective offline as it is within the classroom setting. Except for the simple expositions for which the MOS device characteristics representations within different device models are compared, all of the exercises represented were directed assignments that were used to acknowledge the role of technology in CMOS logic and CMOS analog circuits. The exercises also served as an example of the simulation factor in the integrated circuit design cycle, since they relate directly to ongoing MOS foundry runs.

At MSU the MOS device course is a specialty course that is directed toward the microelectronics option of the ECE (Electrical and Computer engineering) curriculum. The techniques and simulation algorithms described by this paper were developed in the fall semester of 2003 and the next time that the course was deployed (due to enrollments) was the fall semester of 2007. The effect of having the approach identified by this paper was that it extended the reach of the topic material and allowed the addition of a coverage of the subthreshold behavior of the MOSFET, a topic that is normally beyond reach of the normal undergraduate class. And it has also yielded entirely new set of simulation algorithms for the exposition of the MOS device physics.

Inasmuch as the circuits-electronics sequence is fundamental to most of the art of electrical engineering, it is essential that it make both an efficient coverage and state-of-the-art exposition of the technology. The integration of circuit simulation at advanced model levels is a very natural approach, minimizes overhead, and realizes a clean exposition by virtue of the flexible and extensible post-processor options that have been developed along with the technology evolution. This presentation has represented the simulator role without prescribing any boundaries, but also recognizes that much of what is hidden by this descriptive approach is of value and interest in the device physics community.

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