AC 2011-1222: INTRODUCTION OF SEMICONDUCTOR TEST ENGINEERING INTO THE BSEE CURRICULUM

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Introduction of Semiconductor Test Engineering into the BSEE Curriculum

Abstract

Semiconductor testing is an essential part of the manufacturing process, especially as integrated circuit (IC) designs become more complex and time to market pressures increase. However, relatively few universities have courses dedicated to training students to be competent IC test engineers. Through a partnership with SPEA, a major supplier of automated test equipment (ATE), the University of Texas at Tyler has initiated a three year plan to integrate practical laboratories in semiconductor testing at all levels of the BSEE curriculum. Past approaches have traditionally implemented a single technical elective in the senior year. The proposed approach is unique in this regard as the conjecture is that introducing laboratories in semiconductor test across the curriculum is more effective. An outline of this plan and its rationale along with expected program outcomes are described in this paper. The experience in the first year of this plan, including design of the interface electronics, implementation of the first two laboratory projects, and interactions with applications engineers, are also discussed.

Introduction

As an increasing number of transistors continue to be fabricated on a single integrated circuit (IC) and more complex functionality is designed into each chip, more efficient test methods are needed. Semiconductor testing is necessary to ensure that a processing defect has not impaired the functionality of a chip and that the design meets the required performance specifications. Both IC designers and test engineers who are well-versed in semiconductor test theory and practices are required to ensure the successful completion of a VLSI chip. For example, it is noted in a recent textbook on VLSI design that it is imperative for the IC designers and test engineers to collaborate on a test plan early in the chip design process to ensure all possible test contingencies are considered – to do otherwise is to guarantee failure.¹ And once the chip design is completed, the test engineer is responsible for implementing an efficient and thorough test plan that ensures the customer receives fully-functioning ICs. The test engineer’s task becomes even more challenging as ICs are implemented in nanoscale technologies due to the host of reliability issues that begin to arise.²

Despite the critical importance of the test engineer, relatively few universities have introduced semiconductor testing into their curriculum. Most test engineers report learning their craft through other means, such as on the job training from co-workers to even trial and error.³ It has been estimated that about six months of training is typically required to bring a new hire up to speed using sophisticated semiconductor test equipment.⁴ A recent survey of leaders from the semiconductor industry underscores the desire for more universities to introduce material into their curriculum that more closely reflects the practices of industry, such as test program development.⁵

This paper will discuss the partnership between The University of Texas at Tyler and SPEA America to introduce test engineering into the BSEE curriculum. SPEA is a major manufacturer of advanced automated test equipment (ATE) and has donated to our institution a high performance
The C340MX semiconductor tester (see Figure 1) along with a three-year grant to support the curriculum development. The faculty and two graduate students are working closely in a team with SPEA’s application engineers to develop the required hardware (interface electronics and load board), test scripts, and laboratory material. In particular, the SPEA engineers have been quite helpful in suggesting tests that reflect real world test scenarios.

Figure 1. A student working on the SPEA semiconductor tester

The proposed approach is to integrate test engineering at all levels of the curriculum instead of just one senior-level class. In the lower level classes, the students will be introduced to simple tests. For example, in a freshman class that introduces the students to the electrical engineering profession, a lab that uses the tester to measure the value of a resistor is planned. A course in digital logic design in the second year will have the students using the tester to perform a parametric test on a logic gate to verify that the logic levels are correct. When students are introduced to opamps in their third year electronics classes, they will use the tester to characterize a commercial opamp IC. A senior level elective is planned to give those students interested in test engineering a more comprehensive learning experience with the ATE tester. The rationale behind this graduated approach is to introduce the students as soon as possible to real world test examples so that they can immediately bridge the gap between academic learning and practical applications from industry. This should reinforce the material learned in lectures and motivate the students as they realize what they are learning has direct relevance in industry.

The outline of this paper is as follows. First, a brief survey of existing approaches for introducing test engineering into a BSEE program is given, followed by an overview of the plans for integrating test engineering into the curriculum. A detailed discussion of the plans will include
the rationale for the integrative approach, along with the pros and cons, and expected student 
learning outcomes. The progress to date and outline of this three year plan will be given. This 
will include some preliminary observations from the past two semesters. A concluding summary 
will outline future work.

**Survey of Existing Approaches**

Of the few institutions integrating test engineering into the university curriculum, most 
implement it as one or two courses at the senior level. A key challenge facing educational 
institutions is providing students with hands-on experience using an industrial-level 
semiconductor tester due to the prohibitive costs of purchasing such equipment. A couple of 
alternatives include the use of virtual instruments and shared access to a tester kept at a central 
location. While a virtual ATE can provide a useful hands-on learning experience, the drawback 
is that the students do not learn the actual test programming and issues related to working with a 
real ATE tester. Remote access to a shared ATE machine does provide students with access to an 
industrial-level tester, but students do report some frustration on not being able to have direct 
physical contact with the tester. Hence, some level of collaboration with an industry partner is 
necessary for most institutions to provide access to a quality semiconductor tester. Texas A&M 
University is one successful example of a college-industry collaboration that is able to provide 
their students with training on an advanced Teradyne semiconductor tester. Their program has 
two required courses in semiconductor test at the junior and senior year. It is their program that 
was examined carefully in developing the proposed plan. This proposed approach appears to be 
unique in introducing semiconductor testing throughout the BSEE curriculum, as described next.

**Integrating Semiconductor Testing into the BSEE Curriculum**

Instead of developing one or two courses that concentrates solely on semiconductor testing, we 
decided to integrate test engineering into all levels of the curriculum. We reviewed the labs used 
by Texas A&M for their Mixed-Signal Test courses and evaluated the classes in our own 
curriculum for possible integration. The proposed plan for distributing the test labs within the 
first three years of the curriculum is outlined in the table below.

<table>
<thead>
<tr>
<th>Time</th>
<th>Course</th>
<th>Tester Lab</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st Yr</td>
<td>Engineering the Future – Intro to Electrical Engineering</td>
<td>Resistor – measure resistance (Kelvin and non-Kelvin)</td>
</tr>
<tr>
<td>2nd Yr</td>
<td>Digital Systems</td>
<td>Logic Gate – logic voltage levels</td>
</tr>
<tr>
<td>2nd Yr</td>
<td>Linear Circuits I</td>
<td>Capacitor – measure capacitance</td>
</tr>
<tr>
<td>3rd Yr</td>
<td>Linear Circuits II</td>
<td>Opamp Characterization</td>
</tr>
<tr>
<td></td>
<td>Electronics I</td>
<td>FET Characterization</td>
</tr>
<tr>
<td>3rd Yr</td>
<td>Signals and Systems Microprocessors</td>
<td>DAC Characterization</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Counter – functional test</td>
</tr>
</tbody>
</table>
The rationale for this approach is threefold. First, this will help with student motivation and retention, as the students see the immediate relevance of theory and its application in industry. Hence, we plan to introduce the first test laboratory in our Engineering the Future class, which introduces incoming students to the scope of work performed by electrical engineers. The course content includes a basic introduction to linear circuits (Ohm’s law), so that a lab that gives an overview of the ATE tester and allows them to see how resistance is measured with the tester is appropriate. An aim of this course is to give the students as much interesting hands-on experiences as possible to encourage them to see that the dynamic and challenging work performed by electrical engineers. The introduction of the semiconductor tester into this class should help with this course goal. Second, this will more closely align the theory learned in classes with its application to the semiconductor testing issues. Thus, the students can immediately bridge the gap between academic learning and practical applications from industry. While Hudson and Copeland note that the elective class in semiconductor test really helped the students pull together the theory from all their course work, this integrative approach will provide this benefit to the students as they progress through the program rather than waiting for their senior year. Third, from a pragmatic perspective, the gradual introduction of the tester labs into the curriculum will allow the faculty to get up to speed on using the tester, introducing material as the lab projects are developed. The proposed learning objectives for each test laboratory are summarized in Table 2.

<table>
<thead>
<tr>
<th>Laboratory</th>
<th>Main Learning Objectives</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>Understand overall ATE architecture and how to control its programmable voltage and current sources</td>
</tr>
<tr>
<td>Logic Gate</td>
<td>Produce a test plan for the parametric testing of a logic gate Construct the test code for implementing the test plan</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Explain how to configure an ATE to measure capacitance</td>
</tr>
<tr>
<td>Opamp</td>
<td>Understand how to program the ATE arbitrary waveform generator Create a test plan for analyzing the frequency response of an opamp</td>
</tr>
<tr>
<td>FET</td>
<td>Determine the appropriate tests for screening FET parts Generate a test report with appropriate statistics for screened parts</td>
</tr>
<tr>
<td>DAC</td>
<td>Summarize how a DAC is characterized for linearity Develop the test code to measure and analyze DAC linearity</td>
</tr>
<tr>
<td>Counter</td>
<td>Produce a test plan based on the datasheet specifications for verifying the functionality and timing of a 4-bit counter IC Demonstrate the ability to troubleshoot a non-functioning IC</td>
</tr>
</tbody>
</table>

The sophistication of the labs will increase with each year, as the students grow in their knowledge of the electrical engineering field and are introduced to more features of the tester. For the freshman class, most of the code for the resistor test will be given to the students, and they can use the help function to reverse engineer it. By year two, the students will have had an
introductory course in structured programming and thus, will be expected to do more extensive writing of the test code. For the digital systems class, the students will be expected develop a test plan for verifying the logic levels of a basic logic gate IC given the standard datasheet for the part. As the students learn the fundamentals of sampling theory in Signals and Systems, more sophisticated labs such as testing a digital-to-analog converter (DAC) become possible. For the Microprocessor class, the students will be required to write test scripts that verify the correct timing and functionality of a 4-bit counter. A hardware bug will be built into the test board to give the students an opportunity to develop troubleshooting skills as they attempt to isolate the problem with a nonfunctioning part.

The three year plan for integrating semiconductor test into the curriculum is outlined in the following table.

Table 3. Lab Development Schedule

<table>
<thead>
<tr>
<th>Year</th>
<th>Tasks</th>
</tr>
</thead>
</table>
| 1    | Design of interface electronics (load boards)  
|      | Faculty and grad students learn to use tester and write test code  
|      | Develop first few labs, introduction into classes |
| 2    | Introduction of labs into correct course sequence  
|      | Continued development of remaining labs |
| 3    | Refine labs based on evaluation from preceding year  
|      | Introduce active learning features into labs  
|      | Plan for Senior Elective in VLSI Test |

We are currently in the midst of our first year of development. Our experiences and challenges to date are detailed in the next section. By the third year, we will be able to make plans for a comprehensive senior elective on semiconductor test. The plan is to further refine the labs by formally introducing aspects of active learning theory such as collaborative and problem-based learning to further enhance the effectiveness of the lab sessions and to emulate more closely an actual work-place environment.¹⁰,¹¹

The projected program outcomes as a result of this integrated approach include the following:
1. Change in student attitudes – students will be more motivated as they realize what they are learning has direct relevance in industry
2. Increased student retention as a result of outcome 1
3. Improvement in academic performance related to theory covered in the tester labs
4. Motivation for life-long learning

The results of hands-on laboratories and introduction of real-world examples through the test engineering classes has shown to result in a deeper understanding and longer retention of the material.⁶ Hence, we expect to see a correlation between improved scores on exams related to the material covered in the test labs. Changes in attitude and motivation will be monitored through
both in-class surveys and official end-of-semester student surveys. Student retention will be monitored at all years. It will be especially interesting to see the impact on 1301 on first year student retention.

While several advantages of the integrative approach have been noted, a potential drawback should be mentioned. Spreading out the tester labs over three years has the downside of loss of momentum and continuity. A review of the test engineering concepts learned from the previous semesters will be needed before each new lab is introduced. It is envisioned that extensive review, though, will be used to reinforce the material, and will be built into the labs as pre-reading assignments.

**First Year Experience**

In this section, a brief history of the development of our partnership and our experiences this first year are overviewed. Some preliminary student survey results are also discussed.

Initial discussions with SPEA were held in August 2010 with a formal kick off of the program at the beginning of the Fall 2010 semester. In addition, we contacted Texas A&M to get their input on their program.

Our plan for the first semester (Fall 2010) was to learn how to use the tester and design the required hardware (interface electronics and load board). Two of our faculty along with two graduate students worked closely with SPEA’s application engineers in developing the test scripts and lab material.

With regard to the hardware, it was decided to design a generic load board, one that would bring out all the relevant ATE I/O signals through a pair of 96 pin connectors. A smaller daughter board would be custom build for each set of required tests. This was deemed to provide the best

![Resistor daughter board and the generic load board](image)
option in terms of flexibility and cost. The load board measures 11 x 11 inches and is four layers. Each daughter board will be two layers and measures 4 x 5 inches square (see Figure 2). Provisions for some future expansion were built into the load board as more expansion boards are added to our tester. SPEA took on the task of completing the PCB design for the load board. Our institution worked on two daughter board designs this past fall (resistor test and counter test). This project helped us (faculty and grad students) get up to speed on how the tester is configured and programmed. The test scripts, daughter board, and write-up of the lab for the resistor test were completed. The counter test board and lab write-up are scheduled to be completed before the end of the spring semester.

At the end of the fall semester, we introduced the SPEA tester into several of our classes. In an Introduction to VLSI Design class (EENG 4331 = senior elective, EENG 5334 = graduate class), a lecture on VLSI testing was given, followed by an overview of the SPEA tester as an example of a typical industrial ATE tester and a demonstration of it running the resistor test. In a junior year Linear Circuits class (EENG 3305), a brief 10 minute overview of the tester was given. The junior year Signals and Systems class (EENG 4311) performed the resistor test lab using the SPEA tester in the Spring 2011 semester. All the students were surveyed to get some initial feedback on their interest and attitudes towards test engineering. The questions and responses are summarized in Table 4. There are a couple observations of note. First, the EENG 3305 and 4311 classes were essentially composed of the same students. The experience of completing the resistor lab resulted in an increased interest in semiconductor testing and exposure to real-world test issues. Second, it should be noted that none of the graduate students in the EENG 5334 class did their undergraduate studies at The University of Texas at Tyler and seemed to be more satisfied with the exposure to real-world test issues in the curriculum.

### Table 4. Student Survey Results

*(Scale: 1 = Strongly Disagree, 2 = Disagree, 3 = Neutral, 4 = Agree, 5 = Strongly Agree)*

<table>
<thead>
<tr>
<th>Question</th>
<th>EENG 3305</th>
<th>EENG 4311</th>
<th>EENG 4331</th>
<th>EENG 5334</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Integration of real-world test issues into the EE curriculum is important.</td>
<td>4.14</td>
<td>4.63</td>
<td>4.11</td>
<td>4.18</td>
</tr>
<tr>
<td>2. There is already enough exposure to real-world testing issues in the EE curriculum at the present</td>
<td>2.71</td>
<td>2.38</td>
<td>2.50</td>
<td>3.41</td>
</tr>
<tr>
<td>3. I would like to learn more about using the SPEA Mixed-Signal Tester</td>
<td>4.29</td>
<td>4.50</td>
<td>3.44</td>
<td>4.00</td>
</tr>
<tr>
<td>4. I would like see an elective/graduate class devoted to semiconductor testing</td>
<td>4.14</td>
<td>4.38</td>
<td>4.11</td>
<td>4.00</td>
</tr>
<tr>
<td>Sample size</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>17</td>
</tr>
</tbody>
</table>

Classes: Linear Circuits II = EENG 3305, VLSI Design = EENG 4331 (undergraduate) Signals and Systems = EENG 4311, = EENG 5334 (graduate)
Conclusions
This paper has outlined a three year plan to collaborate with SPEA on integrating test engineering into our undergraduate curriculum. The experiences to date have shown that it is vital to have the support of the ATE vendor in learning how to use their equipment and in developing practical tests. Building upon the experiences of another institution with an ATE machine in their curriculum (Texas A&M) has also been very beneficial. Many of their test lab projects will serve as the foundation for the lab projects to be used with the SPEA tester. Learning how to write the test code for a complex instrument such as an ATE tester has been challenging but has given us a better perspective on how to teach the students. For example, our decision to give the students most of the code for the resistor test, the first lab they will encounter, and let them reverse engineer it, arose out of our own learning experiences under the guidance of the SPEA application engineers. In addition, developing the labs with SPEA’s engineers have ensured that the students will develop practical skills. For example, the decision to place a hardware bug in the counter test board arose out of a concern from the application engineers that the practicing test engineer should have the ability to troubleshoot and solve problems in the field. The initial survey results indicating student interest in learning how to use the new tester are encouraging.

In sum, the collaborative effort with our industry partner has generated excitement among both the faculty and students as the introduction of real-world test experiences into curriculum is expected to have a significant impact on the educational value of our program. The unique approach being tested in this college-industry partnership is to introduce test engineering across the BSEE curriculum as opposed to a single technical elective course. It is anticipated that such an approach will expose students to real career opportunities throughout their studies and provide industry with a pool of trained graduates.

Acknowledgments
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References
5. Presentation at the *Industry and Academia Roundtable*, held at Texas A&M University, May 21, 2010.

